ENGR 3426: Final Project

Proposal due November 7, 2016
Design Review 1 November 17, 2016
Design Review 2 December 8, 2016
Report due December 16, 2016

For the remainder of the semester you will be working in groups of two or three to design a mixed-signal integrated circuit. The circuit must have some kind of analog circuitry and some kind of digital circuitry that interact with each other and must fit within the size, time, and technological constraints that you are under. You should form project groups around project ideas that are of mutual interest. By the start of class on Monday, November 7, each project group must submit a brief (i.e., one or two pages) proposal describing the project that you hope to undertake along with any references that you have consulted in forming your initial idea/approach. We will hold design reviews in class on Thursday, November 17, and on Thursday, December 8. Each group will need to submit their final chip design and a project report documenting the design and providing an initial testing plan by Friday, December 16.

Project Ideas

The following list of suggested project ideas is meant as a starting point for developing your own project idea. In most cases, I have provided some references that I believe are interesting approaches or provide relevant background to the type of circuit described in a given heading. You are free to adopt or adapt one of these for your project or you can do something completely different.

1. **Integrating (Ramp) ADC**. An ADC architecture with very low hardware complexity that capable of high resolution but supports only relatively low sampling rates. (See section 29.2.4 of R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS: Circuit Design, Layout, and Simulation*, Piscataway, NJ: IEEE Press, 1998).

2. **Time-Based ADC**. A very interesting ADC architecture that combines ideas from ramp ADCs with ideas from algorithmic ADCs. (See J. Jung and S. Shin, "Low-Power Time-Based ADC with Alternating Time-Residue Amplification," *Electronics Letters*, vol. 52, no. 22, pp. 1845-1847, 27 October 2016; H. Y. Yang and R. Sarpeshkar, "A Bio-Inspired Ultra-Energy-Efficient Analog-to-Digital Converter for Biomedical Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 11, pp. 2349-2356, 2006; H. Y. Yang and R. Sarpeshkar, "A Time-Based Energy-Efficient Analog-to-Digital Converter," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 8, pp. 1590-1601, 2005).

3. **Current-Steering DAC with Dynamic Element Matching**. A simple current-output DAC architecture in which 2^n unit current sources are switched onto an output line when the nth bit of the input word is high. Dynamic element matching is an electronic trimming approach for producing very well matched unit current sources, reportedly capable of achieving matching sufficient for 16-bit resolution DACs. (See

H. J. Schouwenaars, D. W. J. Groeneveld, and H. A. H. Termeer, "A Low-Power Stereo 16-bit CMOS D/A Converter for Digital Audio," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 6, pp. 1290-1297, 1988; D. W. J. Groeneveld, H. J. Shouwenaars, H. A. H. Termeer, and C. A. A. Bastiaansen, "A Self-Calibration Technique for Monolithic High-Resolution D/A Converters," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 6, pp. 1517-1522, 1989).

4. **Charge-Redistribution Successive Approximation Register (SAR) ADC**. An ADC architecture that uses a DAC, a comparator, and a register to generate one bit of the result per clock cycle in a register called the *successive approximation register*. (See sections 29.1.5 and 29.2.5 of R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS: Circuit Design, Layout, and Simulation*, Piscataway, NJ: IEEE Press, 1998).

5. **Zero-Crossing-Based ADCs**. Design an ADC based on a relatively new family of switched-capacitor circuits that used open-loop comparators instead of closed-loop op amps. (See H.-S. Lee, L. Brooks, C. G. Sodini, "Zero-Crossing-Based Ultra-Low-Power A/D Converters," *Proceedings of the IEEE*, vol. 98, no. 2, pp. 315-332, 2010; J. K. Fiorenza, T. Sepke, P. Holloway, C. G. Sodini, H.-S. Lee, "Comparator-Based Switched-Capacitor Circuits for Scaled CMOS Technologies," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2658-2668, 2006; for an example hot off the presses, see Y. Shen, S. Liu, and Z. Zhu, "A 12-bit 50MS/s Zero-Crossing-Based Two-Stage Pipelined SAR ADC in 0.18 μm CMOS," *Microelectronics Journal*, vol. 57, pp. 26-33, 2016).

6. **MOS-R-2R-Ladder-Based DAC/ADC**. Design a current-output DAC, based on an R-$2R$-like ladder network of MOS transistors or use such a DAC to design a SAR ADC. (See C. M. Hammerschmied and Q. Huang, "Design and Implementation of an Untrimmed MOSFET-Only 10-Bit A/D Converter with −79-dB THD," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 8, pp. 1148-1157, 1998; B. Linares-Barranco, T. Serrano-Gotarredona, and R. Serrano-Gotarredona, "Compact Low-Power Calibration Mini-DACs for Neural Arrays With Programmable Weights," *IEEE Transactions on Neural Networks*, vol. 14, no. 5, pp. 1207-1216, 2003).

7. **Harmonic Cancelling Sine-Wave Generator**. A relatively low-complexity architecture for digitally synthesizing high-quality sine waves. (See P. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, "A Simple Digital Architecture for a Harmonic-Cancelling Sine-Wave Synthesizer," in *Proceedings of the 2014 IEEE International Symposium on Circuits and Systems*, Melbourne, Australia, 1-5 June 2014, pp. 2113-2116; P. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, "Design of a Digital Harmonic-Cancelling Sine-Wave Synthesizer with 100 MHz Output Frequency, 43.5 dB SFDR, and 2.26 mW Power," in *Proceedings of the 2015 IEEE International Symposium on Circuits and Systems*, Lisbon, Portugal, 24-27 May 2015, pp. 3052-3055; P. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, "The Effect of Amplitude Resolution and Mismatch on a Digital-to-Analog Converter Used for Harmonic-Cancelling Sine-Wave Synthesis," in *Proceedings of the 2016 IEEE*

International Symposium on Circuits and Systems, Montreal, Canada, 22-25 May 2016, pp. 2018-2021).

8. **Chopper-Stabilized Operational Amplifier**. Chopper stabilization is a technique for eliminating both the offset voltage (i.e., reducing it to a few μVs) of an op amp arising from component mismatch and low-frequency (i.e., $1/f$) noise. (See C. C. Enz, E. A. Vittoz, and F. Krummenacher, "A CMOS Chopper Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 3, pp. 335-342, 1987; C. C. Enz and G. C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584-1614, 2002).

9. **"Digital" Phase-Locked Loop**. A mixed-signal circuit block commonly used in digital communication systems for clock and data recovery comprising a controllable ring oscillator, a phase detector, and a negative feedback loop that adjusts the oscillators output to match the frequency and phase of an external clock signal. (See chapter 19 of R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS: Circuit Design, Layout, and Simulation*, Piscataway, NJ: IEEE Press, 1998).

10. **Integrated CMOS Temperature Sensor**. Design a temperature sensor based on a PTAT circuit and clever circuit techniques to produce an accurate, calibrated temperature output in an analog or digital format. (See M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS Smart Temperature Sensor With a 3σ Inaccuracy of ± 0.1°C from -55°C to 125°C," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2805-2815, 2005).

11. **Continuous-Time Digital Signal Processing**. DSP without sampling and aliasing. (See Y. Tsividis, "Digital Signal Processing in Continuous Time: A Possibility for Avoiding Aliasing and Reducing Quantization Error," in *Proceedings of the 2004 IEEE International Conference on Acoustics, Speech, and Signal Processing*, Montreal, Canada, 17-21 May 2004, vol. II, pp. 589-592; B. Schell and Y. Tsividis, "A Continuous-Time ADC/DSP/DAC System With No Clock and With Activity-Dependent Power Dissipation," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 11, pp. 2472-2481, 2008).