ENGR 3426: Machine Problem 4

due October 31, 2016

In this machine problem, you will need to design a switched-capacitor amplifier circuit that computes during an evaluate phase of operation the relationship

$$V_{\text{out}} = 2V_{\text{in}} - V_{\text{ref}}$$

for (possibly time-varying) signals V_{in} and V_{ref} in the range of 0 V to 3 V. Such a circuit is commonly used as a building block in certain types (e.g., algorithmic) of analog-to-digital converters (ADCs).

For the op amp, you should use the folded-cascode amplifier that you designed for MP3. As you did in MP3, you should run the op amp on a single-ended 5-V supply and you can supply the required bias current from a single independent current source. You can use pulse or PWL voltage sources (with reasonable rise and fall times) to generate any clock signals required by your design. Given the specified range of input voltages, you should be able to use *n*MOS transistors as switches. For the capacitors, you should use poly-poly2 capacitors. In laying out your caps, you should follow the unit-matching principle, in which you connect an integer number of unit devices in parallel to obtain a given ratio. You should use a unit capacitor of about 1 pF. Otherwise, you do not need to worry about things like compesation tabs, common-centroid geometries, and dummy devices for the capacitors in your design. You should make your design hierarchical so that the op amp and bias circuit(s) are subcells within the top-level switched-capacitor amplifier cell. You do not, however, need to make the capacitor banks or switch transistors subcells.

Your final design must be free of DRC errors and must pass LVS. You will need to submit (both pre- and post-layout) simulation results showing that your circuit implements the specified relationship. You will also need to submit a brief written report explaining your design approach, showing schematics, layout design, and simulation results. You will also need to submit evidence showing that your design passes LVS. In addition to submitting this report, you will need to submit all of your schematics, circuit symbols, and cell layouts.