ENGR 3426: Machine Problem 3

due October 17, 2016

In this machine problem, you will learn about and design a single-stage differential amplifier circuit comprising a *p*MOS differential pair, a low-voltage cascode current mirror, and two pairs of *n*MOS transistors in a circuit arrangement called a *folded cascode*. This amplifier is conceptually quite similar to the five-transistor differential amplifier and to the current-mirror differential amplifier that you investigated near the end of ENGR 2420. This type of amplifier is called a *folded-cascode* differential amplifier. In addition to submitting the items requested below, you will need to bundle all of your schematics, circuit symbols, and cell layouts into a zip archive or a tarball and submit these via e-mail.

1. **Grok the Circuit**. This question has been constructed to help you prepare to do the rest of this machine problem efficiently. Please complete this question first *before* you fire up LTspice. Unless otherwise stated, you should assume that like transistors match and that the Early effect is negligible.

   (a) Consider the differential amplifier circuit shown in the attached schematic comprising a *p*MOS differential pair, four *n*MOS transistors, and a *p*MOS low-voltage cascode current mirror. Such a circuit is called a folded-cascode differential amplifier. Transistors M_5 and M_6 act as cascode transistors, pinning the drains of the diff-pair transistors, M_1 and M_2. Transistors M_3 and M_4 act as current sinks, providing pivot points for *folding* over the differential-pair output currents. Which input voltage is the noninverting input? Which is the inverting input? Explaing your reasoning briefly.

   (b) What is the allowable common-mode input voltage range of this circuit? Explain your reasoning.

   (c) If the output voltage were fixed by a voltage source somewhere in the middle of the rails, what would be the output current in terms of I_1 and I_2 if the Early effect were negligible?

   (d) Do we need to make the bias current sunk by M_3 and M_4 equal to the diff-pair bias current, I_b? If so, explain why. If not, what constraints exist on this current level with respect to I_b?

   (e) Using the basic low-voltage cascode bias circuit that we discussed in class as a starting point, design a bias circuit for the folded-cascode amplifier that receives input from a single current source, I_b, and generates cascode bias voltages, V_{cn} and V_{cp}, optimally for a given bias current I_b so as to maximize the output voltage swing of the amplifier. Your circuit must also generate the other bias voltages, $V_{\mathrm{b}n}$ and $V_{\mathrm{b}p}$, so that $I_3 = I_4 = I_\mathrm{b}$.

2. **Schematic Capture and Simulation**. Using LTspice, implement the folded-cascode differential amplifier and associated bias circuit. You should place each of these into its own schematic, create appropriate symbols for them, and instance them inside a

test harness for running your simulations. You should make each unit transistor (i.e., both nMOS and pMOS) have an effective width of $36\,\mu$m and a length of $1.8\,\mu$m. You should run your amplifier on a single-ended +5-V power supply and you should set the bias current I_b so as to obtain a gain-bandwidth product of 1 MHz with a 2-pF load capacitor using a single external bias current source.

(a) **Voltage Transfer Characteristics**. Perform a simulation to obtain VTCs as you sweep the noninverting input for at least five different values of the inverting-input voltage that are spread evenly throughout the allowable common-mode input-voltage range. Turn in a plot showing these VTCs. What is the DC gain of this circuit from the slope of the VTCs?

(b) **Voltage-to-Current Transfer Characteristics**. Fix the output voltage of the amplifier somewhere in the middle of the rails so that all of the transistors in the output branch will operate in saturation. For a single value of the inverting input voltage (choose one of those for which you measured a VTC), measure the ouput current as you sweep the noninverting input around the inverting input voltage. Turn in a plot showing the amplifier's voltage-to-current characteristics. What is the incremental transconductance gain of the circuit? What are the limiting values of the output current?

(c) **Loopgain**. Connect a 2-pF capacitor between the output of your amplifier and ground. Attach a DC source to the noninverting input and adjust its value to match the voltage that you used for the simulation of the circuit's voltage-to-current transfer characteristics. Simulate the loopgain of your circuit by attaching an AC voltage source in the feedback loop, as discussed in the tutorial video. You can use a 1-V AC magnitude and a phase of zero degrees for convenience. Perform an AC analysis on the circuit, measuring the loopgain of the circuit from 1 Hz to 1 GHz. Turn in a plot showing the magnitude (in dB) and phase (in degrees) of the amplifier's loopgain. How does the low-frequency gain compare with the one you obtained from the VTC? What is the unity-gain crossover frequency? How does this value compare with the one you would expect from the circuit's load capacitance and its incremental transconductance gain?

(d) **Unity-Gain Follower Frequency Response**. With the 2-pF load capacitor in place, connect your amplifier as a unity-gain follower. Using the same DC offset as you have been using, perform an AC analysis of your circuit over the same range of frequencies that you just used for the open-loop response. Turn in a plot showing the magnitude and phase response of the circuits transfer function. How does the corner frequency in the circuit's response compare to the unity-gain crossover frequency in the loopgain?

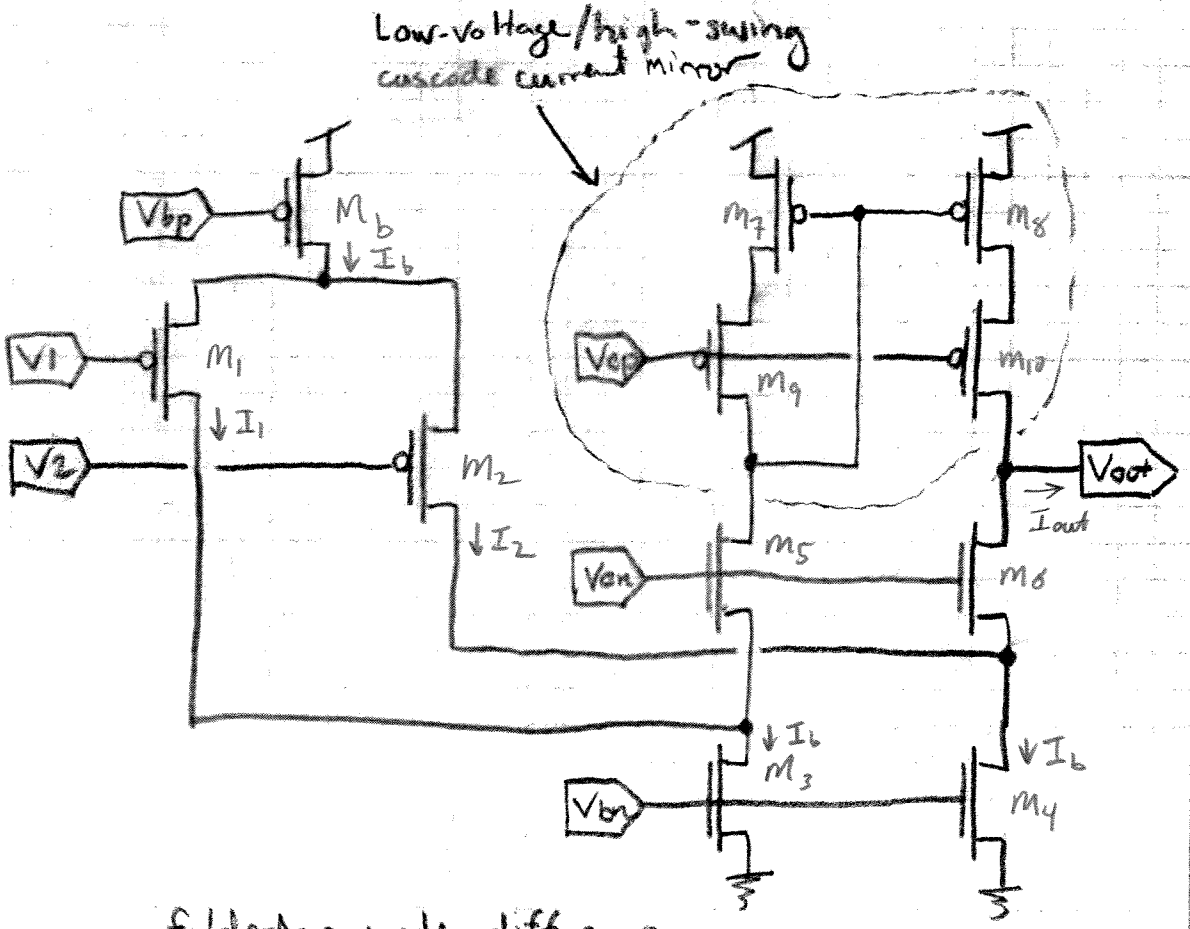
(e) **Small-Signal Step Response**. Replace the AC voltage source on the input of your unity-gain follower with a pulse or PWL voltage source. Performa a transient simulation showing the response of your circuit to a small-amplitude step in both the up-going and down-going directions, starting at the input level that you have been using consistently throughtout. What considerations go into deciding how small to make your input step? Adjust the time course of your simulation so that

you can see V_{out} just settle into its final value for the steps in both directions. Is the response symmetrical? Does the amplifier exhibit approximately linear behavior? Extract a time constant for both the up-going and the down-going transitions. How do these compare with each other? How do these compare with the corner frequency from the frequency response simulation?

(f) **Large-Amplitude Step Response**. Increase the amplitude of your input step to a couple of volts. Adjust the time course of the simulation so that you can see V_{out} get to its final values in both directions. Turn in a plot showing the circuit's large-amplitude step response. Is the response of the circuit to the large-amplitude steps symmetrical? Extract slew rates for both the up-going and down-going step responses. How do these compare to the slew rate you would expect from the load capacitnace and limiting output current values?

3. **Layout Design**. Using Glade, lay out a folded-cascode differential amplifier and its associated bias circuit. You should put the amplifier and the bias circuit in different subcells. In doing your layout, you should make the circuit as small as possible and follow as many of the analog layout considerations for matching as you can. The final cell must include appropriate substrate and well contacts and must pass DRC.

4. **Layout Versus Schematic**. Extract netlists of your folded-cascode differential amplifier and bias circuit both the schematic and the layout and use Gemini to compare the two netlists. If they are not equivalent, you will need to find and rectify any differences. You will need to submit the LVS output showing that the two netlists match.



folded-cascode diff amp