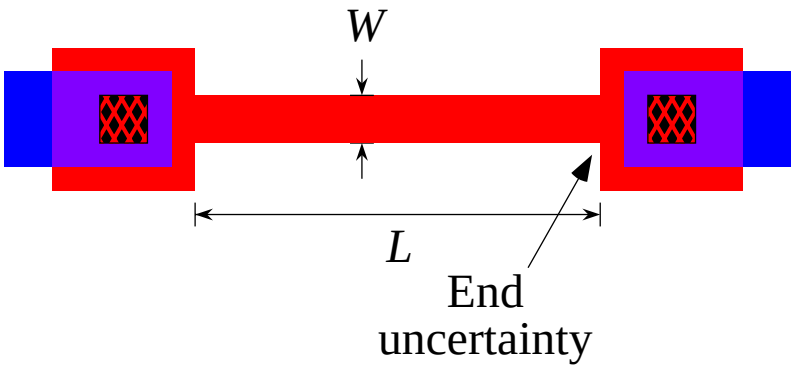
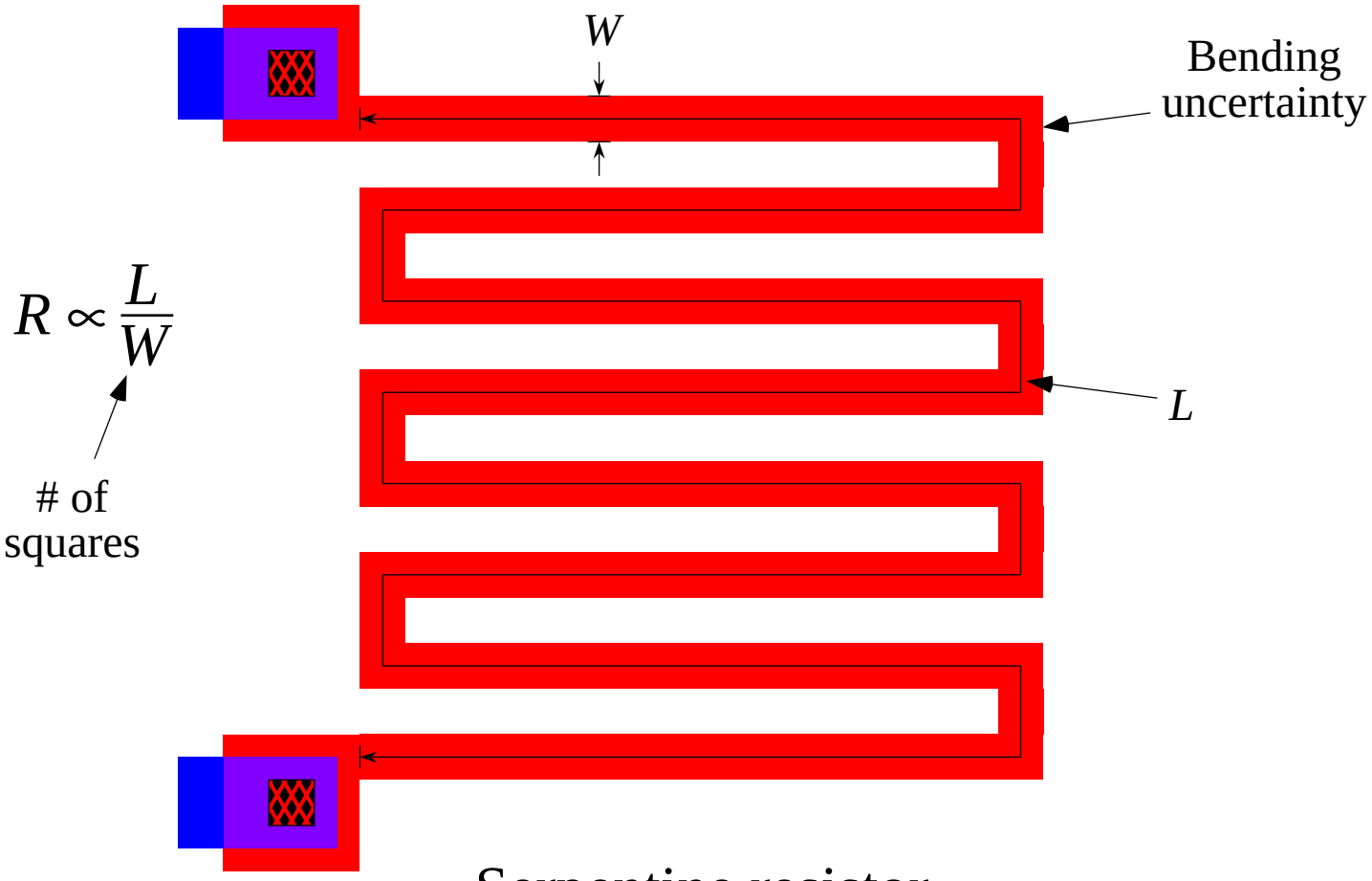
Layout for Analog Integrated Circuits

- Layout is the process of specifying the physical placement of and interconnections between all of the devices in a circuit.
- Layout is used to generate all of the mask layers used for chip fabrication.
- Layout for digital circuits:
  - Usually many transistors
  - Many transistors are minimum size
  - Transistors are sized to minimize delays
  - Focus on interconnections between modules
- Layout for analog circuits:
  - Usually relatively few transistors
  - Few transistors are minimum size
  - Transistors are sized to minimize offsets
  - Focus on optimizing individual devices

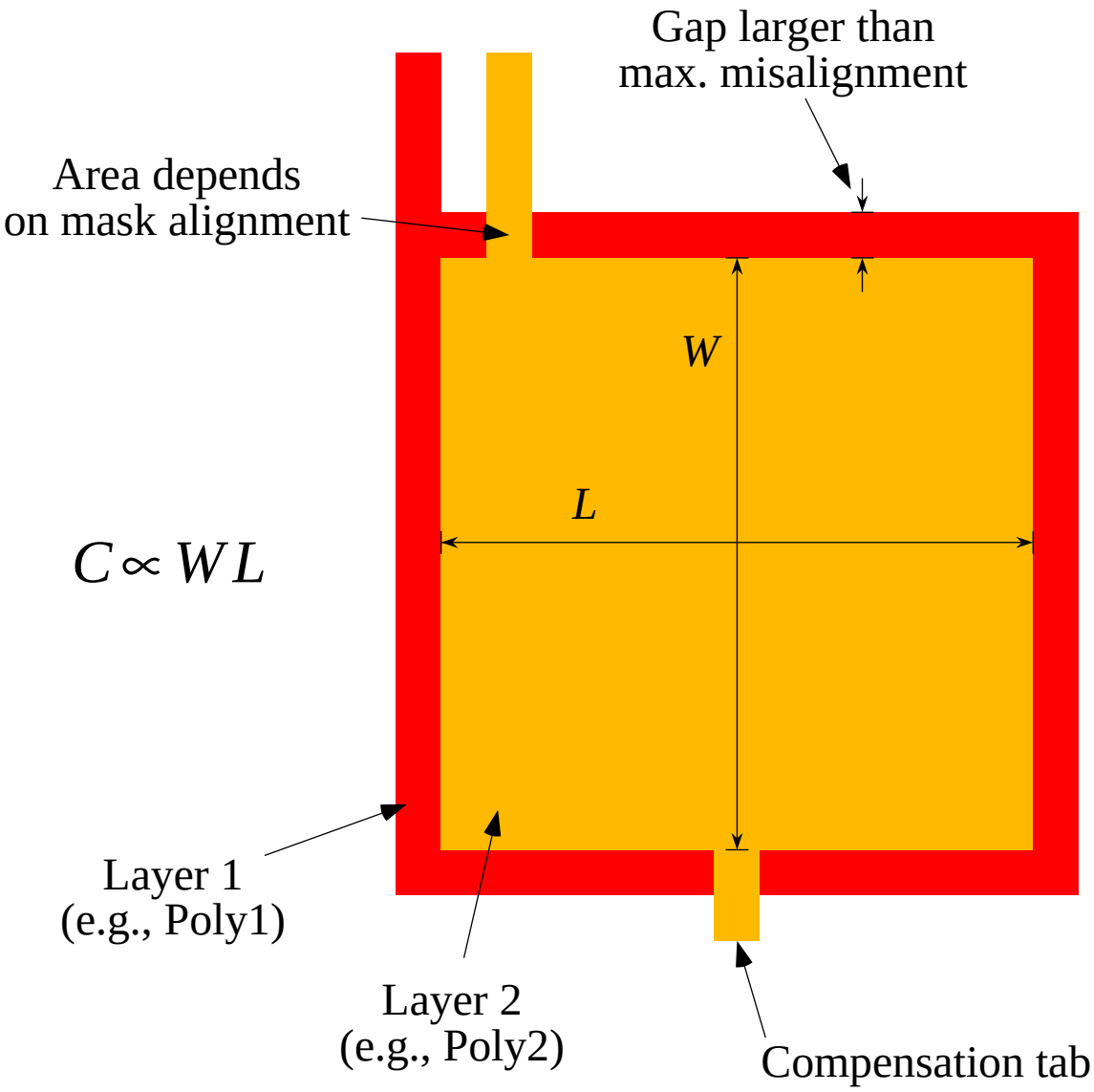
Resistors





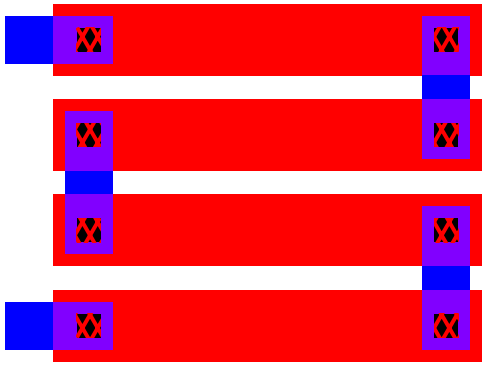
Serpentine resistor
large L/W

Capacitors


Gap larger than
max. misalignment
Area depends
on mask alignment
W
L
$C \propto WL$
Layer 1
(e.g., Poly1)
Layer 2
(e.g., Poly2)
Compensation tab

Control of Absolute Component Values

- Control device geometries by avoiding uncertainties.
  Examples:
  - Stacked vs serpentine MOS transistors
  - Bending uncertainties in a resistor controlled by a low resistivity layer



- Avoid using minimum dimensions.

$$R = R_{\square}\frac{L}{W} \qquad C = C_S WL$$

$$\frac{\Delta R}{R} = \underbrace{\frac{\Delta R_{\square}}{R_{\square}}}_{\text{indep. of } W \text{ \& } L,\ \sim 5\text{–}50\%} + \underbrace{\frac{\Delta L}{L} - \frac{\Delta W}{W}}_{\text{minimize by making } W >> W_{min} \text{ and } L >> L_{min}} \qquad \frac{\Delta C}{C} = \underbrace{\frac{\Delta C_S}{C_S}}_{\text{indep. of } W \text{ \& } L,\ \sim 5\text{–}50\%} + \underbrace{\frac{\Delta L}{L} + \frac{\Delta W}{W}}_{\text{minimize by making } W >> W_{min} \text{ and } L >> L_{min}}$$

- Good circuit designs minimize reliance on absolute component values.

Layout for Device Matching

- Devices on the same die can match well (precision):

$$\frac{\Delta C}{C} \sim 0.1\% \qquad \frac{\Delta R}{R} \sim 0.1\% \qquad \frac{\Delta I_s}{I_s} \sim 1\text{–}10\%$$

- For circuits characteristics (e.g., gains) that depend on ratios of component values,

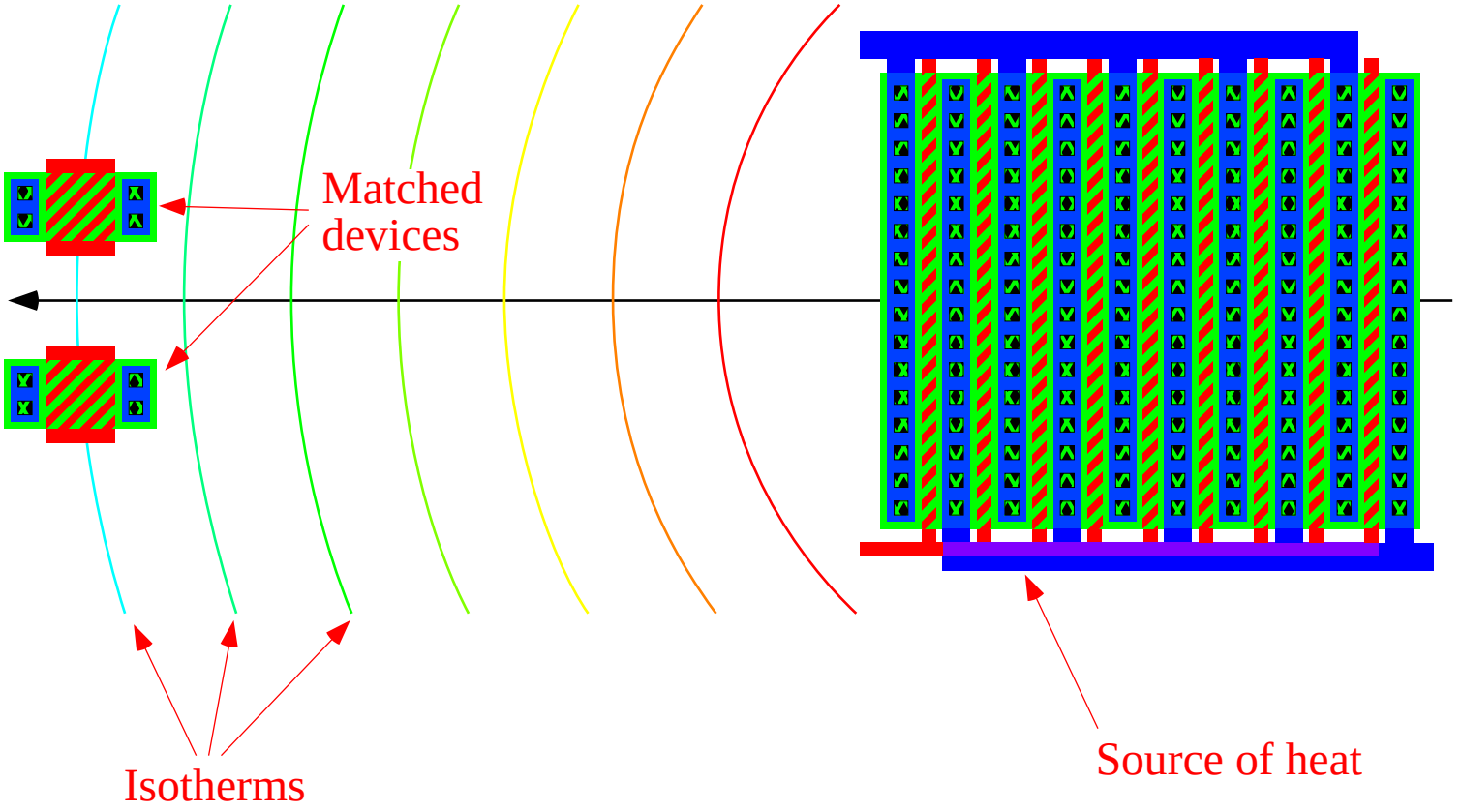
  Precise matching ⇒ Accurate characteristics

- To improve device matching, use devices with
  - Same temperature
  - Identical shape and size
  - Minimum spacing
  - Common centroid geometries
  - Same orientation
  - Same surroundings
  - Nonminimum size

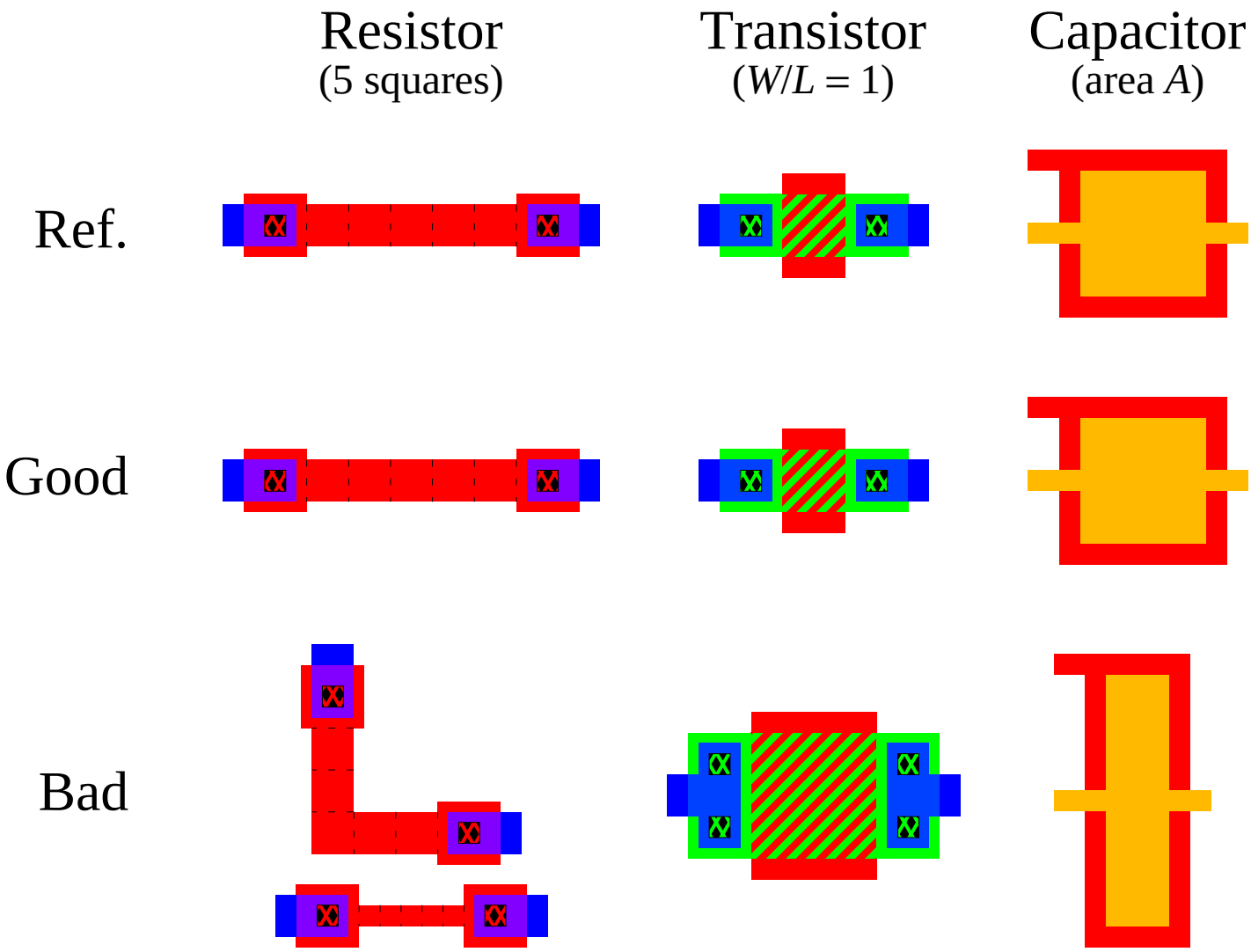
- *Caveat emptor!* The relevance of each "rule" depends on particulars of the process and devices involved.

Matching: Same Temperature

- Not a serious problem if the total power dissipation on chip is low enough (e.g., subthreshold CMOS).
- Place devices symmetrically with respect to the source of heat along an isotherm:



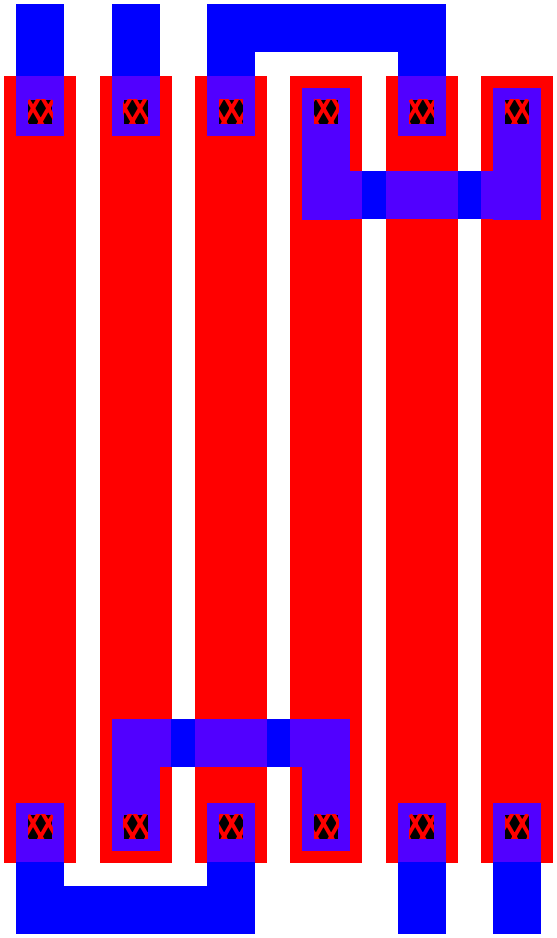
Matching: Identical Shape and Size



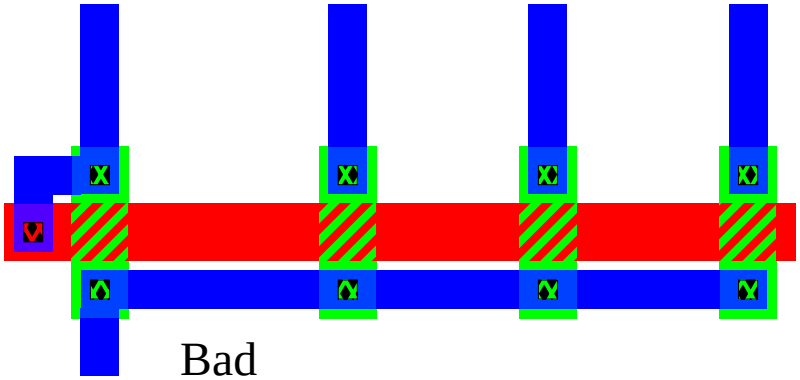
Matching: Minimum Distance

- Take advantage of spatial correlations.
- Place devices as close together as possible.
- Examples:

Matched Resistors

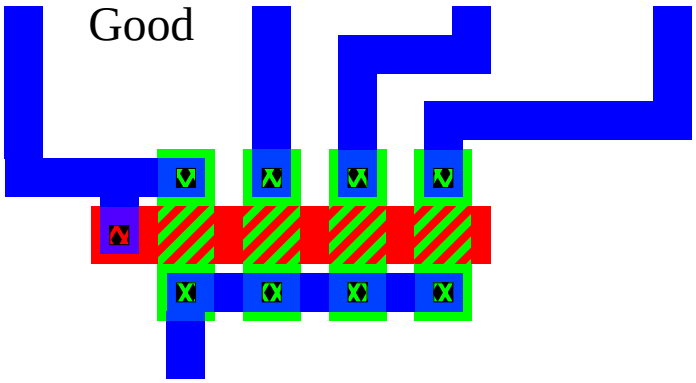


3-Output Current Mirror



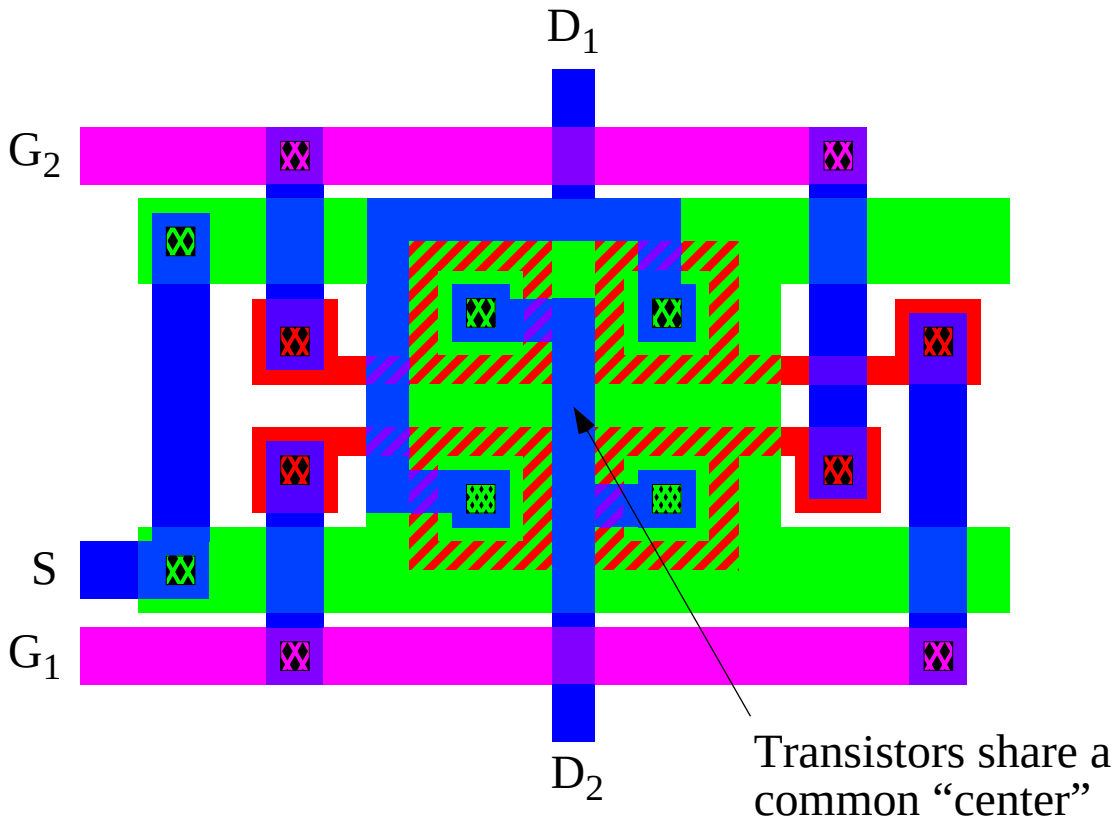
Bad

Good



Matching: Common Centroid

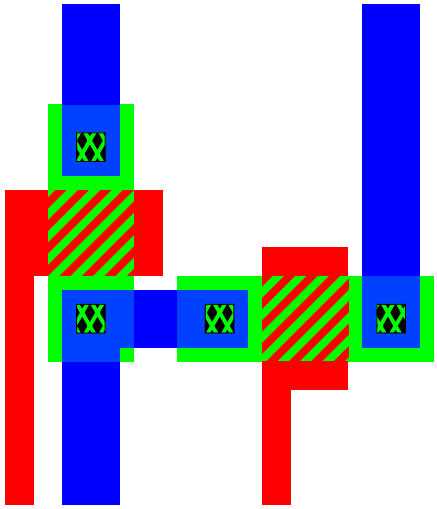
- Compensation of constant gradients
  - Temperature
  - Oxide thickness
  - Substrate Doping
- Example: Cross-coupled quad



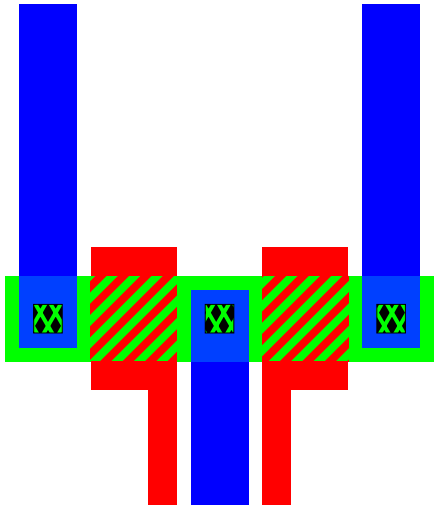
- Complicated layout ⇒ not practical for > 2×2

Matching: Same Orientation

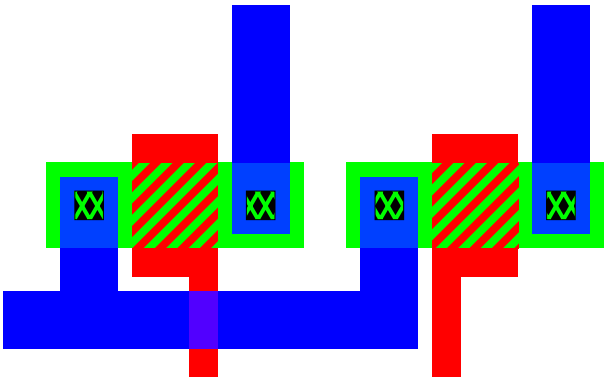
- Eliminate mismatch arising from:
  - Anisotropic substrate
  - Anisotropic process steps
  - Packaging-induced stresses
- Example: Differential Pair



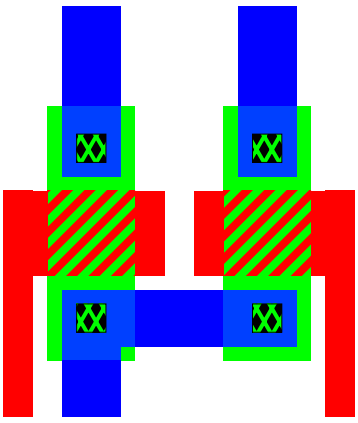
Ugly



Bad



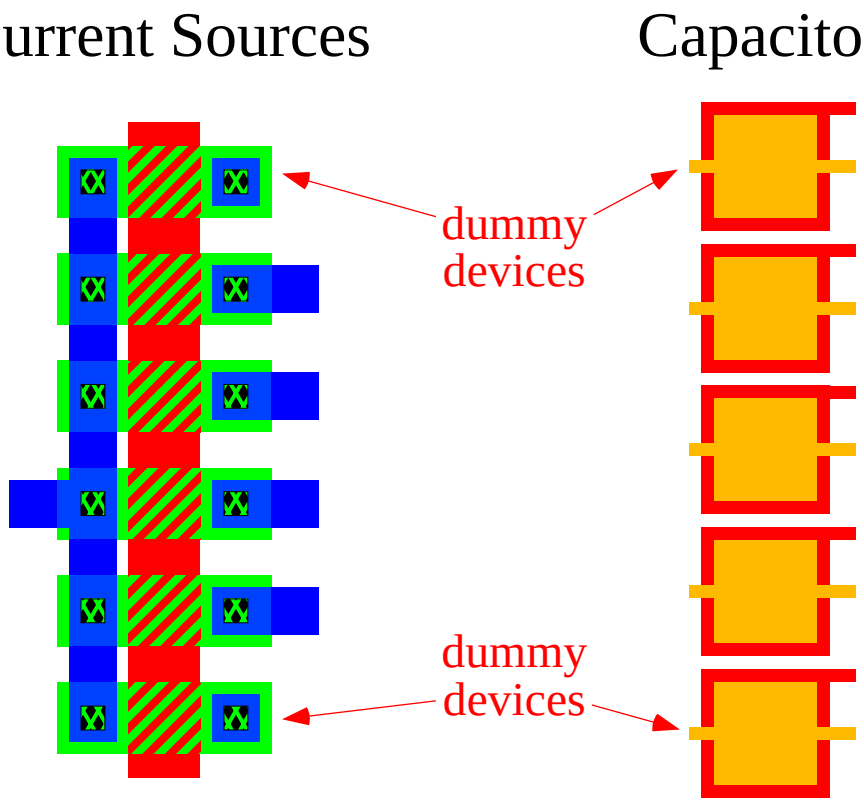
Fair



Good

Matching: Same Surroundings

- Reasons are not always clear. Possibilities include:
  - Fringing fields
  - Nonuniform lithography
  - Nonuniform etching during processing
- Use dummy devices to make all functional devices have the same surroundings.
- Examples:

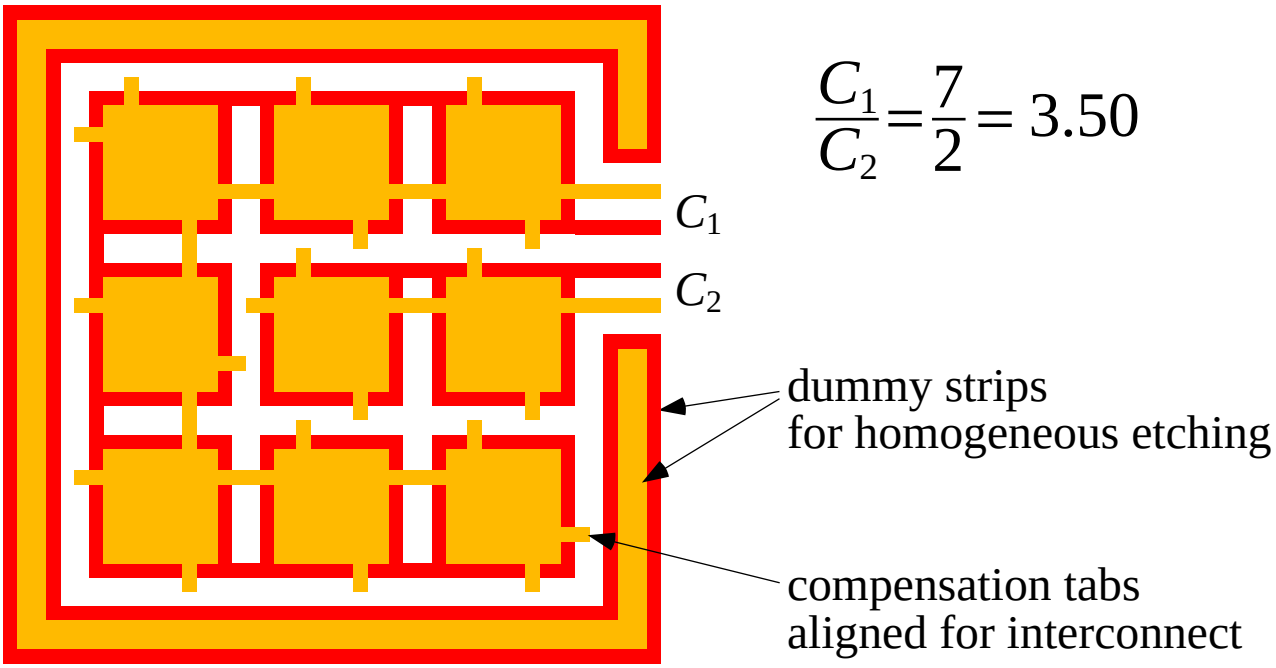


- Sometimes the surround can be simulated adequately with dummy strips.

Matching for Non-Unity Ratios

- For n/m ratios, use $n+m$ unit devices:

Example: Capacitors



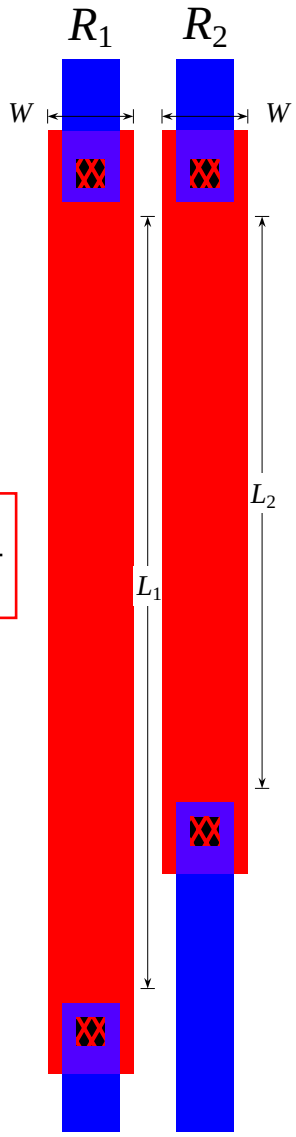
$$\frac{C_1}{C_2} = \frac{7}{2} = 3.50$$

Matching for Non-Unity Ratios

- For arbitrary ratios, violate matching rules optimally.

Examples:

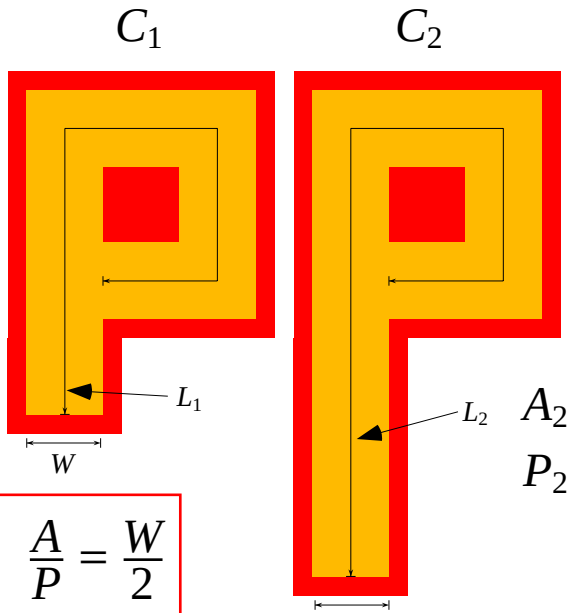
Resistors



$$\frac{R_2}{R_1} = \frac{L_2}{L_1}$$

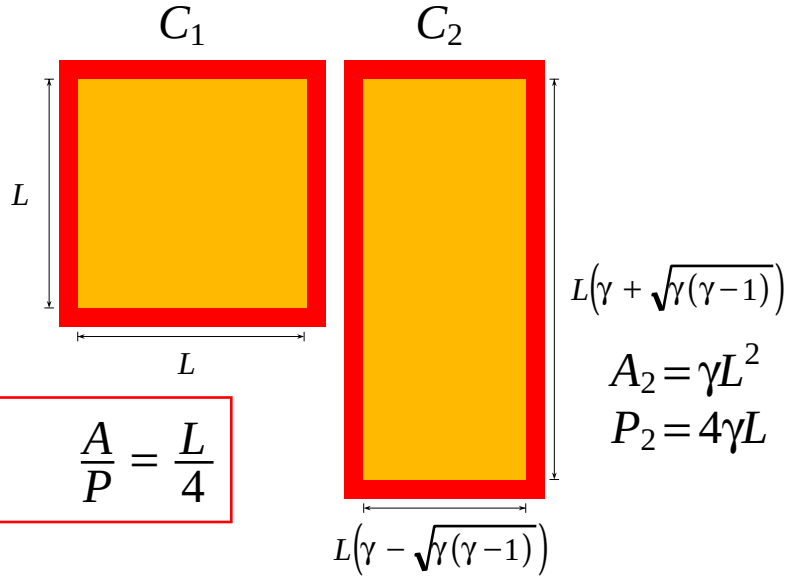
Same W,
$L_1 >> L_{min}$, $L_2 >> L_{min}$

Capacitors



$$A_1 = WL_1$$
$$P_1 = 2L_1$$
$$A_2 = WL_2$$
$$P_2 = 2L_2$$

$$\frac{C_2}{C_1} = \frac{L_2}{L_1} \qquad \frac{A}{P} = \frac{W}{2}$$



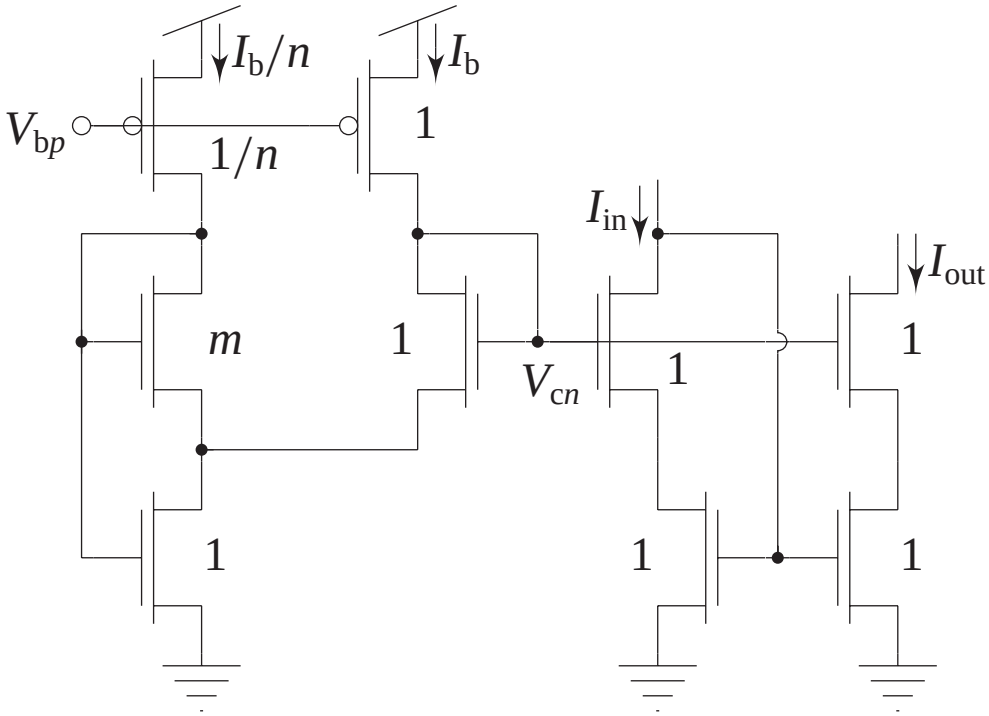
$$A_1 = L^2$$
$$P_1 = 4L$$
$$A_2 = \gamma L^2$$
$$P_2 = 4\gamma L$$

$$\frac{C_2}{C_1} = \gamma \qquad \frac{A}{P} = \frac{L}{4}$$

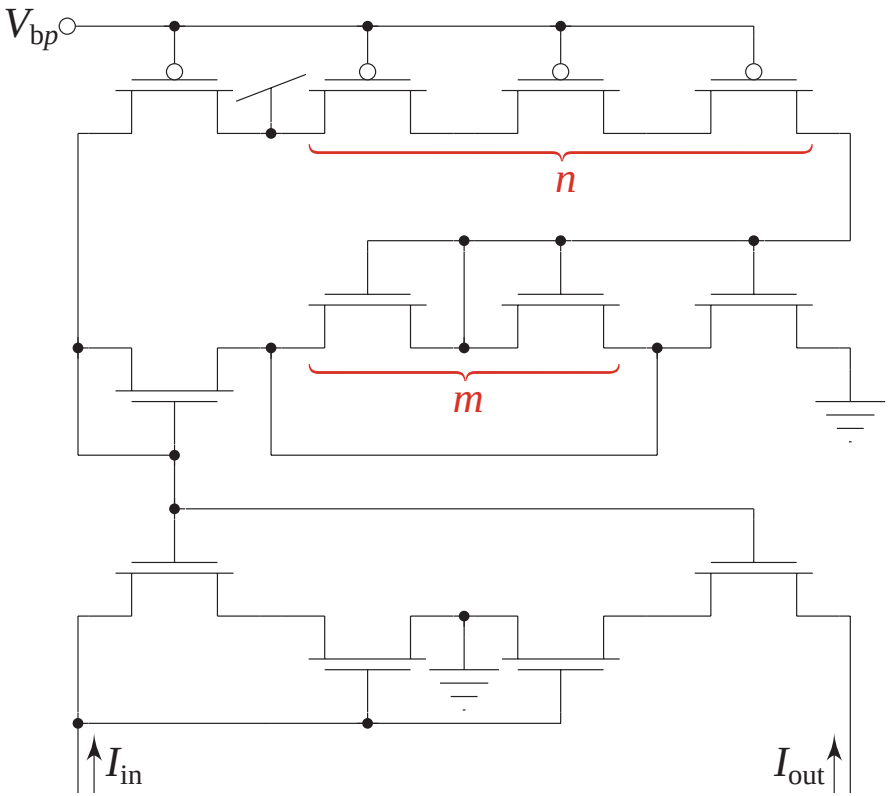
Same area:perimiter ratio

Layout Considerations for a Low-Voltage Cascode Current Mirror

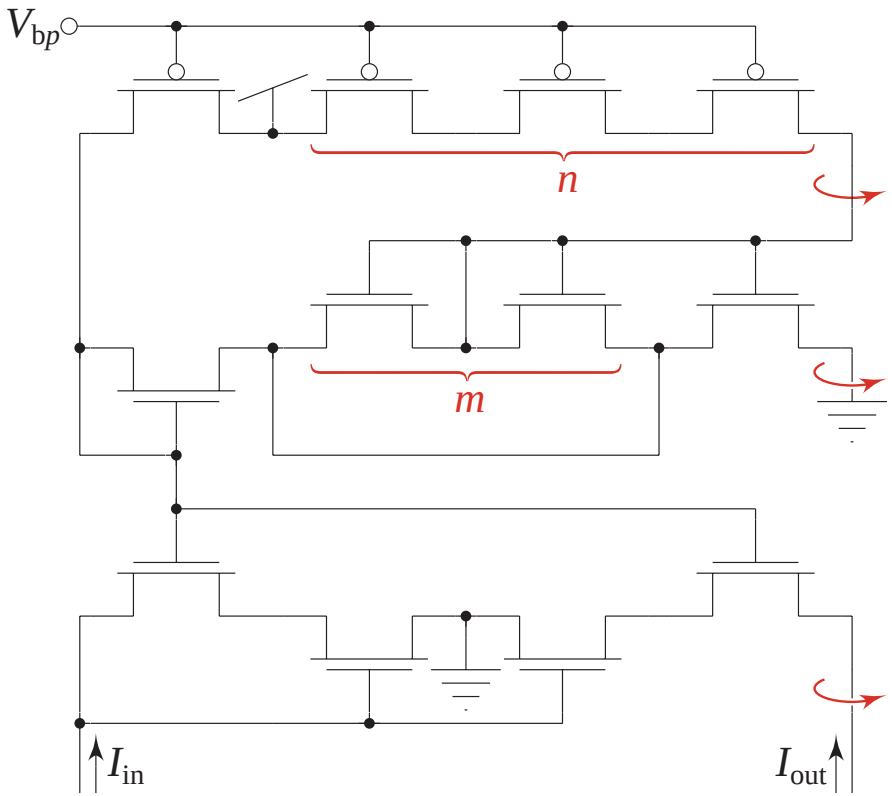
- To get accurate ratios, we implement the *n*MOS of width *m* as a parallel connection of *m* unit transistors.
- Similarly, we implement the *p*MOS of length *n* as a series connection of *n* unit transistors.
- If we choose *m* to be even, we can optimally share source/drain regions of the *n*MOS transistors in the bias circuit.
- If we choose $n = m + 1$, we have as many *p*MOS strips as *n*MOS strips.



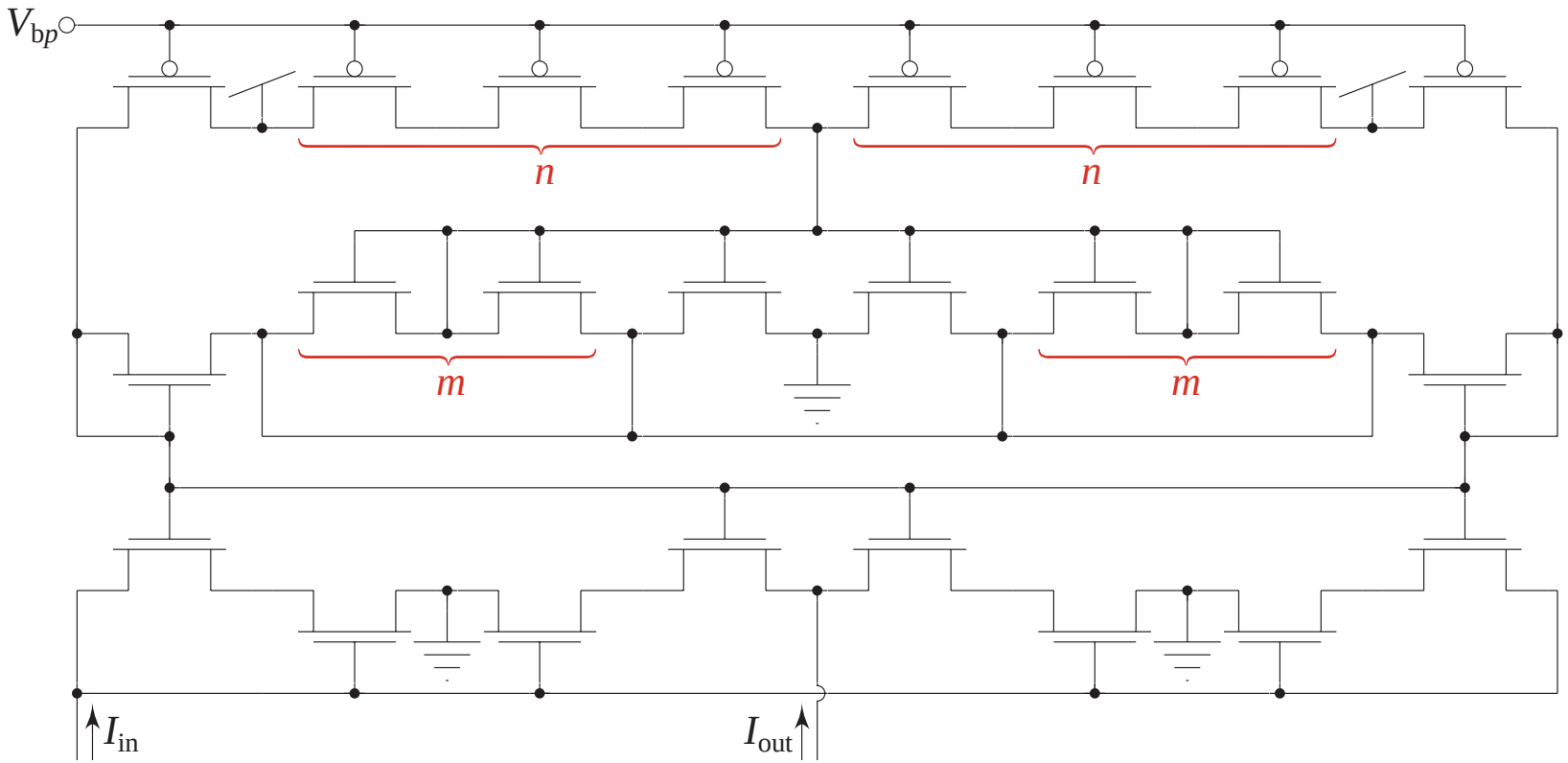
Layout-Driven Schematics



Layout-Driven Schematics



Layout-Driven Schematics



CORNELL

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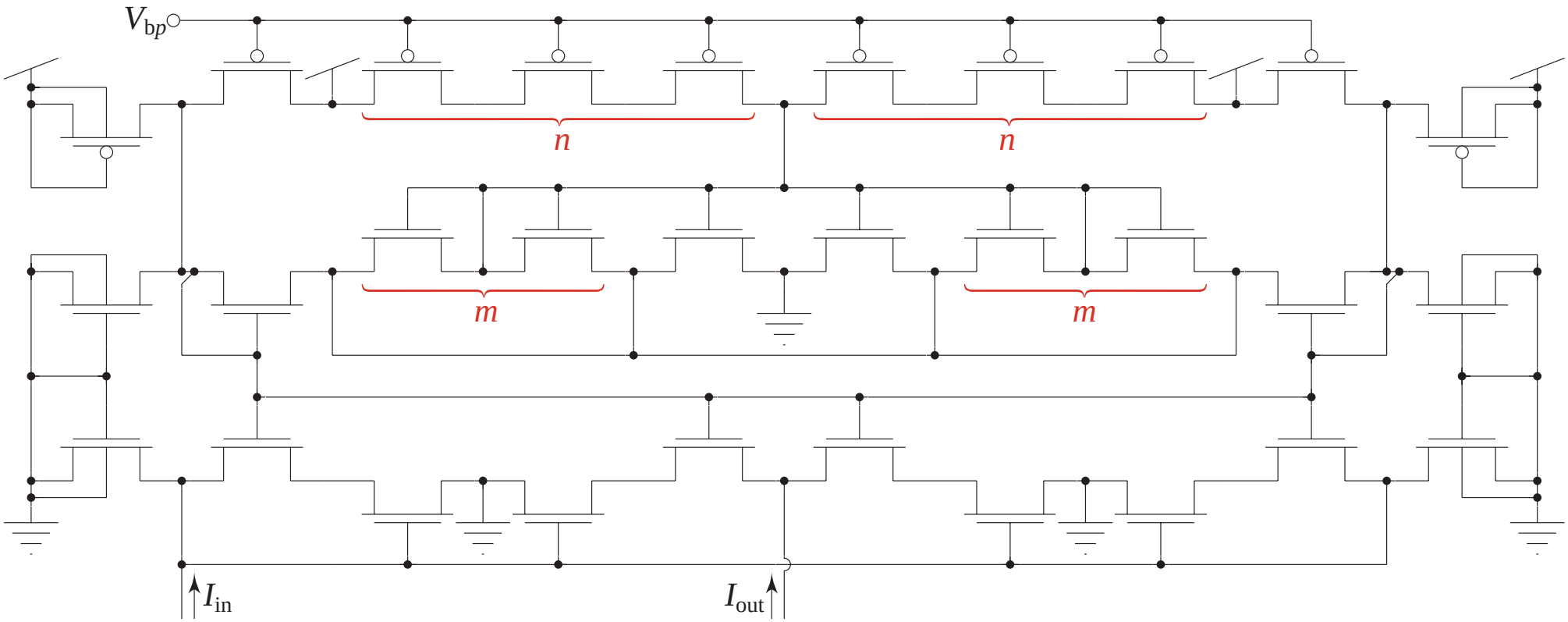
Layout-Driven Schematics



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