ENGR 3426: Machine Problem 2

due September 29, 2016

In this machine problem, you will learn about and design an edge-triggered complementary set-reset logic (CSRL) D flip-flop, which is a very elegant implementation of a basic necessity in the transistor-level design of digital circuits. You will also compose four of these into a shift register. If you find yourself in need of a D flip-flop in your project later in the semester, you should definitely consider using this one. In addition to submitting the items requested below, you will need to bundle all of your schematics, circuit symbols, and cell layouts into a zip archive or a tarball and submit these via e-mail.

1. **Schematic Capture and Simulation**. Using LTspice, design a *rising* (or *leading*) edge-triggered CRSL D flip-flop based on an appropriate sequence of transparent CRSL D latches. Construct a circuit symbol for your D flip-flop, link it to your schematic, and compose four of these into a four-bit shift register. Add input and clock voltage sources and a power supply, and perform a transient simulation showing the behavior of your shift register. You will need to submit schematics showing the simulation test harness and the transistor-level schematic of your D flip-flop as well as the plot from the transient simulation.

2. **Layout Design**. Using Glade, lay out your rising edge-triggerd CRSL D flip-flop in such a way that it can be connected into a shift register by simply abutting the cells. The clock signal and the power and ground rails should be routed horizontally in a metal layer. The input should come into the cell from the left and propagate to the right. You should try to make your cell fit into as tight a pitch as you reasonably can (i.e., it should be tall and skinny), so that you can fit as many bits worth of a shift register in as narrow a width as possible. Array four of these cells in a higher-level cell to create a four-bit shift register. Your cells must pass DRC. Your score on this part of the assignment will depend in part on the width of your four-bit shift register. You must report the overall width of the bounding box of your shift register. You will also need to submit a picture showing your flip-flop cell layout as well as your four-bit shift register layout.

3. **Layout Versus Schematic**. Extract netlists of your four-bit shift register from both the schematic and the layout and use Gemini to compare the two netlists. If they are not equivalent, you will need to find and rectify any differences. You will need to submit the LVS output showing that the two netlists match.