ENGR 3426: Machine Problem 1

due September 15, 2016

In this machine problem, you will perform many of the tasks that your final project will involve on a very simple circuit (i.e., a two-input CMOS AND gate) in an effort to learn how to use the CAD tools that you will be using this semester.

1. **Schematic Capture and Simulation**. Using LTspice, make a an appropriate symbol for a CMOS inverter and link it to a transistor-level schematic. Likewise, make an appropriate symbol for a two-input NAND gate and link it to a transistor-level schematic of the appropriate complementary CMOS gate. From your symbols, make a two-input AND gate. Load the output of the circuit with a 200-fF capacitor, add appropriate input voltage sources and a power supply, and perform a transient simulation showing the behavior of your AND gate as the inputs cycle through all possible input combinations. You will need to submit schematics showing the simulation test harness and both subcircuits as well as the plot from the transient simulation.

2. **Layout Design**. Using Glade, lay out a CMOS inverter in one cell and a two-input NAND gate in another cell. Instance these cells within a thrird cell to make a two-input AND gate. You should design your NAND gate and CMOS inverter subcells so that they fit together nicely (e.g., the power and ground rails fit together by abutting the cells). The layout must be free of design rule violations, there must be appropriate substrate and well contacts, and the AND gate's inputs and output should be available at the boundary of the top-level cell in metal. You will need to submit a picture showing your top-level cell layout.

3. **Layout Versus Schematic**. Using LTspice, create a netlist of your two-input AND gate for LVS. Using Glade, extract your top-level cell layout. Compare the two netlists using the LVS dialog in Glade. If they are not equivalent, you will need to find and rectify any differences. You will need to submit the LVS output showing that the two netlists match.