ENGR 3426: Mixed Analog-Digital VLSI I

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Instructor: Bradley A. Minch

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Office Hours: Upon request E-mail: bradley.minch@olin.edu

Class Meetings: MR 1:30–3:10 PM, AC 304

Credits: 4 ENGR

Hours: 4–4–4

Prerequisites: ENGR 2420 or permission of instructor

Course Description:

This course will provide an overview of mixed-signal (analog and digital) integrated circuit design in complimentary metal-oxide (CMOS) technologies. Students will learn transistor-level design of digital and analog circuits, layout techniques for digital and analog circuit modules, and special physical considerations that arise in a mixed-signal integrated circuit. Students will design a custom mixed-signal integrated circuit that will be sent out for fabrication (subject to the approval of MOSIS funding) at the end of the semester if they commit to testing their chips when they come back.

Course Web Page: madvlsi.olin.edu/madvlsi

Grades: 40% Machine Problems, 60% Project.

To determine your course grade, I will compute a weighted average of all of your machine problem and project scores. If your weighted average is 90% or higher, you will receive at least an A–. If your weighted average is 80% or higher, you will receive at least a B–. If your weighted average is 70% or higher, you will receive at least a C–. I may adjust the boundaries between letter grades down, depending on the distribution of overall weighted averages. No individual assignments will be curved.

Learning Objectives: At the end of this course, students will:

- Understand and design using various combinational and sequential CMOS logic styles.
- Understand and apply the principles of designing robust analog integrated circuits.
- Understand the special issues and trade-offs that arise in the design of mixed-signal integrated circuits and how these may be addressed.
- Design a mixed-signal integrated circuit of moderate complexity using computer-aided design tools.

Text:

There is no required textbook for this course. Neither is there an optional text. If you would like a text to consult as a reference to complement the course materials, you might consider one of the suggested books listed on the course web page. Our approach to the course material will be sufficiently different from that taken in these books that none of them would have been suitable for use as a course text.

Machine Problems:

During the first third of the semester, you will be working individually on several machine problems that will involve the design, layout, simulation, and verification of various anlog, digital, and mixed-signal integrated circuit modules. In the process, you will become familiar with the tools and process typically employed in the design of custom integrated circuits. You will be required to submit a report and your design files for each machine problem.

Project:

During the last two thirds of the semester, you will be working indvidually or with one or two other students in the class on a design project that will involve the design, layout, simulation, and verification of a mixed-signal integrated circuit of modest complexity, such as a CMOS image sensor, or a data convertor. A final project report will be due at the end of the semester documenting the design of your chip. Subject to the approval of our application to the MOS Implementation Service (MOSIS) Education Program and at least one of your group members committing to test your chip, we will send your designs out for fabrication during winter break through MOSIS.

Course Policies:

Collaboration. You are free to discuss the machine problems with other students in the class, but when it comes time to do the work, you should work alone. You may not simply sit next to a classmate, looking over their shoulder at the computer screen and turn in a copy of their design files or simulation results. You should have a sufficient understanding of everything that you turn in that you could explain it to someone else (e.g, me) and answer his or her questions about it without consulting anyone else.

Late Assignments. Machine problem and project reports will be on the announced dates and times. These reports can be handwritten neatly or typeset. Late reports will be penalized at a rate of up to 5% per day or fraction thereof.