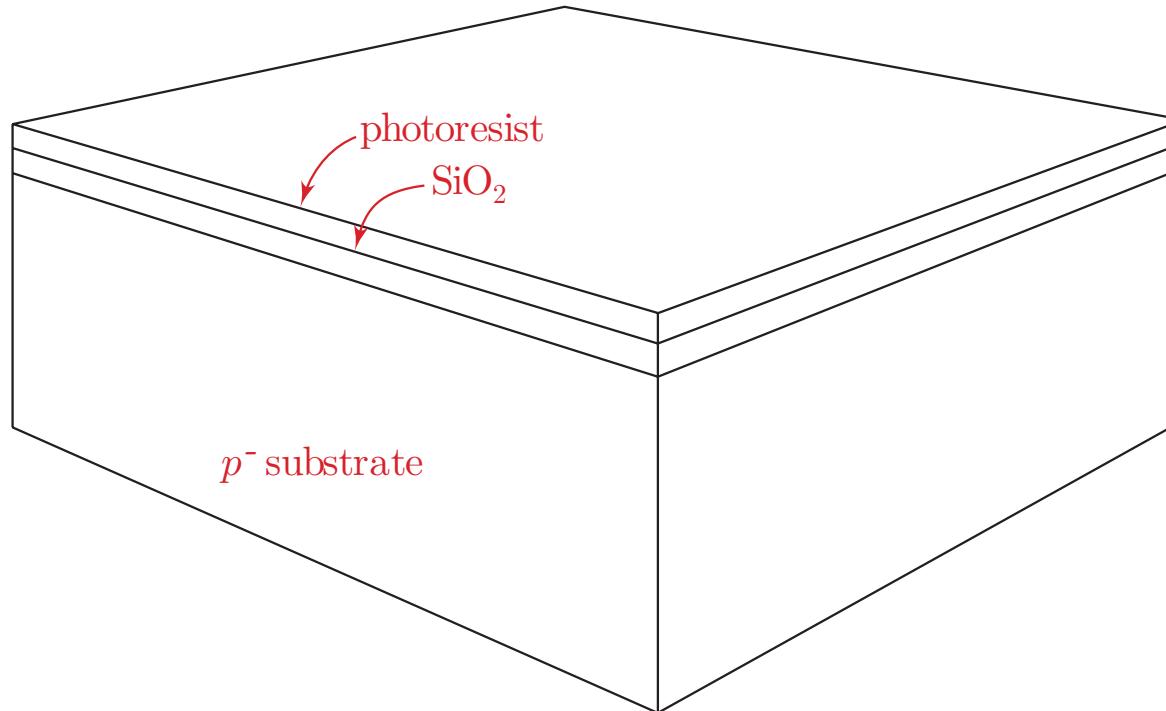


CMOS Fabrication

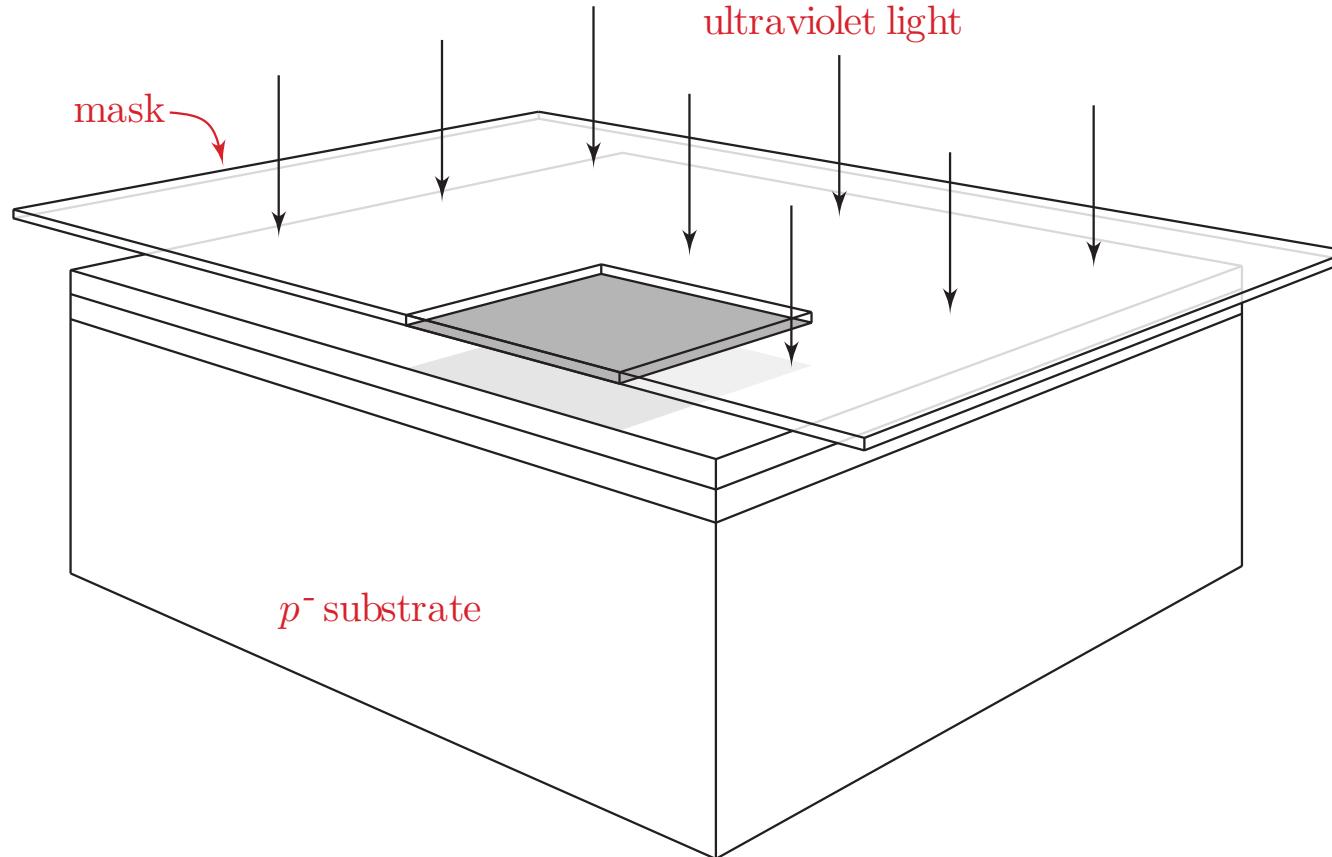


Oxidize silicon surface and coat with photoresist

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CMOS Fabrication

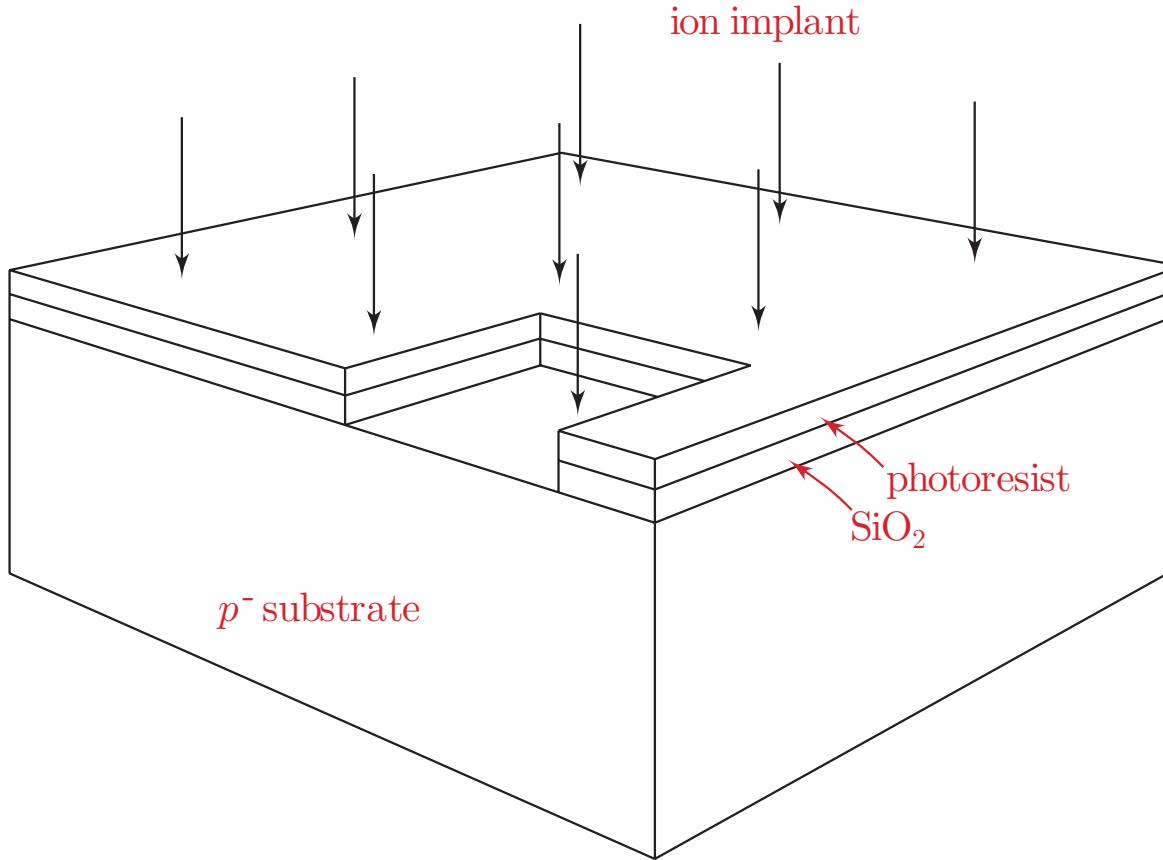


Pattern and selectively etch oxide layer

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CMOS Fabrication

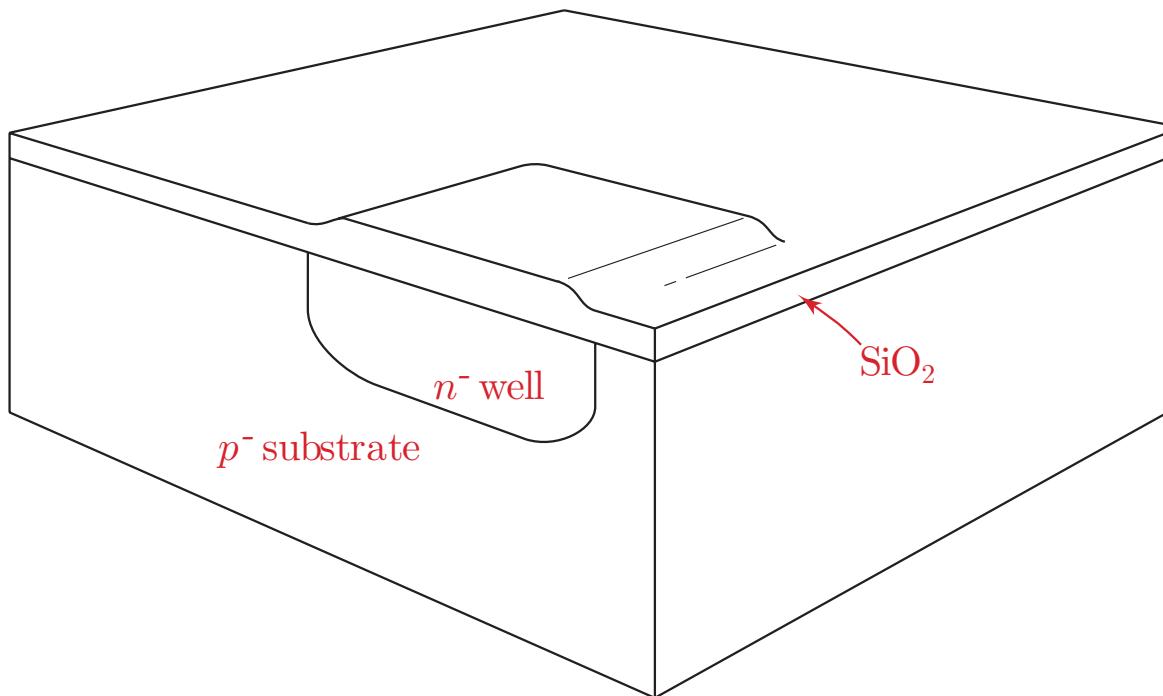


Ion implant for n -well regions

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CMOS Fabrication

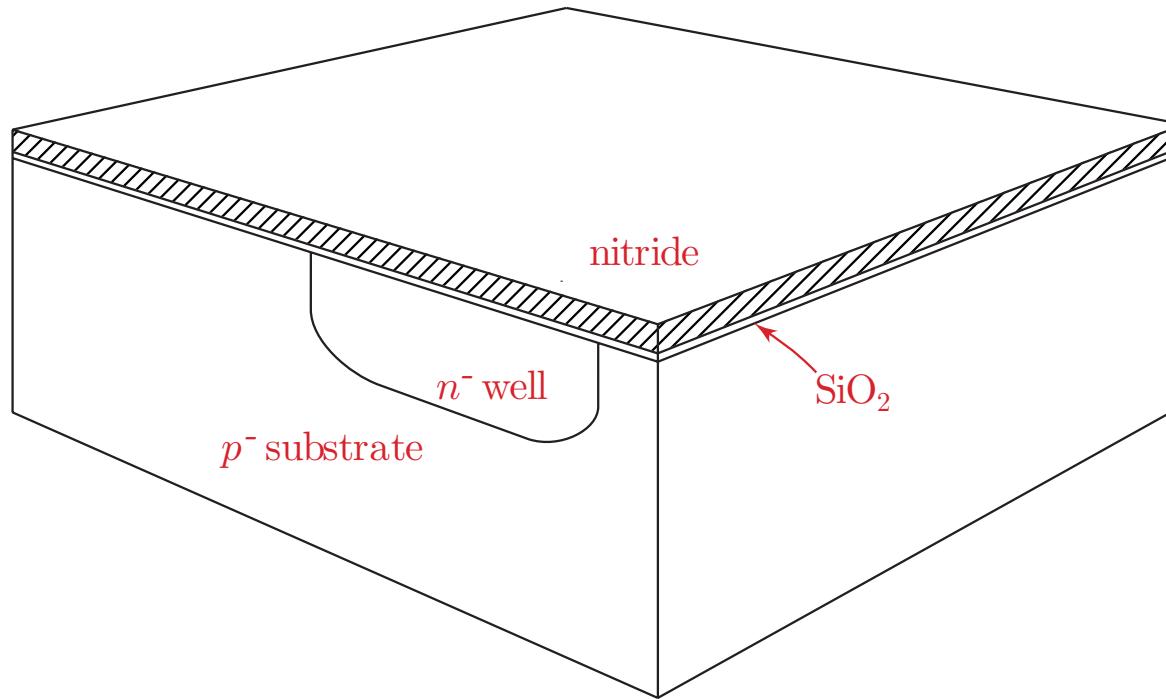


Anneal n -well implant and grow oxide

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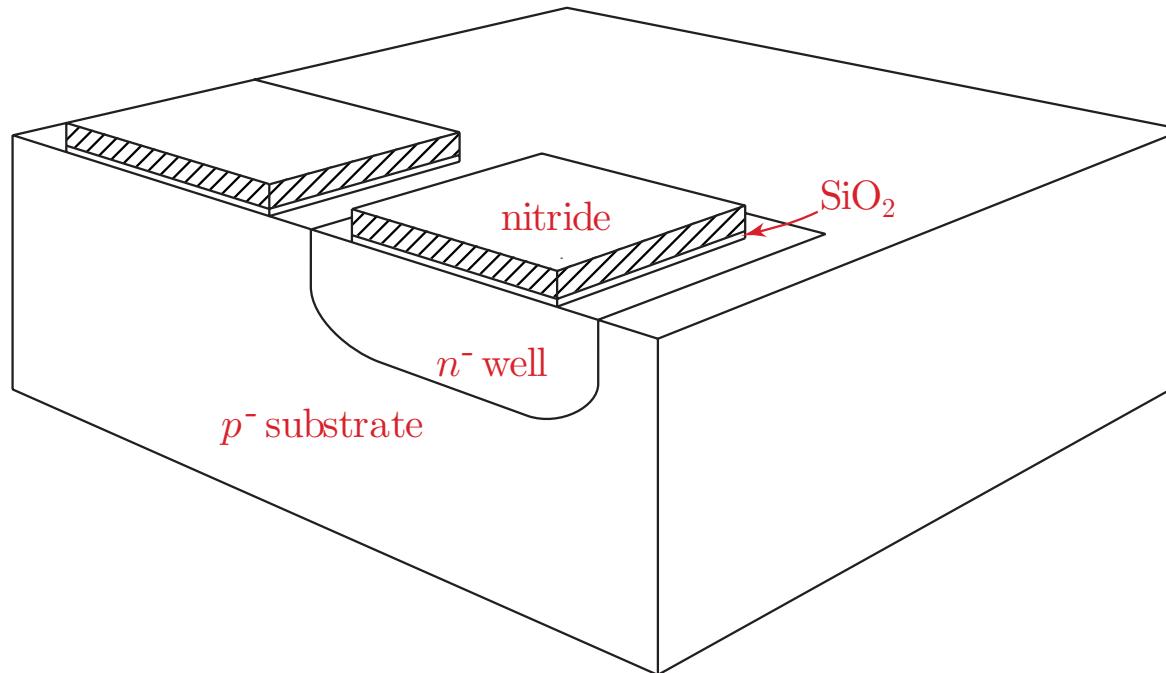
CMOS Fabrication



Remove all oxide, regrow thin oxide, and deposit nitride layer

CORNELL

CMOS Fabrication

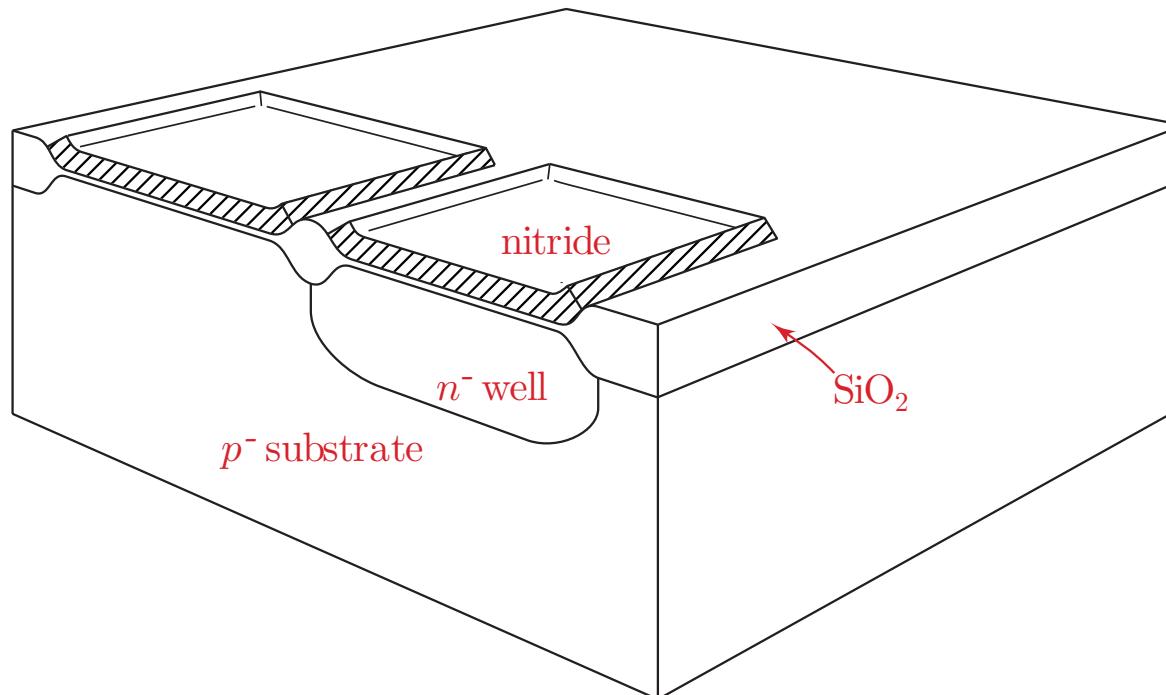


Pattern and selectively etch oxide and nitride layers

CORNELL

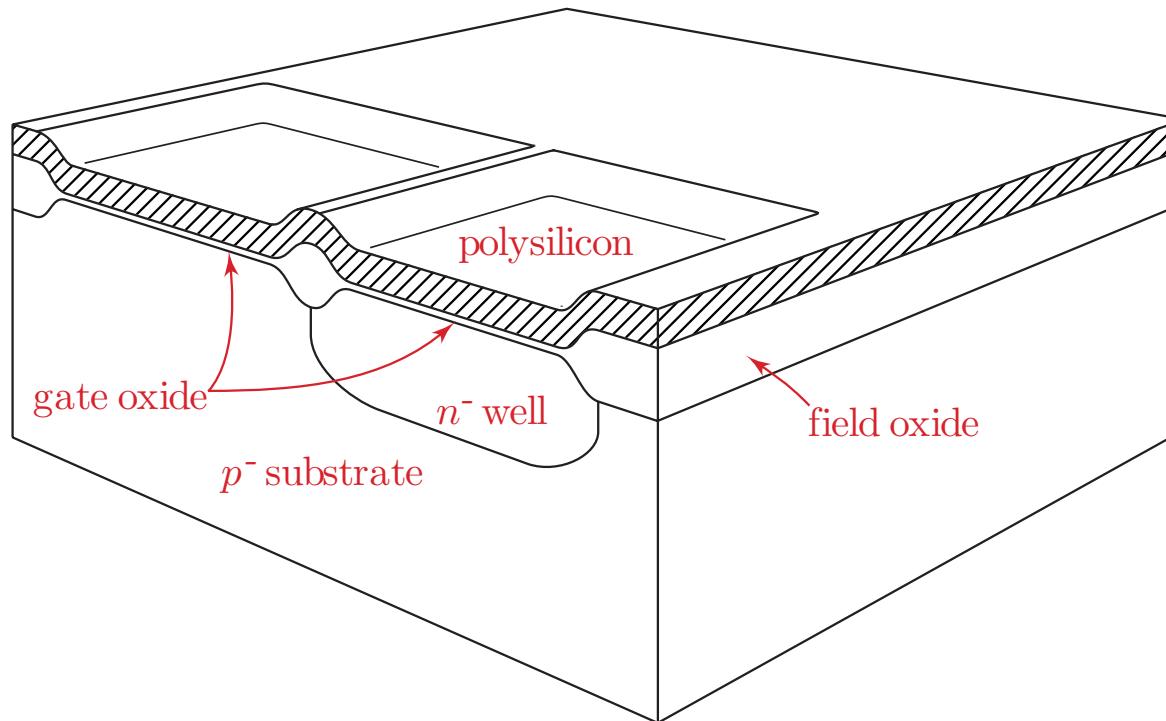
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Grow field oxide in areas without nitride

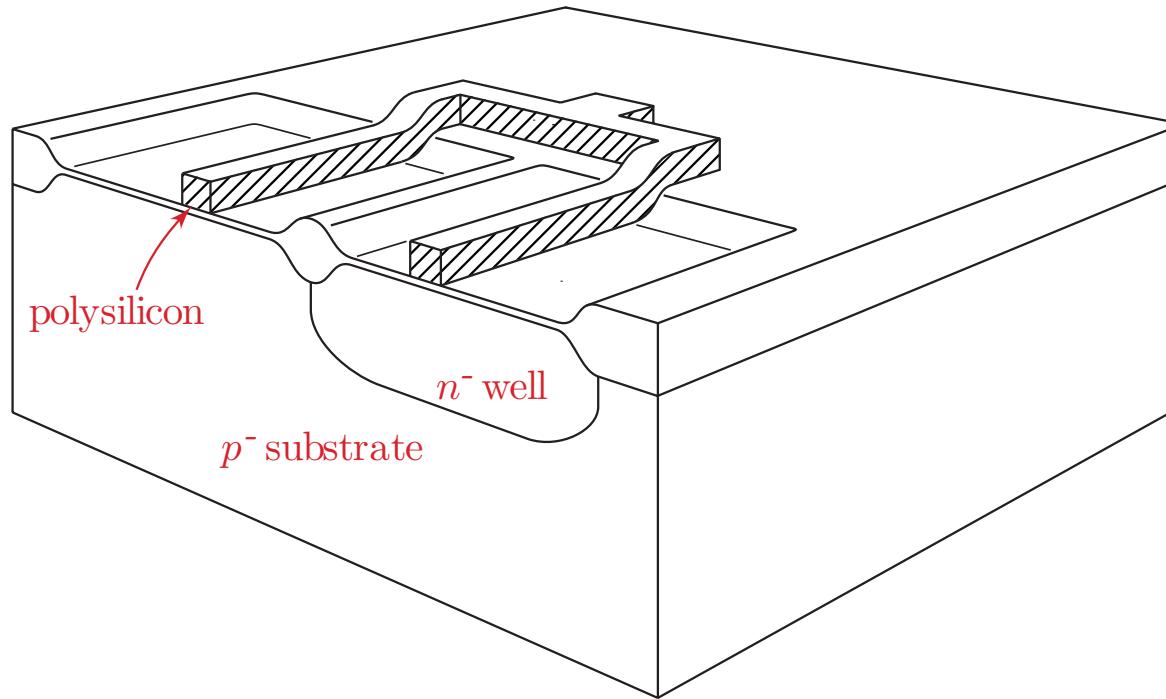
CMOS Fabrication



Remove nitride and thin oxide, grow gate oxide, and deposit poly

CORNELL

CMOS Fabrication

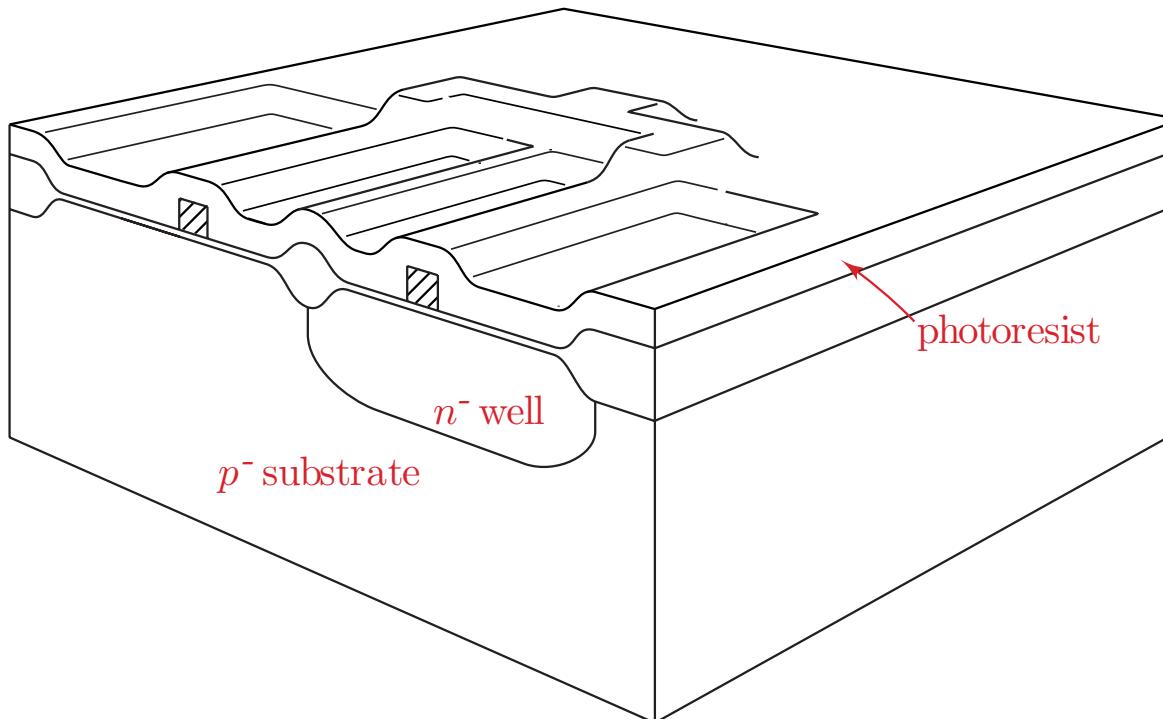


Pattern and selectively etch polysilicon

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CMOS Fabrication

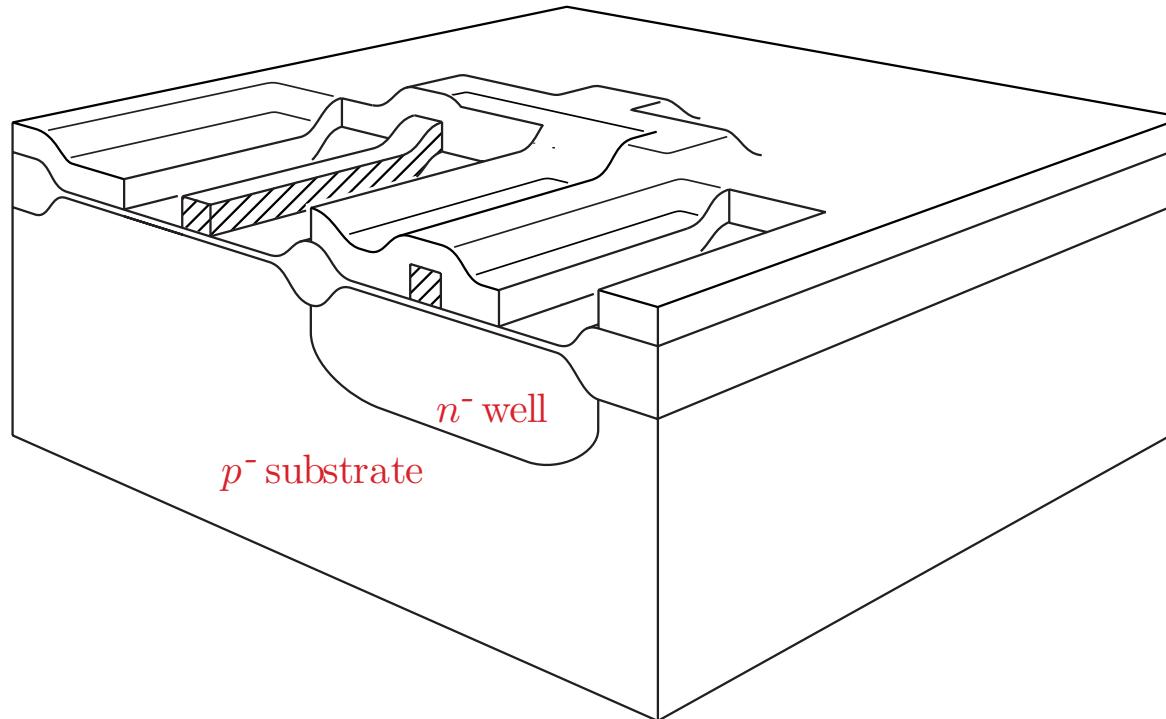


Conformally coat entire surface with photoresist

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CIRCUITS & SYSTEMS LAB

CMOS Fabrication

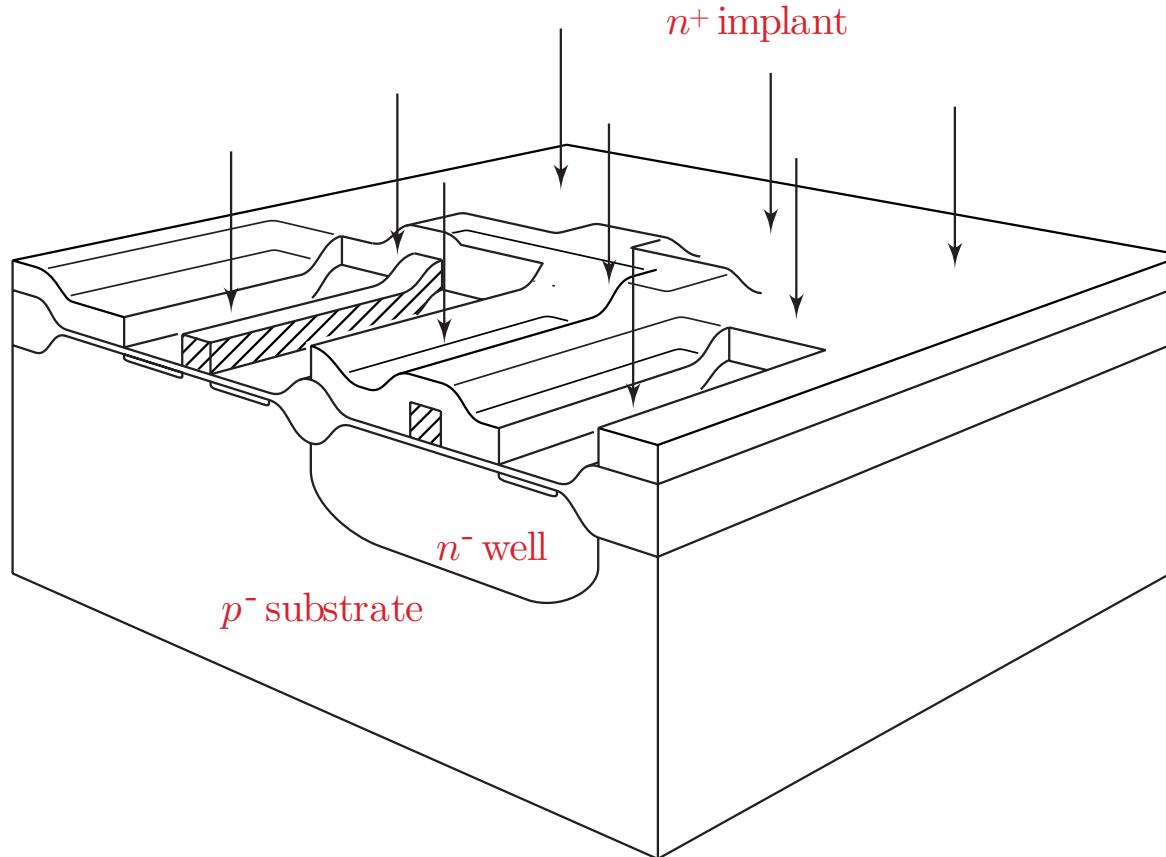


Remove photoresist to expose regions for n^+ implant

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CIRCUITS & SYSTEMS LAB

CMOS Fabrication

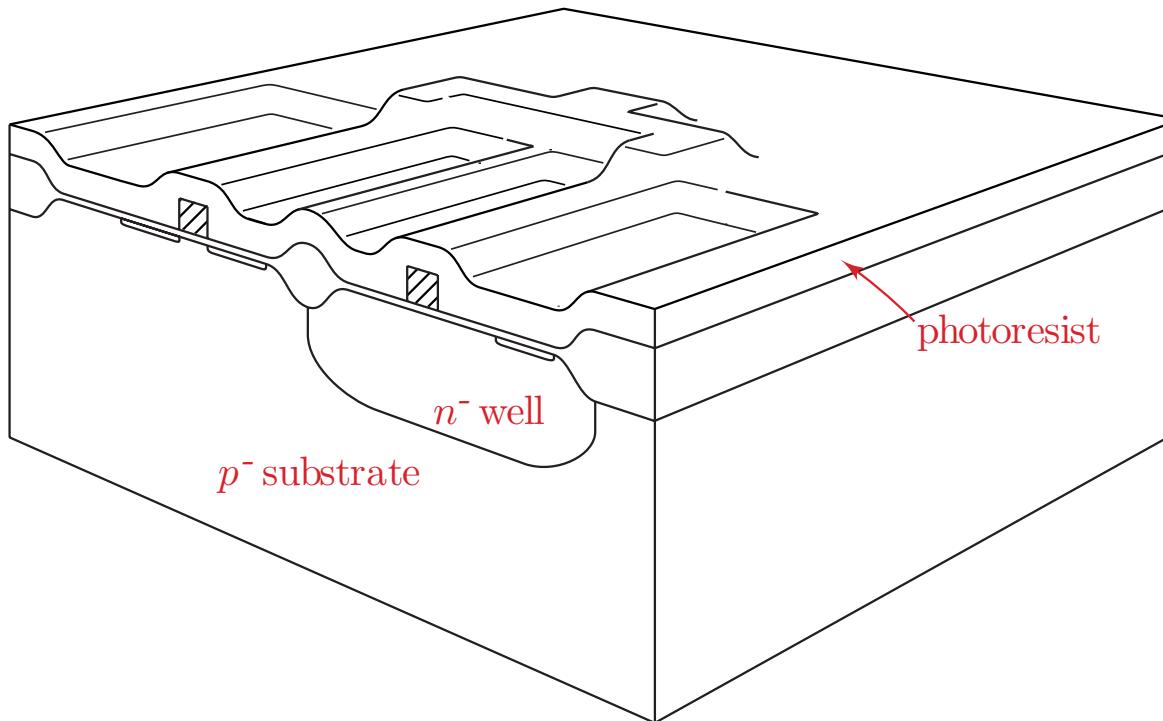


Ion implant for n^+ regions and remove all photoresist

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MAD VLSI
CIRCUITS & SYSTEMS LAB

CMOS Fabrication

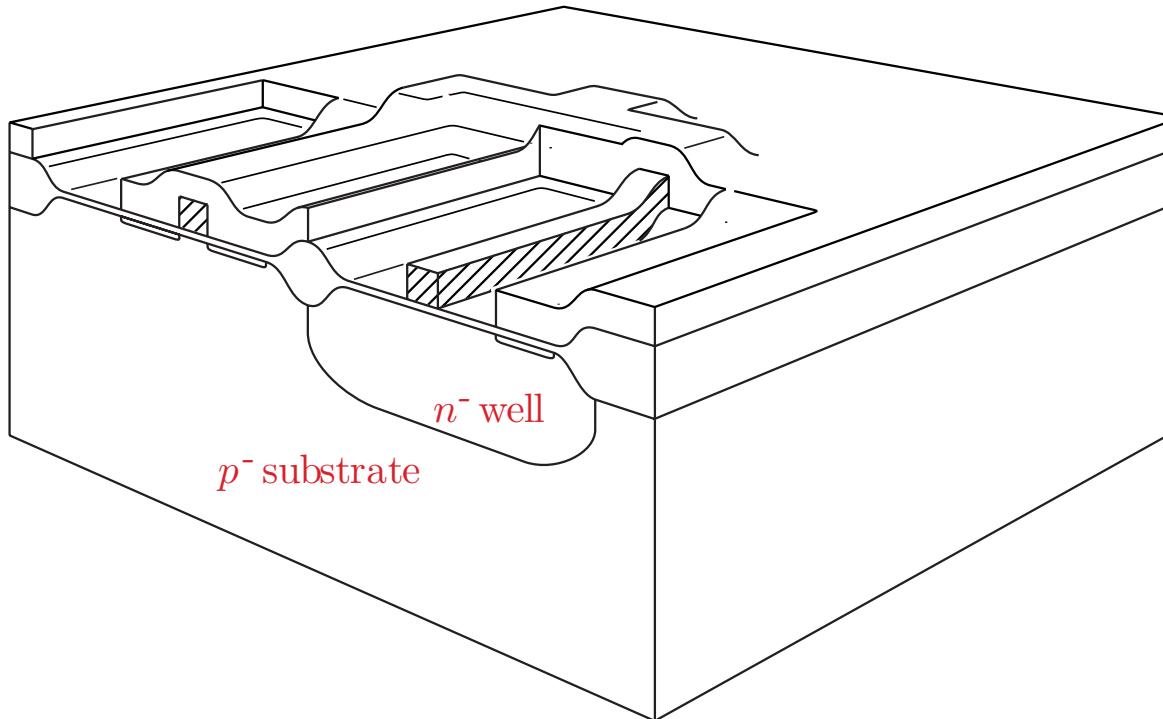


Conformally coat entire surface with photoresist

CORNELL

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CMOS Fabrication

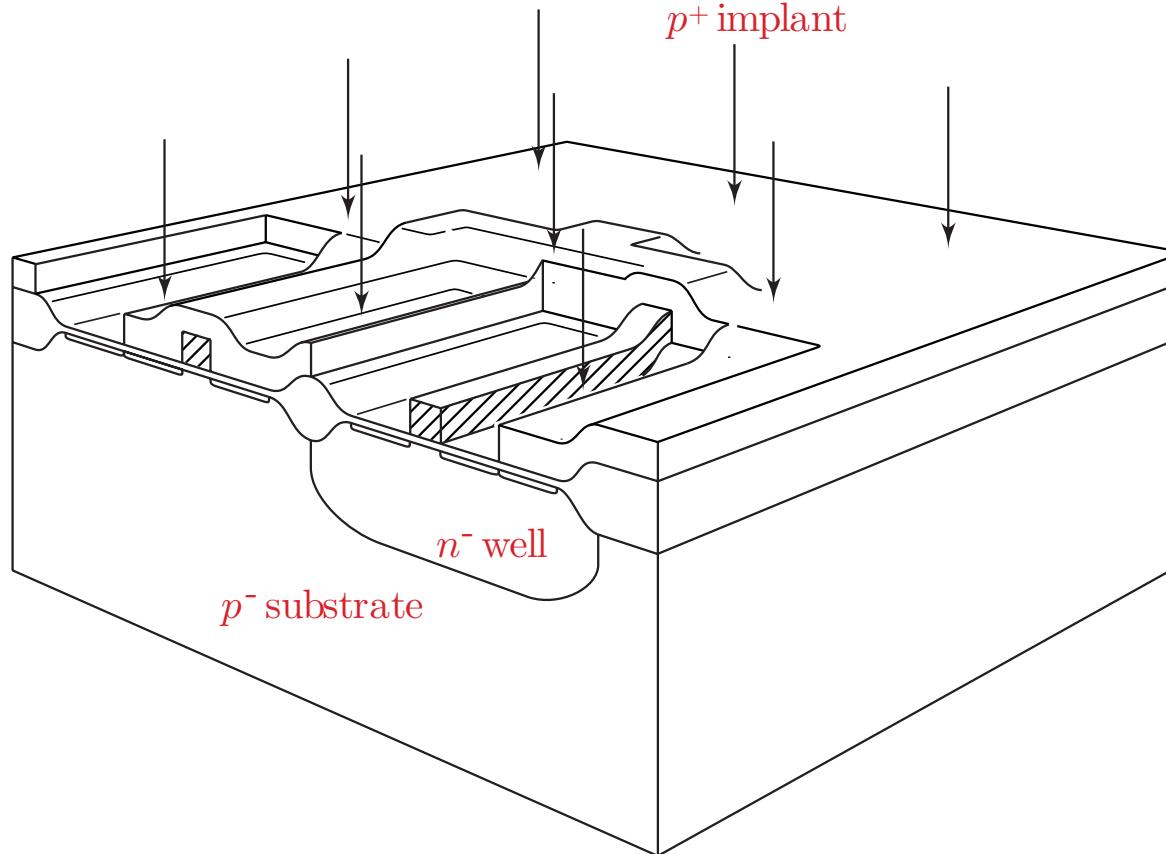


Remove photoresist to expose regions for p^+ implant

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CMOS Fabrication

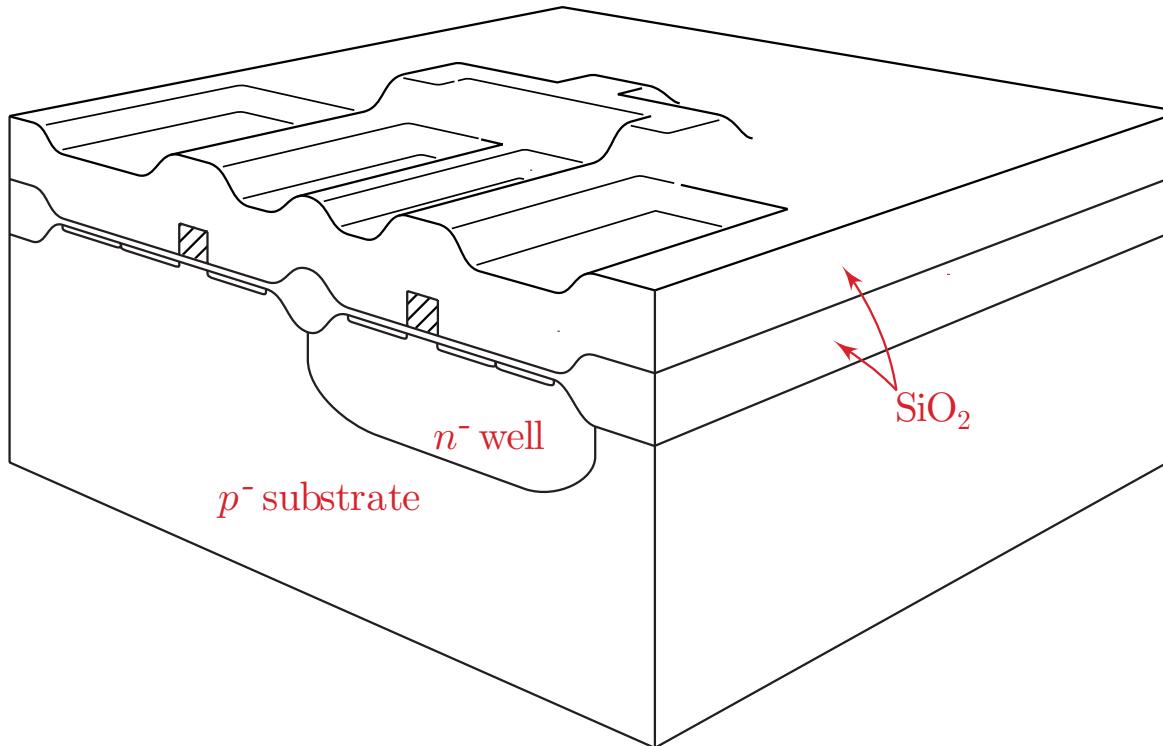


Ion implant for p^+ regions and remove all photoresist

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MAD VLSI
CIRCUITS & SYSTEMS LAB

CMOS Fabrication

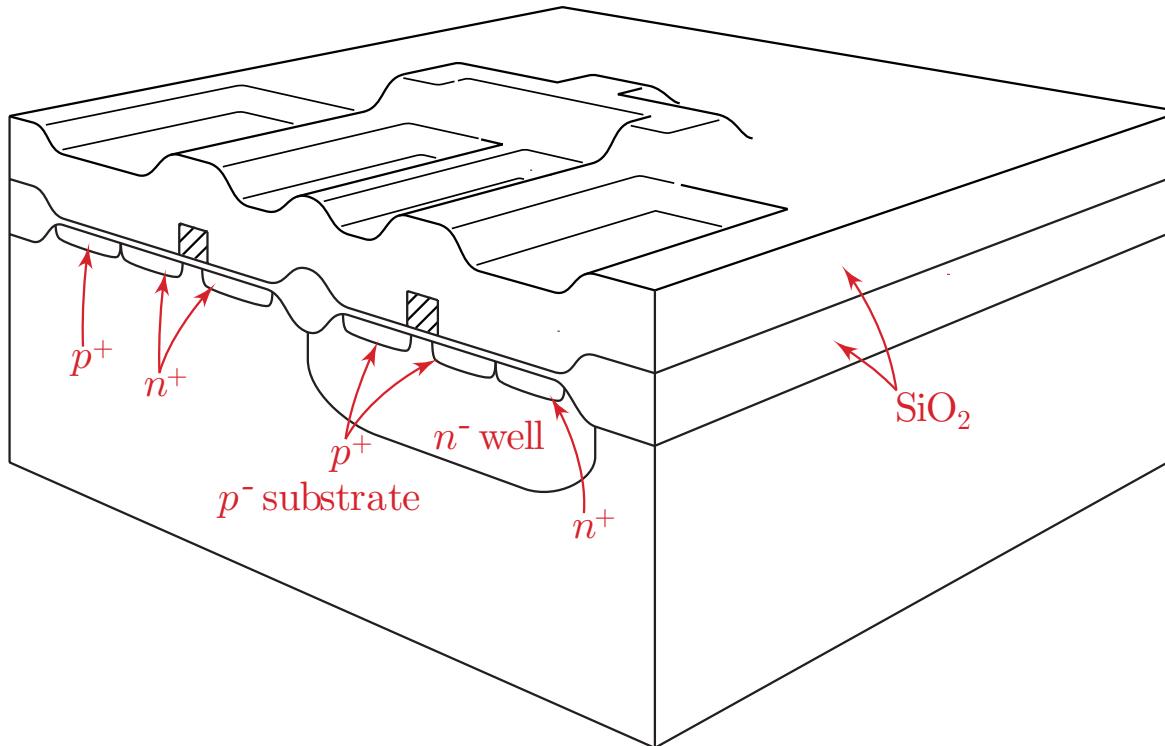


Deposit thick oxide layer over entire surface

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CMOS Fabrication

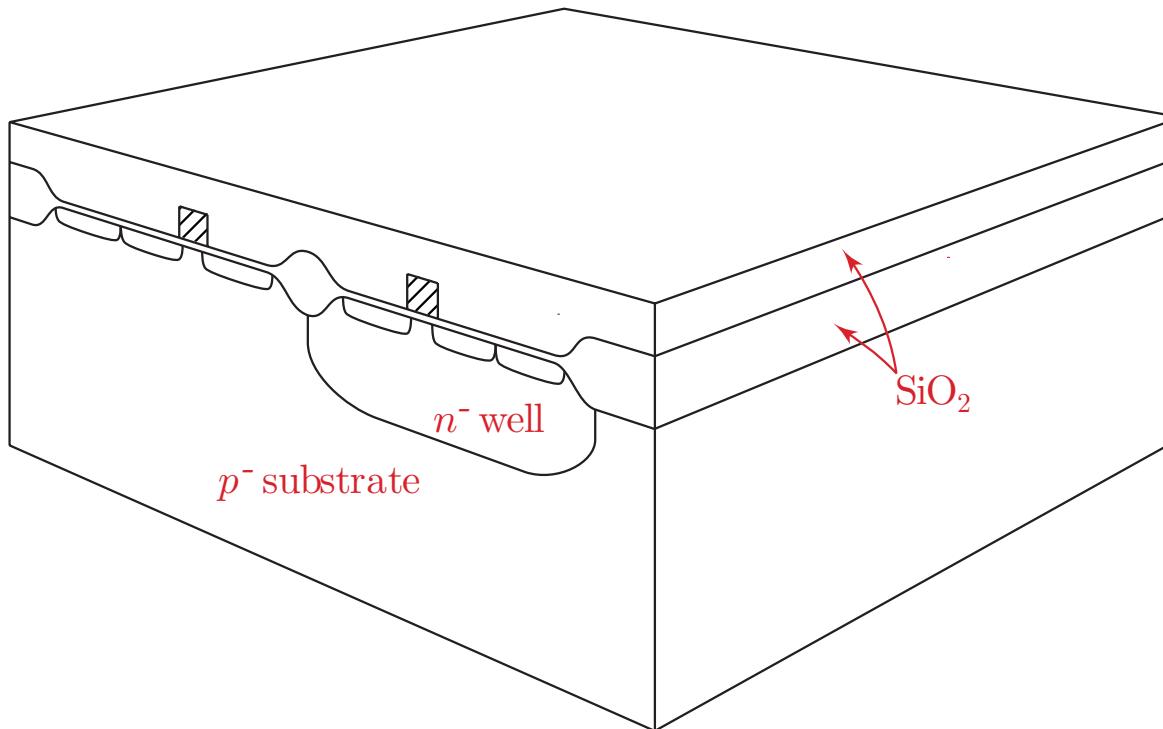


Anneal and drive in both implants

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CMOS Fabrication

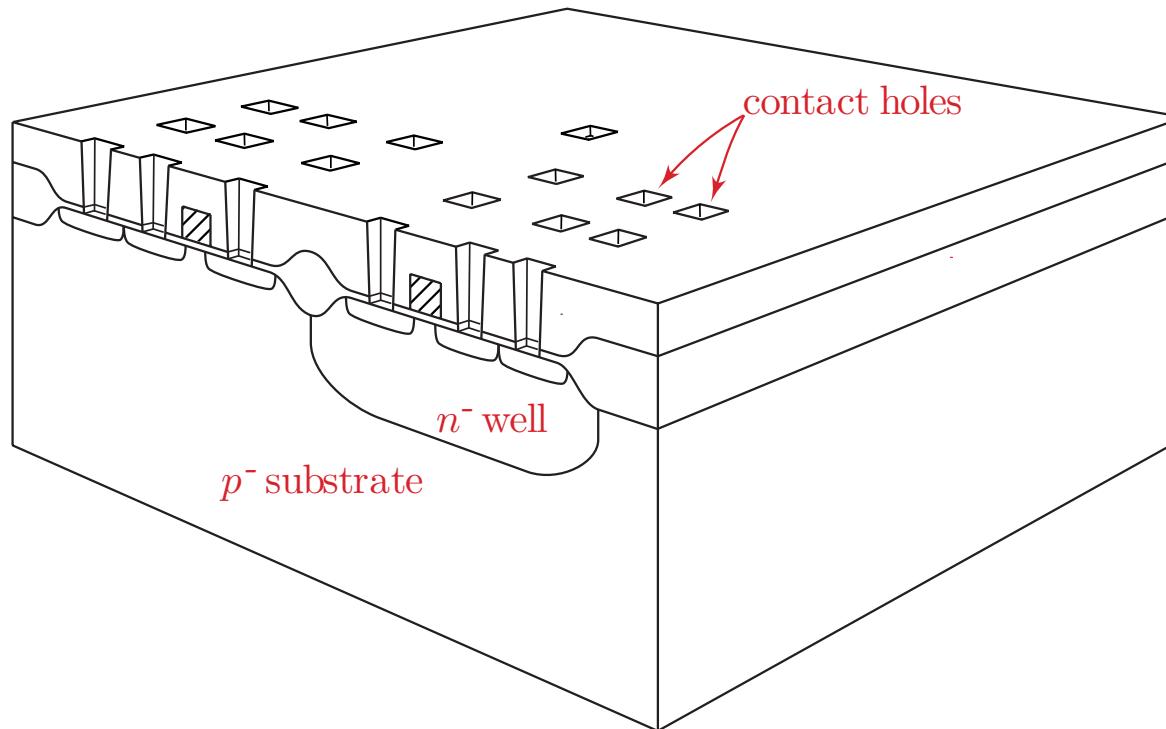


Planarize surface by chemical-mechanical polishing

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CMOS Fabrication

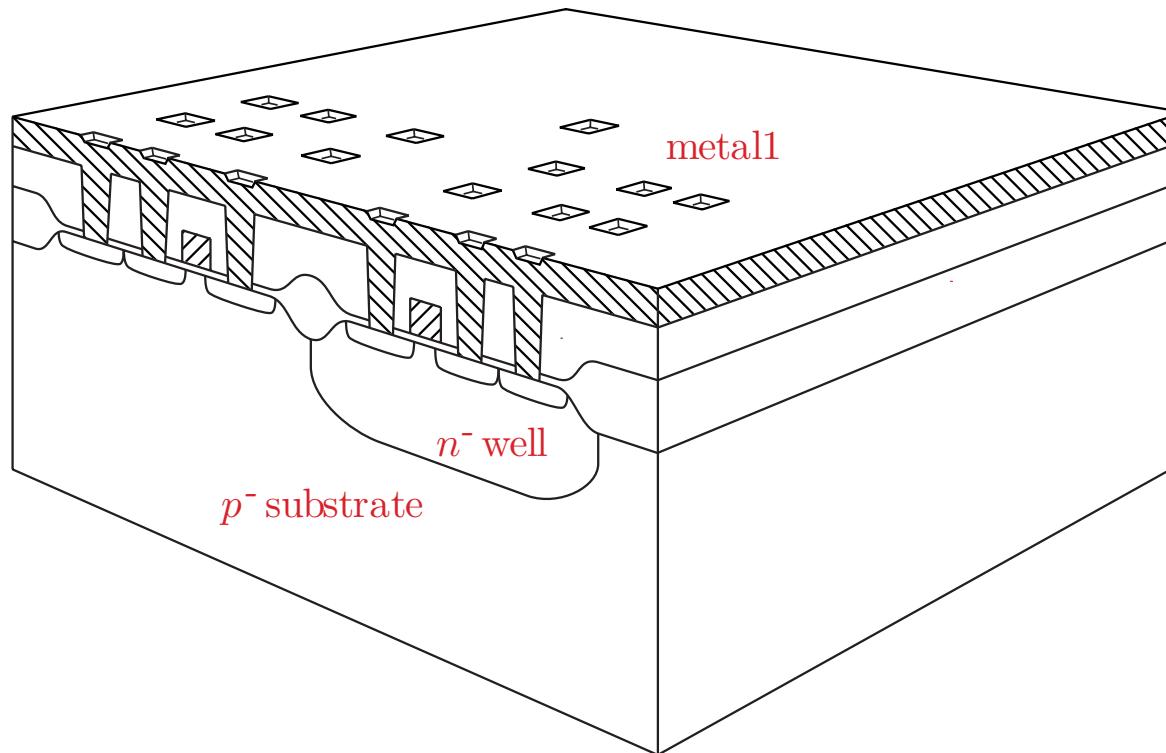


Open contact windows in the oxide

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CMOS Fabrication

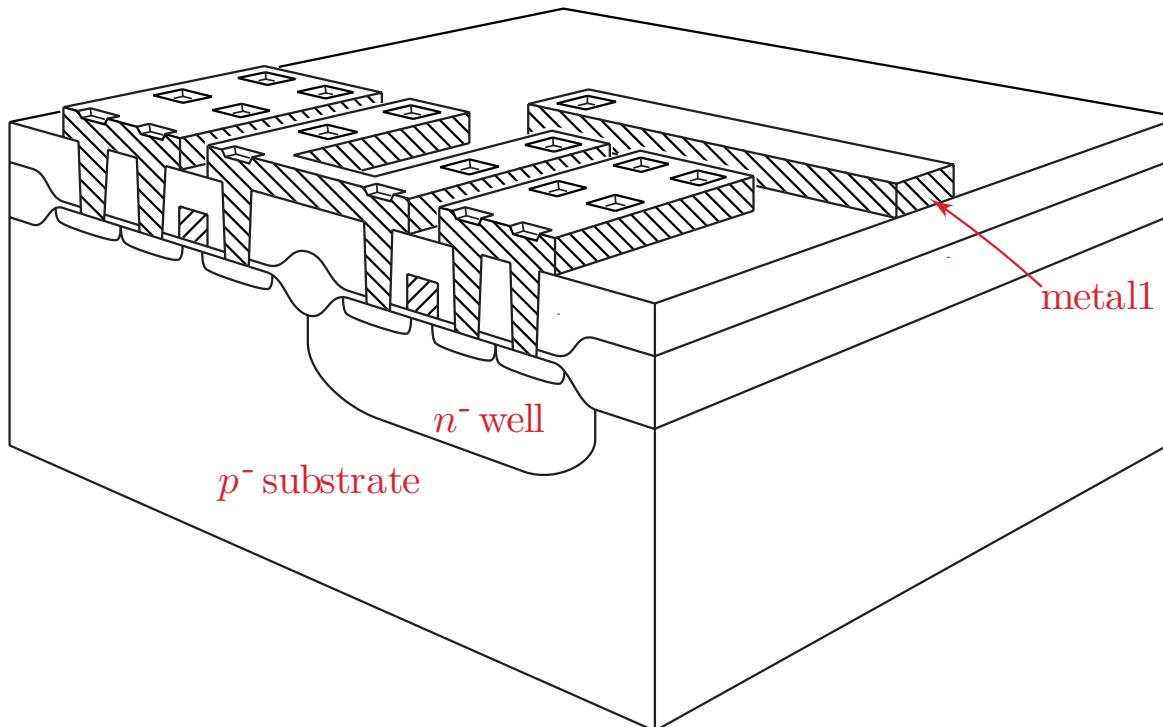


Fill contact holes with metal and deposit metall1

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CIRCUITS & SYSTEMS LAB

CMOS Fabrication

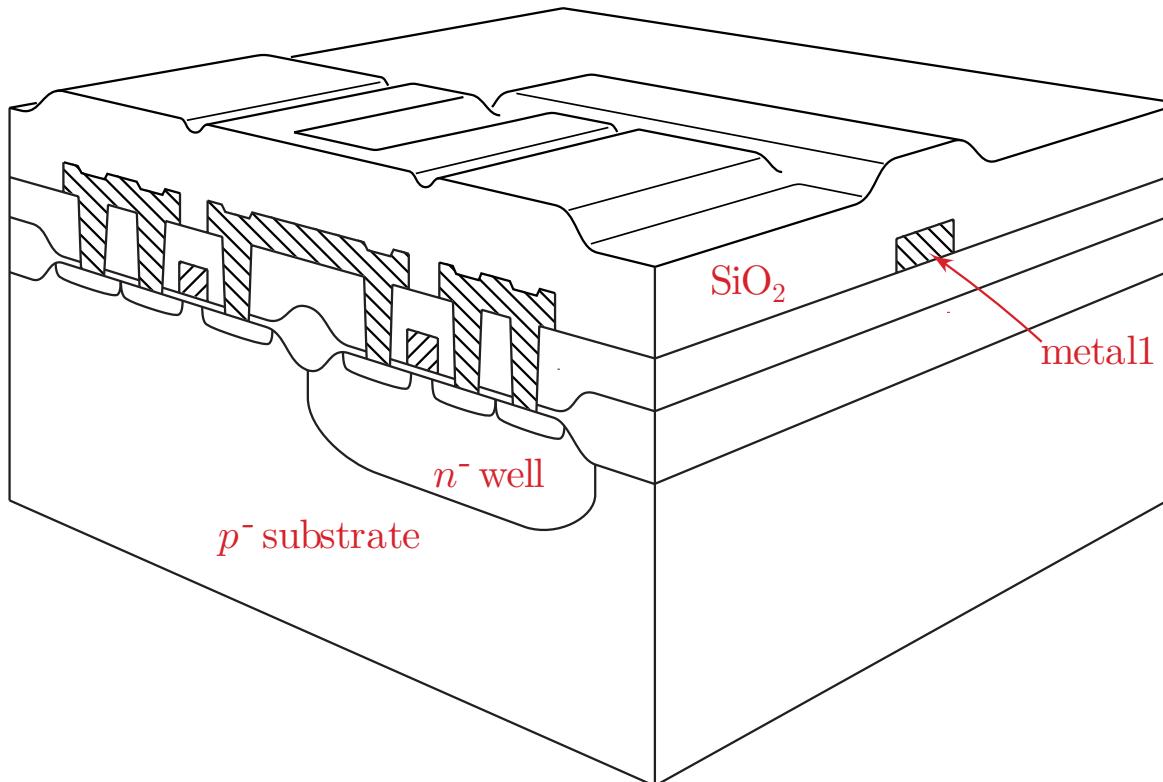


Pattern and selectively etch metall1

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CIRCUITS & SYSTEMS LAB

CMOS Fabrication

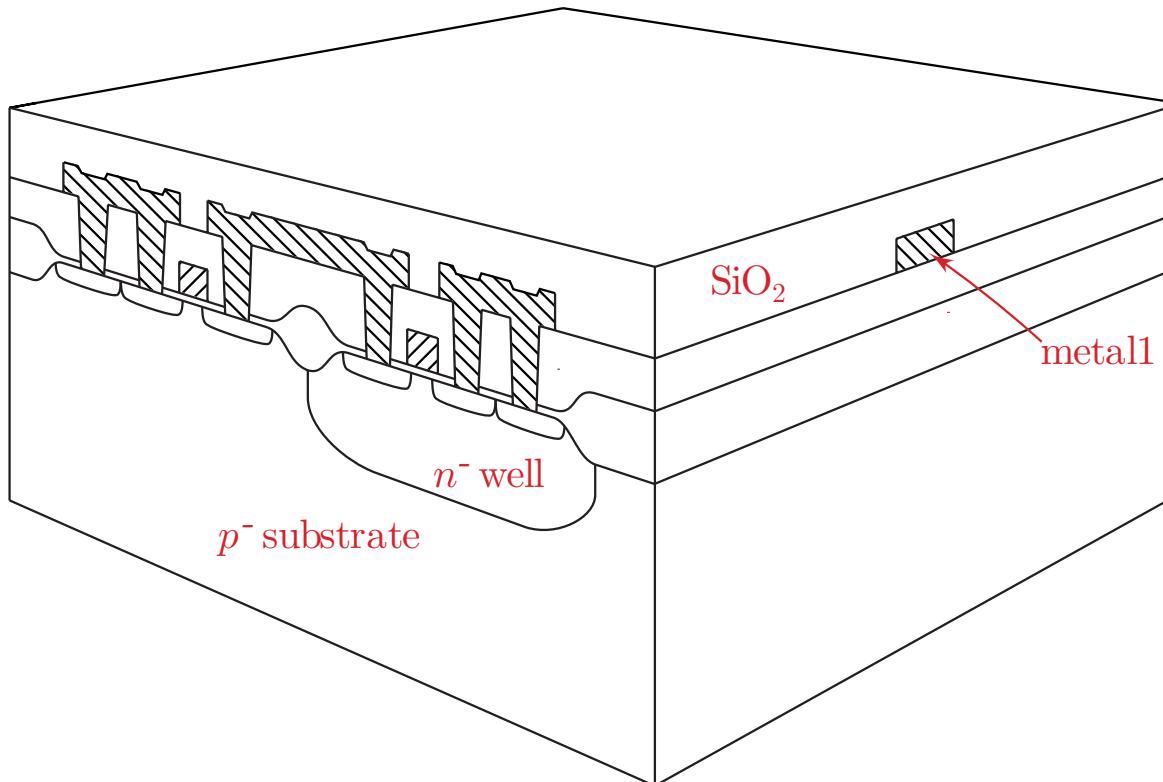


Deposit thick oxide layer over entire surface

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CIRCUITS & SYSTEMS LAB

CMOS Fabrication

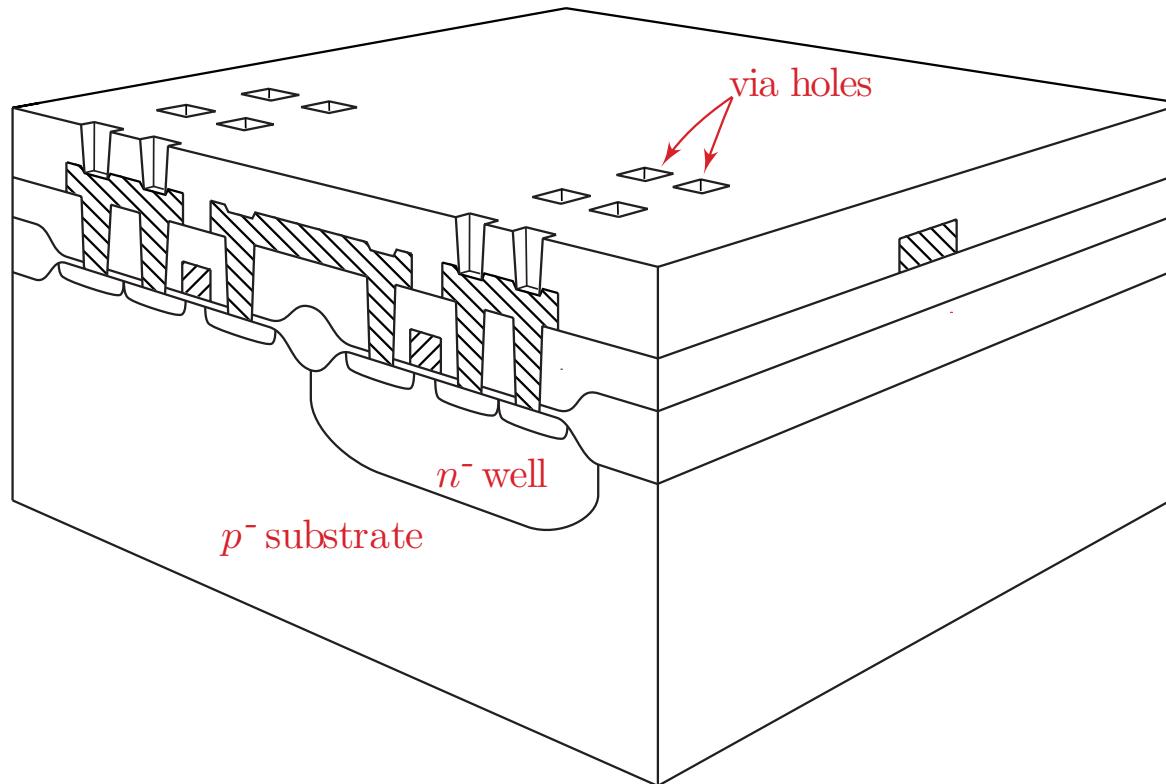


Planarize surface by chemical-mechanical polishing

CORNELL

MAD VLSI
CIRCUITS & SYSTEMS LAB

CMOS Fabrication

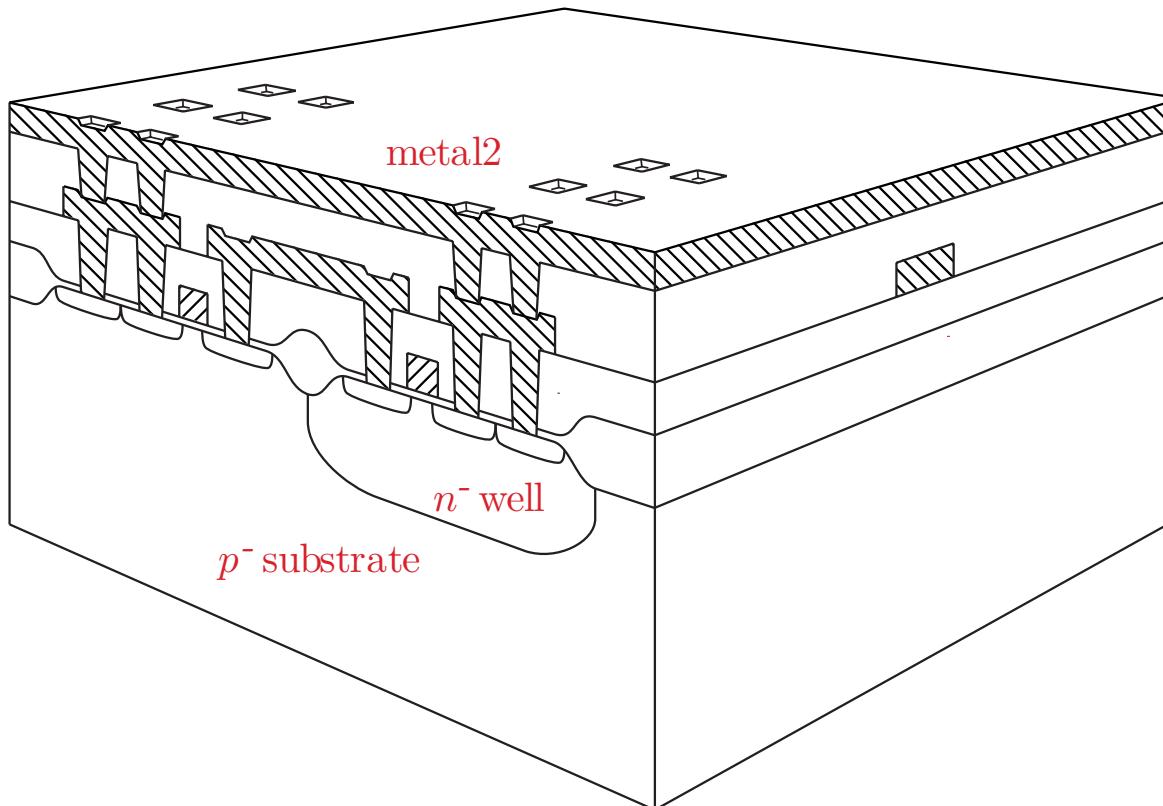


Open via windows in the oxide

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CIRCUITS & SYSTEMS LAB

CMOS Fabrication

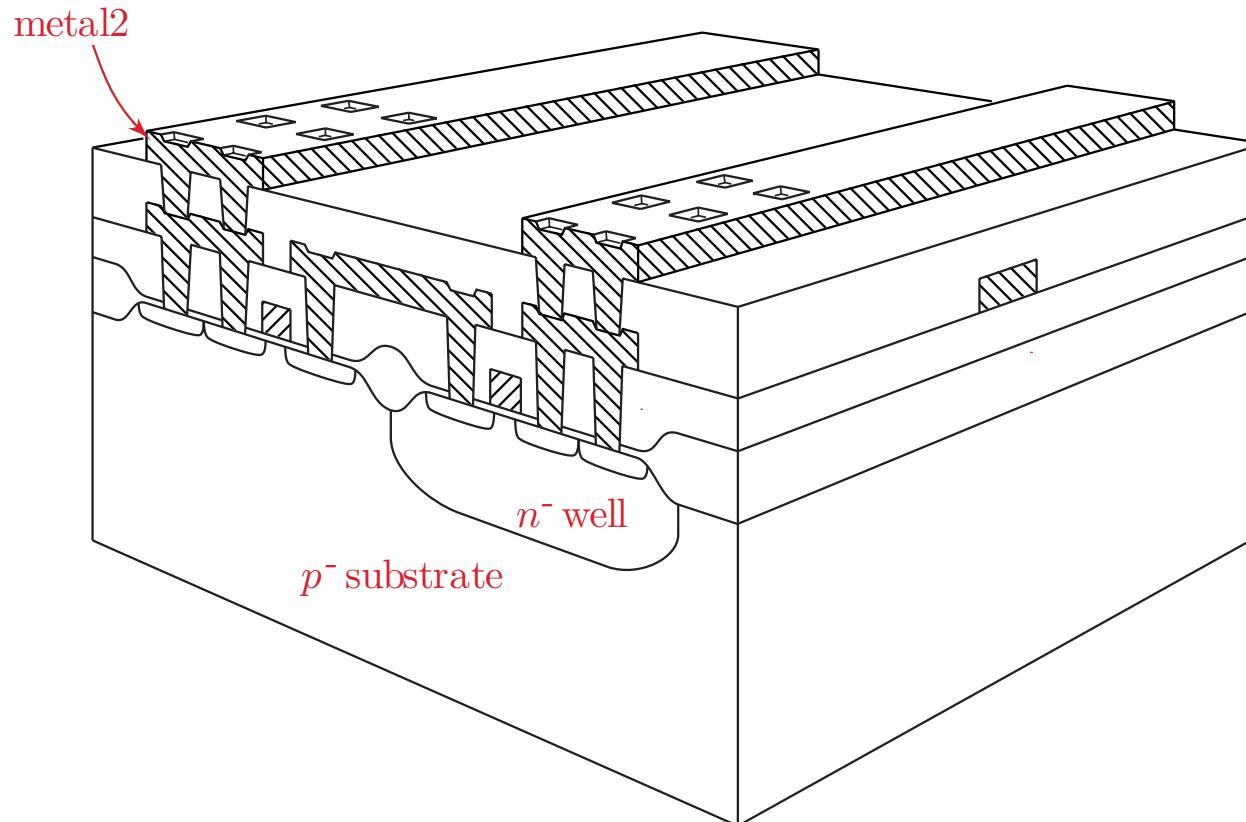


Fill via holes with metal and deposit metal2

CORNELL

MAD VLSI
CIRCUITS & SYSTEMS LAB

CMOS Fabrication

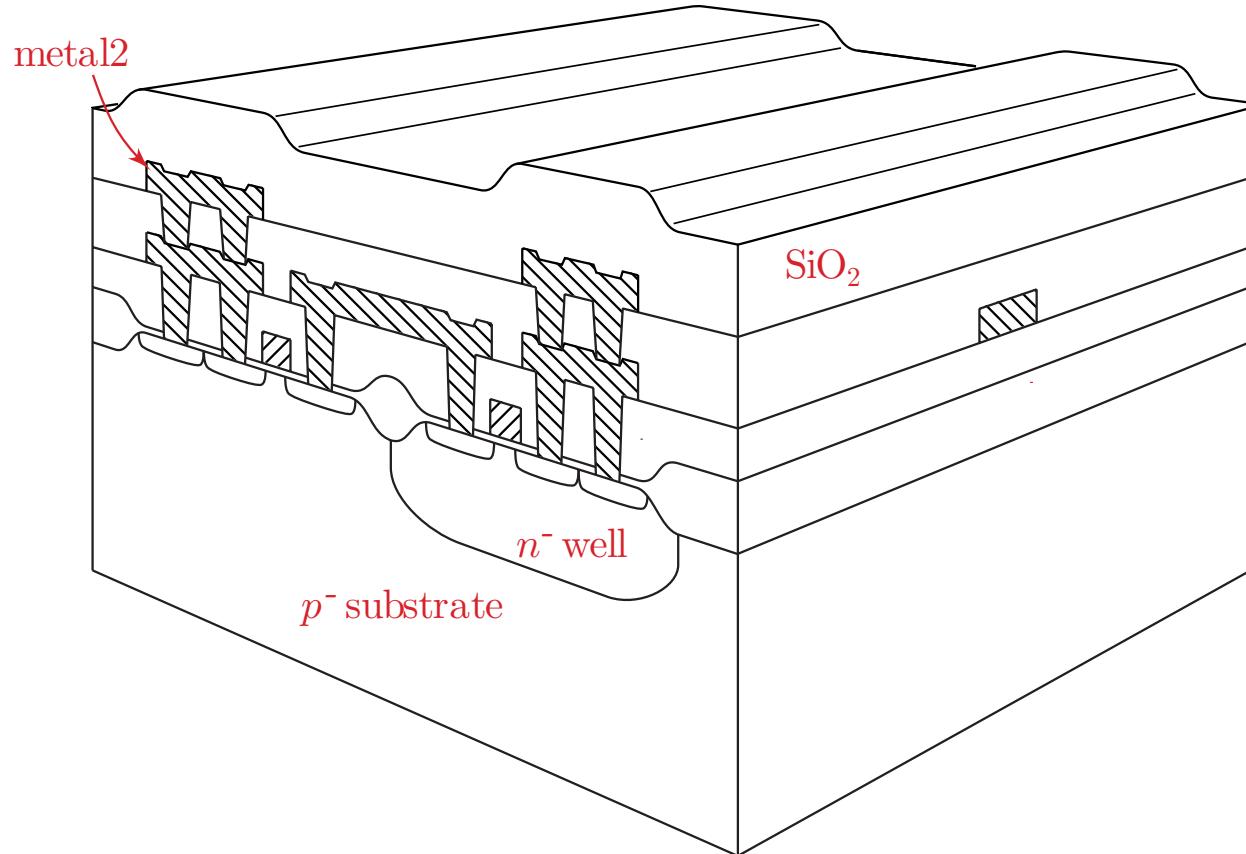


Pattern and selectively remove metal2

CORNELL

MAD VLSI
CIRCUITS & SYSTEMS LAB

CMOS Fabrication



Deposit thick oxide layer over entire surface

CORNELL

MAD VLSI
CIRCUITS & SYSTEMS LAB