



MICROCHIP

PIC18F2455/2550/4455/4550

PIC18F2455/2550/4455/4550 Rev. A3 Silicon Errata

The PIC18F2455/2550/4455/4550 parts you have received conform functionally to the Device Data Sheet (DS39632), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2455/2550/4455/4550 will be reported in a separate Data Sheet errata. Please check the Microchip Web site for any existing issues.

All of the issues listed here will be addressed in future revisions of the PIC18F2455/2550/4455/4550 silicon.

The following silicon errata apply only to PIC18F2455/2550/4455/4550 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2455	01 0010 011	00010
PIC18F2550	01 0010 010	00010
PIC18F4455	01 0010 001	00010
PIC18F4550	01 0010 000	00010

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTA register is set), an ongoing transmission's timing can be corrupted if the TX9D bit (for the next transmission) is not written immediately following the setting of TXIF. This is because any write to the TXSTA register results in a reset of the Baud Rate Generator which will effect any ongoing transmission.

Work around

Load TX9D just after TXIF is set, either by polling TXIF or by writing TX9D at the beginning of the Interrupt Service Routine, or only write to TX9D when a transmission is not in progress (TRMT = 1).

2. Module: Timer1/Timer3

When Timer1/Timer3 is operating in 16-bit mode and the prescale setting is not 1:1, a write to the TMR1H/TMR3H Buffer registers may lengthen the duration of the period between the increments of the timer for the period in which TMR1H/TMR3H was written.

Work around

Do not write to TMR1H/TMR3H while Timer1/Timer3 is running, or else write to TMR1L/TMR3L immediately following a write to TMR1H/TMR3H.

Do not write to TMR1H/TMR3H and then wait for another event before also updating TMR1L/TMR3L.

3. Module: MSSP

In Slave Transmit mode, when a transmission is initiated, the SSPBUF register may be written for up to 10 Tcy before additional writes are blocked. The data transfer may be corrupted if SSPBUF is written during this time.

The WCOL bit is set any time an SSPBUF write occurs during a transfer.

Work around

Avoid writing SSPBUF until the data transfer is complete, indicated by the setting of the SSPIF bit (PIR1<3>).

Verify the WCOL bit (SSPCON1<7>) is clear after writing SSPBUF to ensure any potential transfer in progress is not corrupted.

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4. Module: Interrupts

If a high priority interrupt occurs during a two-cycle instruction that modifies the STATUS, BSR or WREG register, the unmodified value of the register will be saved to the corresponding Fast Return (Shadow) register and upon a fast return from the interrupt, the unmodified value will be restored to the STATUS, BSR or WREG register.

For example, if a high priority interrupt occurs during the instruction, `MOVFF TEMP, WREG`, the `MOVFF` instruction will be completed and WREG will be loaded with the value of TEMP before branching to ISR. However, the previous value of WREG will be saved to the Fast Return register during ISR branching. Upon return from the interrupt with a fast return, the previous value of WREG in the Fast Return register will be written to WREG. This results in WREG containing the value it had before execution of `MOVFF TEMP, WREG`.

Affected instructions are:

`MOVFF Fs, Fd`
where Fd is WREG, BSR or STATUS;

`MOVSF Zs, Fd`
where Fd is WREG, BSR or STATUS; and

`MOVSS [Zs], [Zd]`
where the destination is WREG, BSR or STATUS.

Work around

1. Assembly Language Programming: If any two-cycle instruction is used to modify the WREG, BSR or STATUS register, do not use the `RETFIE FAST` instruction to return from the interrupt. Instead, save/restore WREG, BSR and STATUS via software in the same manner as is done with low priority interrupts. Alternatively, in the case of `MOVFF`, use the `MOVF` instruction to write to WREG instead.
2. C Language Programming: The exact work around depends on the compiler in use. Please refer to your C Compiler documentation for details.

If using the Microchip MPLAB® C18 C Compiler, define both high and low priority interrupt handler functions as “low priority” by using the `pragma interruptlow` directive. This directive instructs the compiler to not use the `RETFIE FAST` instruction. If the proper high priority interrupt bit is set in the IPRx register, then the interrupt is treated as high priority in spite of the `pragma interruptlow` directive.

The following code snippet demonstrates the work around using the C18 compiler:

```
#pragma interruptlow MyLowISR
void MyLowISR(void)
{
    // Handle low priority interrupts.
}

// Although MyHighISR is a high priority interrupt, use interruptlow pragma so that
// the compiler will not use retfie FAST.

#pragma interruptlow MyHighISR
void MyHighISR(void)
{
    // Handle high priority interrupts.
}

#pragma code highVector=0x08
void HighVector (void)
{
    _asm goto MyHighISR _endasm
}
#pragma code /* return to default code section */

#pragma code lowVector=0x18
void LowVector (void)
{
    _asm goto MyLowISR _endasm
}
#pragma code /* return to default code section */
```

5. Module: ECCP

When monitoring a shutdown condition using a bit test on the ECCPASE bit (ECCP1AS<7>), or performing a bit operation on the ECCPASE bit, the device may produce unexpected results.

Work around

Before performing a bit test or bit operation on the ECCPASE bit, copy the ECCP1AS register to the working register and perform the operation there.

By avoiding these operations on the ECCPASE bit in the ECCP1AS register, the module will operate normally.

In Example 1, ECCPASE bit operations are performed on the W register.

EXAMPLE 1:

```
MOVF    ECCP1AS, W
BTFSC   WREG, ECCPASE
BRA     SHUTDOWN_ROUTINE
```

6. Module: ECCP

ECCP1 configured for auto-shutdown with Comparator 1 corrupts the PWM duty cycle pulse. In addition, it does not always synchronize the pulse to the beginning of the period and the end of the pulse can occur at any time within the period.

Work around

None.

7. Module: ECCP

When operating either Timer1 or Timer3 as a counter with a prescale value other than 1:1 and operating the ECCP in Compare mode with the Special Event Trigger (CCP1CON bits CCP1M3:CCP1M0 = 1011), the Special Event Trigger Reset of the timer occurs as soon as there is a match between TMRxH:TMRxL and CCPR1H:CCPR1L.

This differs from the PIC18F452, where the Special Event Trigger Reset of the timer occurs on the next rollover of the prescale counter after the match between TMRxH:TMRxL and CCPR1H:CCPR1L.

Work around

To achieve the same timer Reset period on the PIC18F4550 family as the PIC18F452 family for a given clock source, add 1 to the value in CCPR1H:CCPR1L. In other words, if CCPR1H:CCPR1L = x for the PIC18F452, to achieve the same Reset period on the PIC18F4550 family, CCPR1H:CCPR1L = x + 1, where the prescale is 1, 2, 4 or 8 depending on the T1CKPS1:T1CKPS0 bit values.

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8. Module: A/D

The A/D offset is greater than the specified limit in Table 28-28 of the Device Data Sheet. The updated conditions and limits are shown in **bold** text in Table 1.

Work around

Three work arounds exist.

1. Configure the A/D to use the VREF+ and VREF- pins for the voltage references. This is done by setting the VCFG<1:0> bits (ADCON1<5:4>).
2. Perform a conversion on a known voltage reference voltage and adjust the A/D result in software.
3. Increase system clock speed and adjust A/D settings accordingly. Higher system clock frequencies decrease offset error.

**TABLE 1: A/D CONVERTER CHARACTERISTICS: PIC18F2455/2550/4455/4550 (INDUSTRIAL)
PIC18LF2455/2550/4455/4550 (INDUSTRIAL)**

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
A06A	E _{OFF}	Offset Error	—	—	<±1.5	LSb	VREF = VREF+ and VREF-
A06	E _{OFF}	Offset Error	—	—	<±3.5	LSb	VREF = Vss and VDD

9. Module: DC Characteristics (BOR)

The values for parameter D005 (VBOR) in **Section 28.1 “DC Characteristics”** of the Device Data Sheet, when the trip point for BORV1:BORV0 = 11, are not applicable as the device may reset below the minimum operating voltage for the device.

Work around

None.

10. Module: USB

When an IN endpoint is owned by USB SIE and the UCON register PKTDIS bit is set, if a USB NAK event occurs on the IN endpoint before the PKTDIS bit is clear, then after the PKTDIS bit is clear, the pending IN endpoint will send out more bytes than expected. For example, if configured to send out 8 bytes, the SIE would actually send out 12 bytes of data.

Work around

The PKTDIS bit is set when a USB control transfer setup packet is received. Clear this bit as soon as possible, and clear it before turning over any IN endpoint ownership to the SIE.

In the distributed C18 version of the USB library, the following change should be made:

File: usbctrltrf.c, version 1.0, dated 11/19/04

Function:

```
void USBCtrlEPServiceComplete(void)
```

Required Modification:

Move UCONbits.PKTDIS = 0, which is located at the end of the function, to the start of the function instead.

REVISION HISTORY

Rev A Document (11/2004)

Original version of this document. Includes silicon issues 1 (EUSART), 2 (Timer1/Timer3), 3 (MSSP), 4 (Interrupts), 5-7 (ECCP), 8 (A/D) and 9 (DC Characteristics (BOR)).

Rev B Document (07/2005)

Added silicon issue 10 (USB).

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NOTES:

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