ENGR 2420: Final Project

Proposal due in lab on April 29, 2020
Report due by 5 PM on May 8, 2020

For the final project, you will need to choose a circuit that you find interesting, learn about it, implement it in simulation or on a breadboard, and tell me something interesting that you learned about it in the process in a final report. Your report will need to include relevant background information, a schematic of your circuit and plots showing some simulation results or some measurement results that you obtained from your circuit, and a description of what you learned. You can work by yourself or in a group of up to three students. The final report is due by 5 PM on Friday, May 8. By the start of lab on Wednesday, April 29, you will need to submit a brief (e.g., one-page) project proposal indicating with whom (if anyone) you will be working, a description of what you would like to do for your project, and any relevant references that you found.

Your circuit should to be something that, in principle, you could implement in a breadboard using the parts that we have been using in the labs this semester (e.g., MMPQ3904, ALD1106, ALD1107, op anps, resistors, capacitors, etc.). Provided below is a list of some project ideas. You are free to adopt one of these, to adapt one from the list, or to ignore the list and come up with one of your own.

Project Ideas:

1. **A MOSFET-Only Current-Output D/A Converter**. Design a current-output digital-to-analog converter based on a MOS transistor R-2R ladder network, such as the one that you looked at in Postlab 6. (*Suggested references*: C. M. Hammerschmied and Q. Huang, "Design and Implementation of an Untrimmed MOSFET-Only 10-Bit A/D Converter with −79-dB THD," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 8, pp. 1148–1157, 1998; B. Linares-Barranco, T. Serrano-Gotarredona, and R. Serrano-Gotarredona, "Compact Low-Power Calibration Mini-DACs for Neural Arrays With Programmable Weights," *IEEE Transactions on Neural Networks*, vol. 14, no. 5, pp. 1207–1216, 2003.)

2. **A Rail-to-Rail CMOS Differential Amplifier**. Design a CMOS differential amplifier that can operate with a rail-to-rail common-mode input voltage range and a wide output swing. Such designs typically make use of a complementary pair of differential pairs to to achieve the rail-to-rail common-mode input-voltage range, similar to the approach that you took in Postlab 9. The real deal usually includes some extra stuff to keep the overall transconductance of the circuit nearly constant as a function of the common-mode input voltage; in effect, only one of the differential pairs is ever on at one time. Such an input stage is usually called a *constant-g_m rail-to-rail input stage*.

3. **An Adaptive-Biasing Differential Amplifier**. The differential amplifiers that we have studied all have a finite *slew rate*, which means that the output voltage ramps up linearly in time at some finite rate when a large differential input is applied. This arises primarily because the differential input stage has a fixed total bias current, which

limits the amount of current that the amplifier can supply to charge a load capacitance. A constant current charging or discharging a capacitor results in a ramp-like output signal. An adaptive-biasing amplifier is capable of sensing when it is slewing and temporarily increases its own bias current to allow the output to "catch up" quickly with the differential input. (*Suggested reference*: M. G. Degrauwe, J. Rijmenants, E. A. Vittoz, and H. J. de Man, "Adaptive Biasing CMOS Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. SC-17, no. 3, pp. 522–528, 1982.)

4. **A Class-AB Differential Amplifier**. This type of circuit has an enhanced slew rate, similar to an adaptive-biasing differential amplifier, but instead of adapting the bias current in a conventional differential pair it replaces the differential pair with a transconductor that has an expansive nonlinear current–voltage characteristic (e.g., sinh-like instead of tanh-like). (*Suggested references*: B. A. Minch, "A Simple Class-AB Transconductor in CMOS," in *Proceedings of the 2008 IEEE International Symposium on Circuits and Systems*, Seattle, WA, May 2008, pp. 69–72; V. Peluso, P. Vancorenland, M. Steyaert, and W. Sansen, "900mV Differential Cass AB OTA for Switched Opamp Applications," *Electronics Letters*, vol. 33, no. 17, pp. 1455–1456, 1997; R. Harjani, R. Heineke, and F. Wang, "An Integrated Low-Voltage Class AB CMOS OTA," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 2, pp. 134–142, 1999.)

5. **A Differential-Difference Amplifier**. The differential-difference amplifier (DDA) is an extension of the traditional operational amplifier concept. It amplifies the difference between two differential voltages. With such a circuit, we can implement many building blocks commonly implemented with operational amplifiers and resistors (e.g., precision-gain amplifiers, unity-gain inverting amplifier, voltage adder/subtractor, voltage doubler/subtractor) with simple feedback connections that parallel the unity-gain follower connection (i.e., no external passive components). However, for these circuits to work well, the input differential stages must have a relatively large linear range. (*Suggested reference*: E. Säckinger and W. Guggenbühl, "A Versatile Building Block: The CMOS Differential Difference Amplifier," *IEEE Journal of Solid-State Circuits*, vol. SC-22, no. 2, pp. 287–294, 1987.)

6. **CMOS Translinear Circuits**. In weak inversion, the MOS transistor has an exponential current–voltage characteristic like the bipolar transistor, and so can be used to implement translinear circuits. It turns out that if you make the transconductance of a device linear in its controlling voltage instead of its output current, you obtain a square-law current–voltage relationship. So, the MOS transistor is also a translinear device in strong inversion. (*Suggested references*: B. A. Minch, "MOS Translinear Principle for All Inversion Levels," *IEEE Transactions on Circuits and Systems II*, vol. 55, no. 2, pp. 121-125, 2008; A. G. Andreou and K. A. Boahen, "Translinear Circuits in Subthreshold MOS," *Analog Integrated Circuits Signal Processing*, vol. 9, no. 2, pp. 141–166, 1996. E. Seevinck and R. J. Wiegerink, "Generalized Translinear Circuit Principle," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 8, pp. 1098–1102, August 1991.)