A Current-Mirror Differential Amplifier

9.1 Objectives

In this lab, you will examine the voltage transfer characteristics, the output-voltage swing, and the dynamical properties of another simple MOS differential amplifier comprising an *n*MOS differential pair and three simple current mirrors. The amplifier that you will construct and characterize is conceptually very similar to the one that you investigated in Lab 8, but this one has a *rail-to-rail output swing*, which means that the high-gain region of the VTC extends from one rail all the way to the other. This type of amplifier is called a *current-mirror* differential amplifier, for reasons that should be relatively obvious.

9.2 Prelab

The following prelab questions have been constructed to help you prepare to do the lab efficiently. Unless otherwise stated, you should assume that like transistors are matched and that the Early effect is negligible. Please complete these questions *before* you come to lab. While you may discuss the prelab questions with your lab partner or with other students in the class, each student in a lab group should complete the prelab assignment individually, so that you each understand the circuit that you will be testing and what you will be doing in the lab.

1. Consider the differential amplifier circuit shown in Fig. 9.1a comprising an *n*MOS differential pair and three simple current mirrors. In answering these questions, you should assume that all transistors of the same type are matched. Which input voltage is the noninverting input? Which is the inverting input? Explain your reasoning briefly.

2. If the output voltage were fixed by a voltage source so that M_4 and M_8 are both saturated, what would be the output current in terms of I_1 and I_2 if the Early effect were negligible?

3. How does I_{out} depend on $V_1 - V_2$ if $V_1 \approx V_2$ (*Hint*: note the sinuous nature of the thingy between the V_1 and V_2)? What is I_{out} if $V_1 \ll V_2$? What is I_{out} if $V_1 \gg V_2$?

4. Now suppose that we connect the current-mirror differential amplifier of Fig. 9.1a as a unity-gain follower and that we connect a large load capacitor, C, to its output, as shown in Fig. 9.1b. If V_{in} has remained constant for a long period of time, what would be the value of V_{out}? If we were to make a small-amplitude step change to V_{in}, how

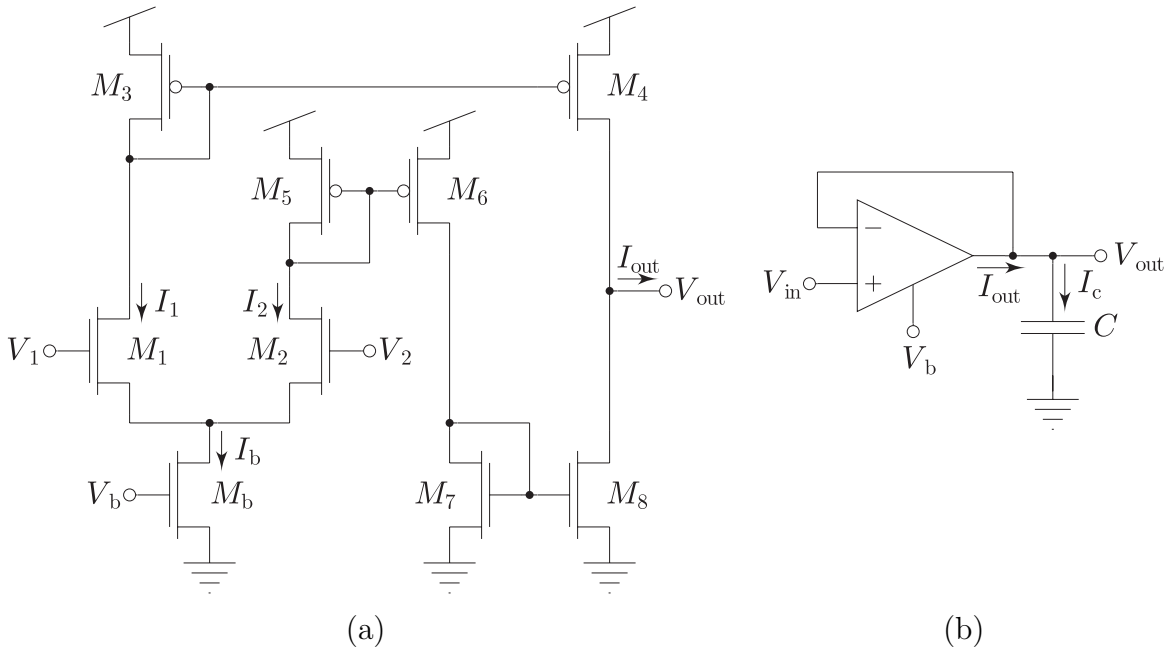

Figure 9.1: (a) A simple MOS current-mirror differential amplifier. (b) A follower-connected current-mirror differential amplifier driving a load capacitor, C.

would V_{out} change in time shortly after the step? If we were to make a large-amplitude step change to V_{in}, how would V_{out} change in time shortly after the step? (*Hint*: Apply KCL at V_{out} to obtain a differential equation for V_{out} and integrate the differential equation to obtain $V_{\text{out}}(t)$.)

9.3 Experiments

You will be doing three experiments in this lab. In the first experiment, you will examine the VTCs of the current-mirror differential amplifier and its output-voltage range. In the second experiment, you will measure the incremental output resistance of the amplifier and its incremental transconductance gain. You will also compute find the differential-mode voltage gain of the circuit in two different ways. In the third experiment, you will investigate the time response of your amplifier configured as a unity-gain follower to both small-amplitude and large-amplitude steps. You will be constructing your circuits from transistors on an ALD1106 quad nMOS transistor array or from transistors on an ALD1107 quad pMOS transistor array. Please note that these are CMOS chips, so you should follow good ESD practices so that these chips survive from one lab to the next. Also, please recall that MOS transistors are four-terminal devices and you will need to connect ground to pin 4 and V_{dd} to pin 11 of both the ALD1106 and the ALD1107 to establish the proper bulk voltage each type of chip.

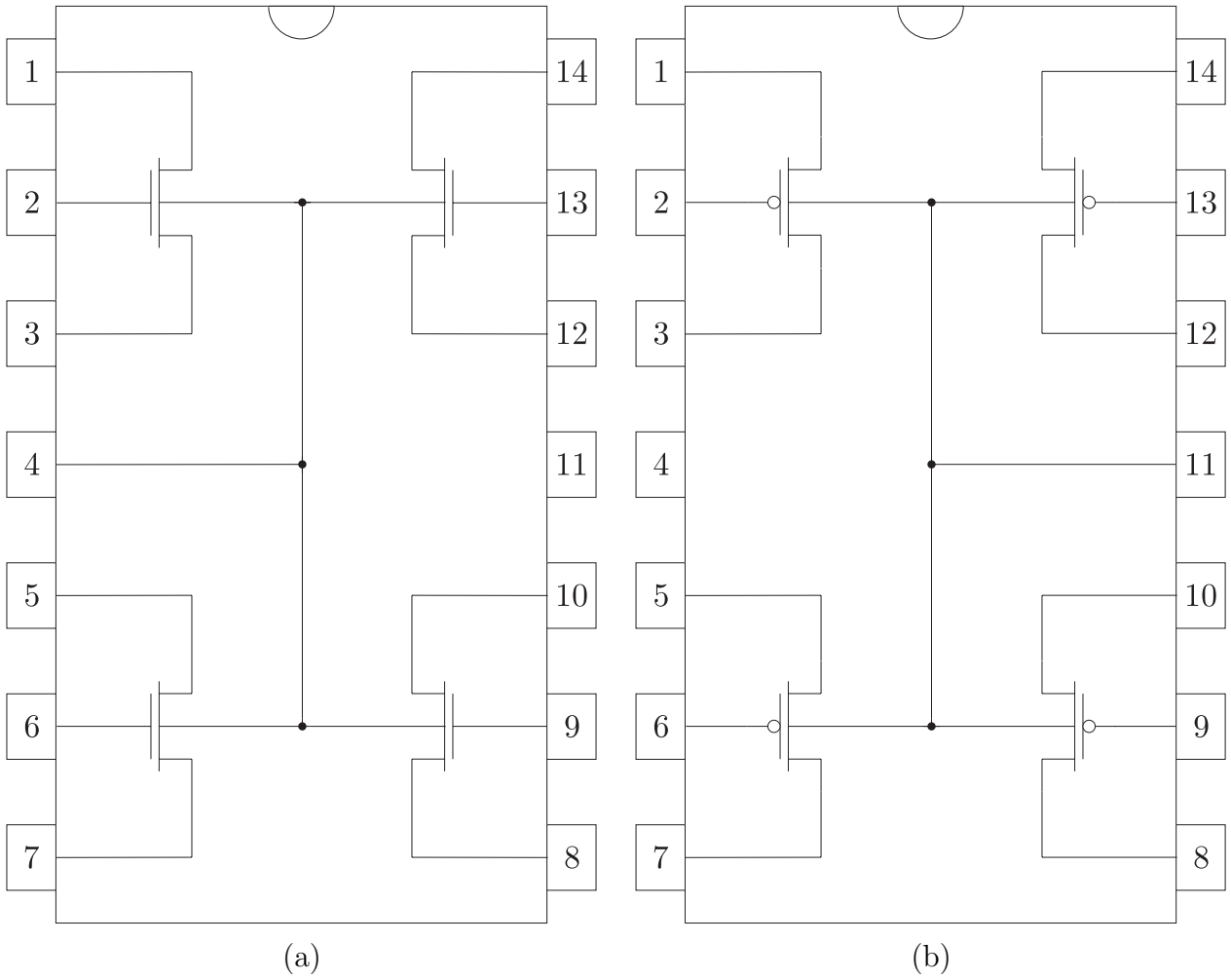

Figure 9.2: Pinouts of (a) the ALD1106 quad nMOS transistor array and (b) the ALD1107 quad pMOS transistor array.

9.3.1 Experiment 1: Voltage Transfer Characteristics

Construct a current-mirror differential amplifier, as shown in Fig. 9.1, with an nMOS differential pair, two simple pMOS current mirrors, and a simple nMOS current mirror. Set the bias voltage of the differential pair so that your bias current is on the order of of microamps, which is in moderate inversion.

As you did in Lab 8, connect the inverting input to a constant voltage source and sweep the noninverting input from one rail to the other, measuring V_{out} for at least three different values of the voltage on the inverting input. In your report, include a single plot showing all of these VTCs. How does the behavior of this amplifier compare to that of the simple differential amplifier that you investigated in Lab 8?

9.3.2 Experiment 2: Transconductance, Output Resistance, and Gain

For a single value of the inverting input voltage, sweep the noninverting input around the inverting one in fine increments while measuring V_{out}. You should try to get several points in the high-gain region. Fit a straight line to the steep part of the curve and determine the differential-mode voltage gain of your circuit from the slope of the best-fit line. In your report, include a plot showing V_{out} versus V_{dm} along with the best-fit line.

Next, set the differential-mode input voltage to zero and measure the current flowing into the output of the amplifier as you sweep V_{out} from one rail to the other. Fit a straight line to the shallow part of this output current–voltage characteristic, which should correspond to the range of output voltages over which the gain of the circuit is large, and determine the incremental output resistance of the circuit from the slope of the best-fit line. In your report, include a plot showing the output current-voltage characteristic along with the best-fit line.

Finally, fix the output voltage somewhere in the range of output voltages for which the circuit's gain is large and measure the current flowing out of the amplifier as you sweep V_{dm} around zero. You should sweep V_{dm} over a sufficiently large range that I_{out} saturates both for positive and for negative values of V_{dm}. Fit a straight line to the curve around where $V_{\text{dm}} = 0$ and extract a value of the incremental transconductance gain of the circuit with the output voltage fixed from the slope of the best-fit line. Also, record the limiting values of I_{out} in both the positive and the negative directions. In your report, include a plot showing I_{out} versus V_{dm} along with the best-fit line.

From your incremental output resistance and your incremental transconductance gain, compute the differential-mode voltage gain of your circuit. How does this value of for the differential-mode gain compare to that which you obtained directly from the slope of the VTC? How does the differential-mode gain of this amplifier compare with that of the simple one that you investigated in Lab 8?

9.3.3 Experiment 3: Unity-Gain Follower Step Response

Configure your amplifier as a unity-gain follower by connecting the output to the inverting input, as you did in Lab 8. Now, load your follower-connected amplifier with a 1 nF capacitor connected between the output of your amplifier and ground.

Apply a small-amplitude square wave to the input of your circuit and observe both the input and output waveforms as a function of time. The peak-to-peak amplitude of your square wave should be smaller than the range of differential-mode voltages over which the I_{out} versus V_{dm} curve that you measured in Experiment 2 was approximately linear. The DC offset should be sufficiently large that the bias transistor of the differential pair always remains in saturation. Adjust the frequency of the square wave and the total simulation time so that you can simultaneously see V_{out} settle into its final value after both an up-going and a down-going step. Is the response symmetrical? Does the amplifier exhibit approximately linear behavior? Extract a time constant both for the up-going and for the down-going output transitions. How do these compare with that which you compute from the measured values of the load capacitance and the differential-mode transconductance gain that you found in Experiment 2? In your report, include a single plot showing both scope traces

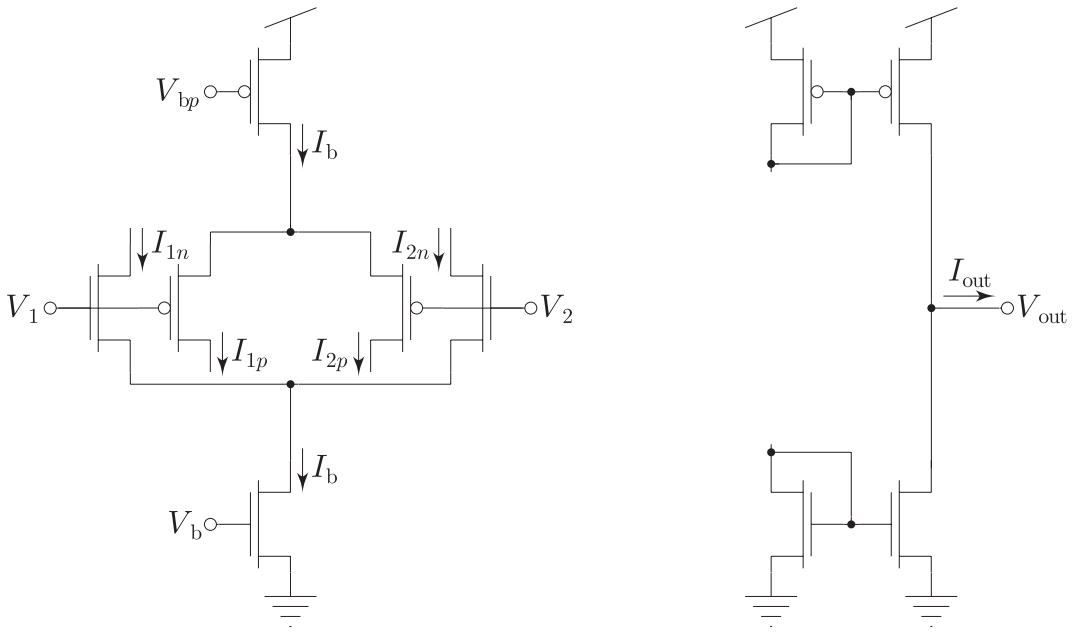

Figure 9.3: An input stage and an output stage for a current-mirror differential amplifier with a rail-to-rail common-mode input range and a rail-to-rail output swing.

along with the extracted time constants.

Next, increase the amplitude of your square wave so that it is a couple of volts. Again, the DC offset should be sufficiently large that the bias transistor of the differential pair always remains in saturation. Adjust the frequency of the square wave and the total simulation time so that you can simultaneously see V_{out} settle into its final value after both an up-going and a down-going step. Is the response symmetrical? You will probably notice that the output of the amplifier follows a linear trajectory in time over most of its response to the large input step. This behavior is called *slewing*, and the constant rate of change of the output voltage with respect to time is called the *slew rate* of the amplifier. Extract a slew rate for both for the up-going and for the down-going output transitions. How do these compare with those which you compute from the load capacitance and the limiting values of the output current? In your report, include a single plot showing both scope traces along with the extracted slew rates.

9.4 Postlab

Recall that the common-mode input voltage to an nMOS differential pair must be sufficiently high that the bias transistor stays in saturation; otherwise, the total current flowing in the differential pair exponentially decreases with the common-mode input voltage. So, if we build a differential amplifier with an nMOS differential pair, we cannot let the input voltages get close to ground. On the other hand, if we instead used a pMOS differential pair, we could let the input voltages get near ground, but then we could not let the input voltages get too close to V_{dd}, or else the pMOS bias transistor would come out of saturation. If we would require

an amplifier that can be used to handle common-mode input voltages from rail to rail, we can use both types of differential pairs, as shown on the left in Fig. 9.3. For input voltages in the middle of the power rails, both differential pairs are properly biased. For input voltages near V_{dd}, the pMOS differential pair shuts off and the nMOS differential pair handles the input voltages. For input voltages near ground, the nMOS differential pair shuts off and the pMOS differential pair handles the input voltages. Design a bias circuit that accepts the nMOS differential pair bias voltage and produces a bias voltage for the pMOS differential pair, $V_{\mathrm{b}p}$, such that both differential pairs have nearly the same bias current I_{b}.

The current-mirror amplifier topology that you examined in this lab is capable of driving its output from one rail to the other. Design a current-mirror differential amplifier that can handle inputs near both power supply rails and that can drive the output voltage from rail to rail. Make V_1 the noninverting input and V_2 the inverting input.

Create a schematic of your design in LTspice, connect it as a unity-gain follower, and load your follower with a 10 pF capacitor, and set the bias current level to be on the high end of moderate inversion (e.g., about $10I_{\mathrm{s}}$, which should be on the order of $10\,\mu$A). Simulate the small-amplitude (e.g., 50 mV) step response of your amplifier for steps starting near (but not at) each rail and in the middle. Turn in plots showing your simulation results. Does the time constant of the circuit change near the rails compared to in the middle of the input range?

Hints: Identify the corresponding output currents of the two differential pairs (i.e., the ones that increase with increasing V_{dm} and the ones that decrease with increasing V_{dm}). Next, add the corresponding output currents together and mirror the current sums to the output. The circuit can be completed with two additional current mirrors.