ENGR 2420: Introduction to Microelectronic Circuits

April 14, 2020

6 Incremental Driving-Point Transfer Function Calculation of CMOS Circuits by Source Splitting

In this section, we shall illustrate the use of (voltage) source splitting to aid in the calculation of the incremental driving-point transfer functions of circuits made from MOS transistors, illustrating the technique by applying it to calculating the incremental input and output resistances of several simple circuits.

6.1 Incremental Transconductance Gain of a Source-Degenerated MOS Transistor

In this section, we shall derive a useful result, which gives the change in the channel current of a saturated MOS transistor in response to a small change in the gate voltage with *source degeneration*. If the source voltage were fixed, the change in the saturation current due to a small change in the gate voltage would be given by $\delta I_{\rm sat} = g_{\rm m}\delta V_{\rm G}$. However, if the source voltage were connected to another device or circuit with a finite incremental terminal resistance, $R_{\rm X}$, as shown on the left in Fig. 1, then the change in the saturation current also must flow into the terminal of X, causing $V_{\rm S}$ to increase. This increase in $V_{\rm S}$, in turn, reduces the original increase in $I_{\rm sat}$ caused by the change in $V_{\rm G}$. In such cases, the effective transconductance of the MOS transistor is reduced or *degenerated* from its value with $V_{\rm S}$ held constant, whence the name *source degeneration*.

We can write the change in the channel current of the MOS transistor due to the change in both the gate voltage and the source voltage as

$$\delta I_{\rm sat} = g_{\rm m}\delta V_{\rm G} - g_{\rm s}\delta V_{\rm S}.$$

This same current increase also must flow into the other part of the circuit, so we can also write that

$$\delta I_{\rm sat} = \frac{\delta V_{\rm S}}{R_{\rm X}}.$$

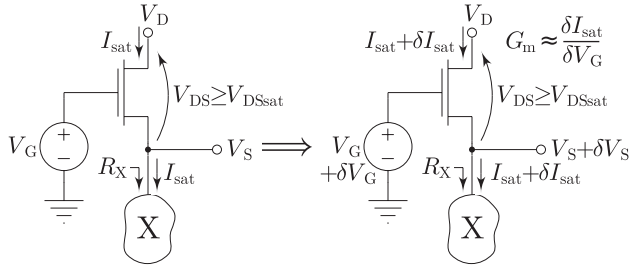


Figure 1: Incremental transconductance gain of an MOS transistor with source degeneration.

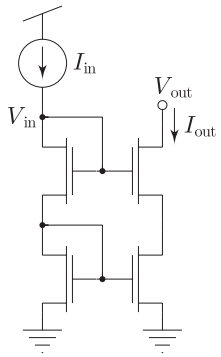


Figure 2: Stacked current mirror.

By equating these, we can solve for the change in the source voltage, which is given by

$$\delta V_{\text{S}} = \frac{g_{\text{m}} R_{\text{X}}}{1 + g_{\text{s}} R_{\text{X}}} \cdot \delta V_{\text{G}}.$$

We can substitute this result into the second equation for δI_{sat} to find that

$$\delta I_{\text{sat}} = \frac{g_{\text{m}}}{1 + g_{\text{s}} R_{\text{X}}} \cdot \delta V_{\text{G}},$$

from which it follows that the incremental transconductance of the MOS transistor with source degeneration is given by

$$G_{\text{m}} = \frac{\delta I_{\text{sat}}}{\delta V_{\text{G}}} = \frac{g_{\text{m}}}{1 + g_{\text{s}} R_{\text{X}}}.$$

We shall make use of this result again and again in performing incremental circuit analyses.

6.2 Source Splitting and Incremental DP Transfer Functions

In this section, we shall illustrate the process of calculating incremental driving-point resistances/conductances using source splitting and superposition via several worked examples. For our first pair of examples, we shall determine the incremental input and output resistances of the stacked cascode current mirror, shown in Fig. 2, using source splitting and superposition. We shall assume that all four nMOS transistors are identical and that the output voltage, V_{out}, is sufficiently far above ground to keep both output transistors saturated.

Example 6.1

To compute the incremental output resistance of the stacked mirror, we simply change the output voltage by a small amount, δV_{out}, and see how much additional current, δI_{out}, goes into the circuit. The ratio $\delta V_{\text{out}}/\delta I_{\text{out}}$ gives us the incremental output resistance. To facilitate the calculation, we can apply voltage source splitting to V_{out} and superposition, as shown in Fig. 3.

The only nonzero components of δI_{out} occur when we change the first replica test voltage source, because the second one is connected to the drain of the (saturated) cascode transistor. We can write δI_{out} as

$$\begin{aligned}
\delta I_{\text{out}} &= \underbrace{\frac{\delta V_{\text{out}}}{r_{\text{o}} + (r_{\text{o}} \| 1/g_{\text{s}})}}_{\delta I_{\text{out11}}} \left(1 - \underbrace{\frac{g_{\text{s}}}{g_{\text{s}} + (1/r_{\text{o}})}}_{\delta I_{\text{out21}}/\delta I_{\text{out11}}} \right) \\
&= \frac{\delta V_{\text{out}}}{r_{\text{o}} + (r_{\text{o}} \| 1/g_{\text{s}})} \cdot \frac{1/r_{\text{o}}}{g_{\text{s}} + (1/r_{\text{o}})} \\
&= \frac{\delta V_{\text{out}}}{r_{\text{o}} + (r_{\text{o}} \| 1/g_{\text{s}})} \cdot \frac{1}{g_{\text{s}} r_{\text{o}} + 1},
\end{aligned}$$

which implies that the incremental output resistance is given by

$$R_{\text{out}} = \frac{\delta V_{\text{out}}}{\delta I_{\text{out}}} = (g_{\text{s}} r_{\text{o}} + 1)\,(r_{\text{o}} + (r_{\text{o}} \| 1/g_{\text{s}})) \approx (g_{\text{s}} r_{\text{o}})\, r_{\text{o}},$$

because $g_{\text{s}} r_{\text{o}} \gg 1$. ∎

Example 6.2

To calculate the incremental input resistance of the stacked mirror, it is convenient to apply a voltage source, whose value is equal to the quiescent value of V_{in}, to the input node and change V_{in} by δV_{in} and calculate how much additional current goes into the circuit, as shown in Fig. 4. As we did in computing the incremental output resistance, we shall apply voltage-source splitting and superposition to facilitate the calculation. For each of the two simple current mirrors in the stack, we have a choice about whether or not to account for the Early effect on the input side of the circuit. The Early-effect resistors each effectively appear in parallel with a driving-point resistance that is on the order of $1/g_{\text{s}}$. Because $1/g_{\text{s}} \ll r_{\text{o}}$, it follows that $1/g_{\text{s}} \| r_{\text{o}} \approx 1/g_{\text{s}}$, which implies that these Early-effect resistors will have a negligible effect on the calculation. Neglecting the Early effect when possible greatly simplifies the analysis process. While accounting for the Early effect here is not

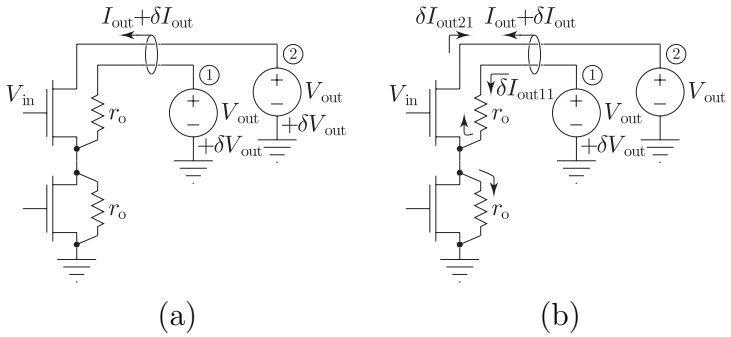


Figure 3: Calculation of the incremental output resistance of the stacked current mirror.

"wrong," it can certainly be counter productive. Unnecessarily accounting for the Early effect complicates greatly the expressions that we get out of the analysis process, which makes them harder to interpret. It also increases our chances of making an error along the way. Learning to recognize where the Early effect is negligible and where it is not is an important bit of circuit intuition to develop.

If we neglect the Early effect on the input side of the circuit, after we apply the test voltage source to the input and split it, we have the circuit shown in Fig. 5a. The only nonzero components of δI_{in} occur when we change the input voltage source on the second branch, as shown in Fig. 4b. Of these, the only nonzero component occurs in the third branch. So, we can write δI_{in} as

$$\delta I_{\text{in}} = \underbrace{\frac{g_{\text{m}}\delta V_{\text{in}}}{1+g_{\text{s}}\left(1/g_{\text{m}}\right)}}_{\delta I_{\text{in32}}} = \frac{g_{\text{m}}\delta V_{\text{in}}}{1+(1/\kappa)} = \frac{\kappa}{\kappa+1}\cdot g_{\text{m}}\delta V_{\text{in}},$$

which implies that the incremental input resistance is given by

$$R_{\text{in}} = \frac{\delta V_{\text{in}}}{\delta I_{\text{in}}} = \frac{\kappa+1}{\kappa}\cdot\frac{1}{g_{\text{m}}}.$$

If we had not neglected the Early effect on the input side of the circuit, we would have the situation depicted in Fig. 6 after applying the test input voltage source and splitting it. Of the sixteen components of δI_{in}, the only nonzero ones occur when we change the input voltage sources on the second and fourth branches. Each of these two cases is illustrated in Fig. 7. By inspection of these circuits, we can write the incremental input current as

$$\begin{aligned}\delta I_{\text{in}} \;=\; & \underbrace{\frac{g_{\text{m}}\delta V_{\text{in}}}{1+g_{\text{s}}\left(r_{\text{o}}\|r_{\text{o}}\|1/g_{\text{m}}\right)}}_{\delta I_{\text{in32}}}\left(1-\underbrace{\frac{1/r_{\text{o}}}{(2/r_{\text{o}})+g_{\text{m}}}}_{\delta I_{\text{out42}}/\delta I_{\text{out32}}}\right)\\ & +\underbrace{\frac{\delta V_{\text{in}}}{r_{\text{o}}+(1/g_{\text{s}}\|1/g_{\text{m}}\|r_{\text{o}})}}_{\delta I_{\text{in44}}}\left(1-\underbrace{\frac{g_{\text{s}}}{g_{\text{s}}+g_{\text{m}}+(1/r_{\text{o}})}}_{\delta I_{\text{out34}}/\delta I_{\text{out44}}}\right)\end{aligned}$$

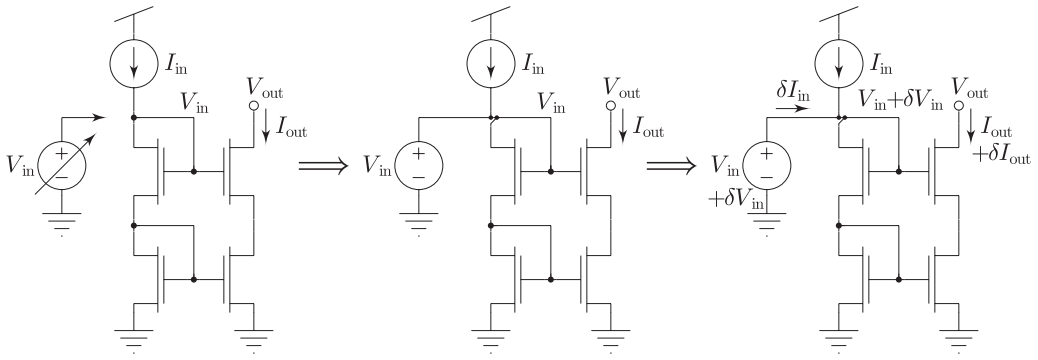
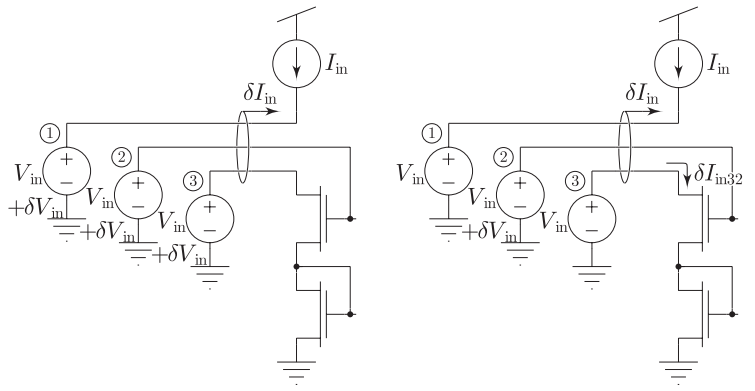


Figure 4: Set-up to determine the incremental input resistance of the stacked current mirror using the voltage-source method.



(a) (b)

Figure 5: Calculation of the incremental input resistance of the stacked current mirror using voltage-source splitting and superposition under the assumption that the Early effect is negligible.

$$= \frac{g_{\rm m}\delta V_{\rm in}}{1+g_{\rm s}\left(r_{\rm o}/2\|1/g_{\rm m}\right)}\cdot\frac{g_{\rm m}r_{\rm o}+1}{g_{\rm m}r_{\rm o}+2}+\frac{\delta V_{\rm in}}{r_{\rm o}+\left(\left(1/g_{\rm s}\|1/g_{\rm m}\right)\|r_{\rm o}\right)}\cdot\frac{g_{\rm m}r_{\rm o}+1}{\left(g_{\rm s}+g_{\rm m}\right)r_{\rm o}+1},$$

which implies that the incremental input resistance is given by

$$\begin{aligned} R_{\rm in} &= \frac{\delta V_{\rm in}}{\delta I_{\rm in}} \\ &= \left(\left(\frac{1}{g_{\rm m}}+\frac{1}{\kappa}\left(\frac{r_{\rm o}}{2}\middle\|\frac{1}{g_{\rm m}}\right)\right)\frac{g_{\rm m}r_{\rm o}+2}{g_{\rm m}r_{\rm o}+1}\right) \\ &\qquad \left\|\left(\left(r_{\rm o}+\left(\left(\frac{1}{g_{\rm s}}\middle\|\frac{1}{g_{\rm m}}\right)\middle\|r_{\rm o}\right)\right)\frac{\left(g_{\rm s}+g_{\rm m}\right)r_{\rm o}+1}{g_{\rm m}r_{\rm o}+1}\right)\right. \end{aligned}$$

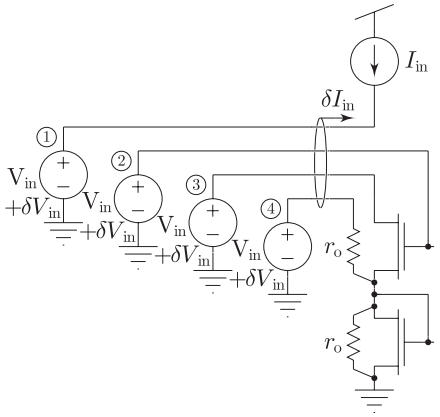


Figure 6: Calculation of the incremental input resistance of the stacked current mirror using voltage-source splitting and superposition with the Early effect.

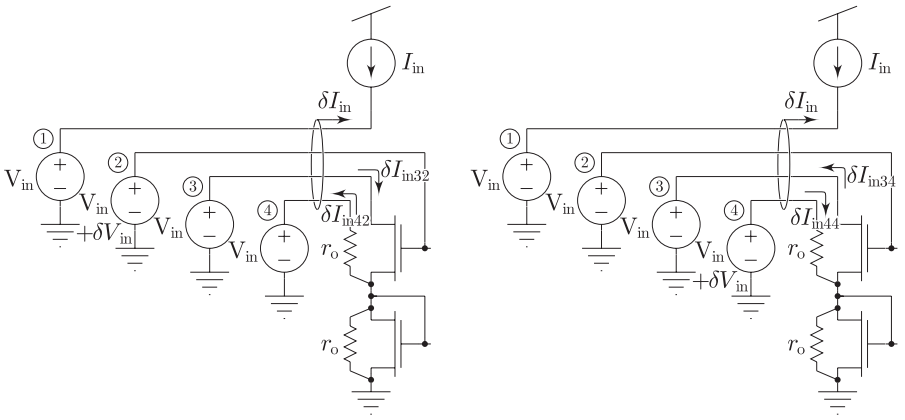


Figure 7: Continuation of the calculation of the incremental input resistance of the stacked current mirror using voltage source splitting and superposition with the Early effect.

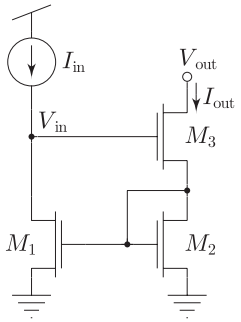


Figure 8: Wilson current mirror.

$$\begin{aligned}
&\approx \left(\frac{1}{g_{\rm m}}+\frac{1}{\kappa}\cdot\frac{1}{g_{\rm m}}\right)\Bigg\|\left(\left(r_{\rm o}+\left(\frac{1}{g_{\rm s}}\Bigg\|\frac{1}{g_{\rm m}}\right)\right)\frac{g_{\rm s}+g_{\rm m}}{g_{\rm m}}\right)\\
&\approx \left(\frac{\kappa+1}{\kappa}\cdot\frac{1}{g_{\rm m}}\right)\Bigg\|\left(\frac{\kappa+1}{\kappa}\cdot r_{\rm o}\right)\\
&= \frac{\kappa+1}{\kappa}\left(\frac{1}{g_{\rm m}}\Bigg\|r_{\rm o}\right)\\
&\approx \frac{\kappa+1}{\kappa}\cdot\frac{1}{g_{\rm m}},
\end{aligned}$$

where all of the approximations that we just made follow from the fact that $g_{\rm s}r_{\rm o}\gg 1$. This result is precisely what we found before with a whole lot less difficulty by neglecting the Early effect. ∎

Next, we shall determine the incremental input and output resistances of the Wilson current mirror, shown in Fig. 8, using source splitting and superposition. We shall assume that all three nMOS transistors are identical and that the output voltage, $V_{\rm out}$, is held sufficiently far above ground to keep the output transistor, M_3, saturated.

Example 6.3

To calculate the incremental input resistance of the Wilson mirror, it is convenient again to apply a voltage source, whose value is equal to the quiescent value of $V_{\rm in}$, to the input node and change $V_{\rm in}$ by $\delta V_{\rm in}$ and calculate how much additional current goes into the circuit, as shown in Fig. 9. As we did in computing the incremental input and output resistances of the stacked mirror, we shall apply voltage-source splitting and superposition to facilitate the calculation. Also, we shall neglect the Early effect for each of the three transistors in the circuit, because transistor M_1 is effectively diode connected through M_3 and M_2, because M_2 is actually diode connected, and because the drain of M_3 is held fixed for this calculation.

After we apply the test voltage source to the input and split it, we have the circuit shown in Fig. 10a. The only nonzero components of $\delta I_{\rm in}$ occur when we change the input voltage source on the second branch, as shown in Fig. 10b. Of these, the only nonzero component occurs in the third branch. So, we can write $\delta I_{\rm in}$ as

$$\delta I_{\rm in} = \underbrace{\frac{g_{\rm m}\delta V_{\rm in}}{1+g_{\rm s}\,(1/g_{\rm m})}}_{\delta I_{\rm in32}} = \frac{g_{\rm m}\delta V_{\rm in}}{1+(1/\kappa)} = \frac{\kappa}{\kappa+1}\cdot g_{\rm m}\delta V_{\rm in},$$

which implies that the incremental input resistance is given by

$$R_{\rm in} = \frac{\delta V_{\rm in}}{\delta I_{\rm in}} = \frac{\kappa+1}{\kappa}\cdot\frac{1}{g_{\rm m}}.$$

Thus, the incremental input resistance of the Wilson mirror is the same as that of the stacked mirror. ∎

Example 6.4

To compute the incremental output resistance of the Wilson mirror, we simply change the output voltage by a small amount, $\delta V_{\rm out}$, and see how much additional current, $\delta I_{\rm out}$, goes into the circuit. The ratio $\delta V_{\rm out}/\delta I_{\rm out}$ gives us the incremental output resistance. To facilitate the calculation, we can apply voltage source splitting to $V_{\rm out}$ and superposition, as shown in Fig. 11. As with the stacked mirror, the only nonzero components of $\delta I_{\rm out}$ occur when we

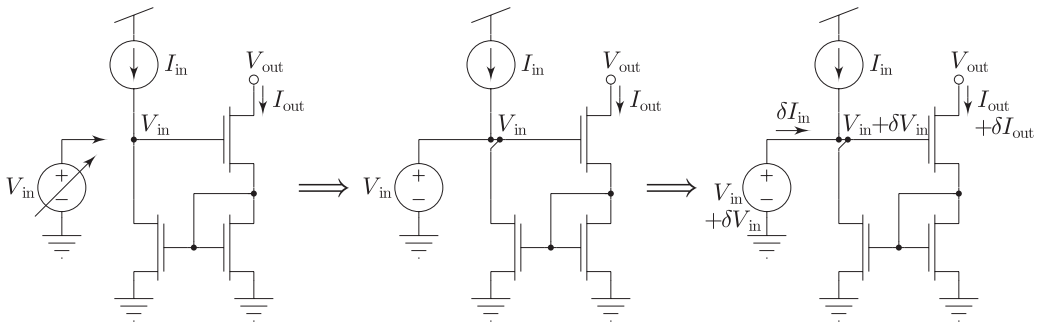


Figure 9: Set-up to determine the incremental input resistance of the Wilson current mirror using the voltage-source method.

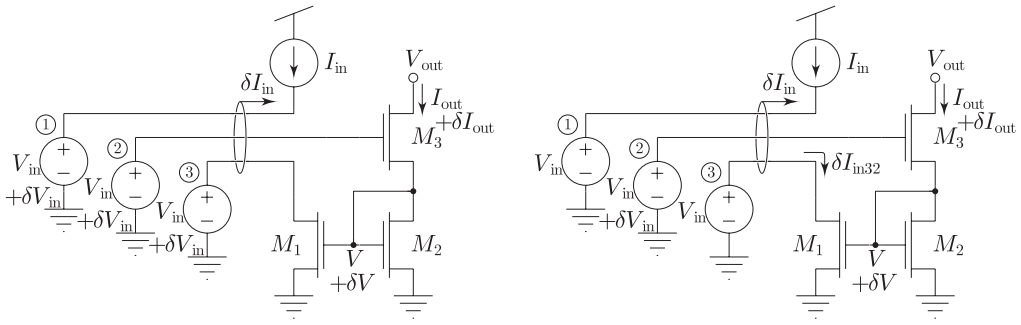


Figure 10: Calculation of the incremental input resistance of the Wilson current mirror using voltage-source splitting and superposition.

change the first replica test voltage source, as shown in Fig. 11b, because the second one is connected to the drain of M_3, which we have assumed to be saturated. We can write $\delta I_{\rm out}$ as

$$\begin{aligned}
\delta I_{\rm out} &= \underbrace{\frac{\delta V_{\rm out}}{r_{\rm o} + (1/G_{\rm S} \| 1/g_{\rm m})}}_{\delta I_{\rm out11}} \underbrace{\left(1 - \frac{G_{\rm S}}{g_{\rm m} + G_{\rm S}}\right)}_{\delta I_{\rm out21}/\delta I_{\rm out11}} \\
&\approx \frac{\delta V_{\rm out}}{r_{\rm o}} \left(1 - \frac{G_{\rm S}}{g_{\rm m} + G_{\rm S}}\right) \\
&= \frac{\delta V_{\rm out}}{r_{\rm o}} \cdot \frac{g_{\rm m}}{g_{\rm m} + G_{\rm S}},
\end{aligned}$$

where $G_{\rm S}$ denotes the effective incremental conductance looking into the source of M_3, $g_{\rm m}$ is the incremental conductance looking into the gate/drain of M_2, and the approximation follows from the fact that $1/g_{\rm m} \ll r_{\rm o}$, regardless of the precise value of $G_{\rm S}$. Recall that $g_{\rm s}$ denotes the incremental conductance of the source of a saturated MOS transistor with the

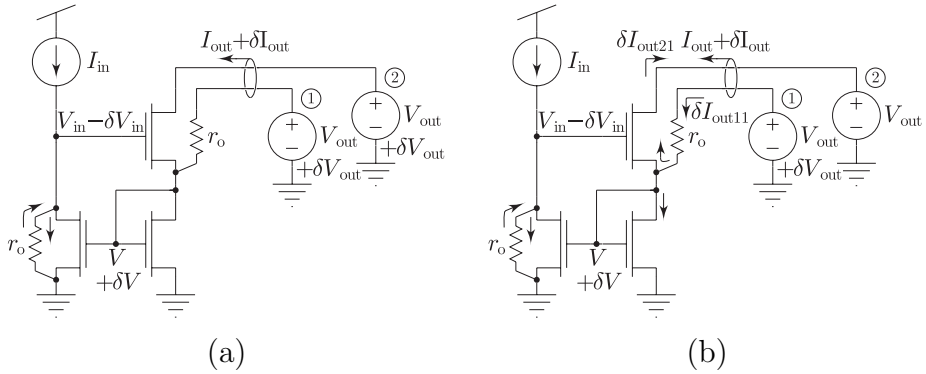


Figure 11: Calculation of the incremental output resistance of the Wilson current mirror.

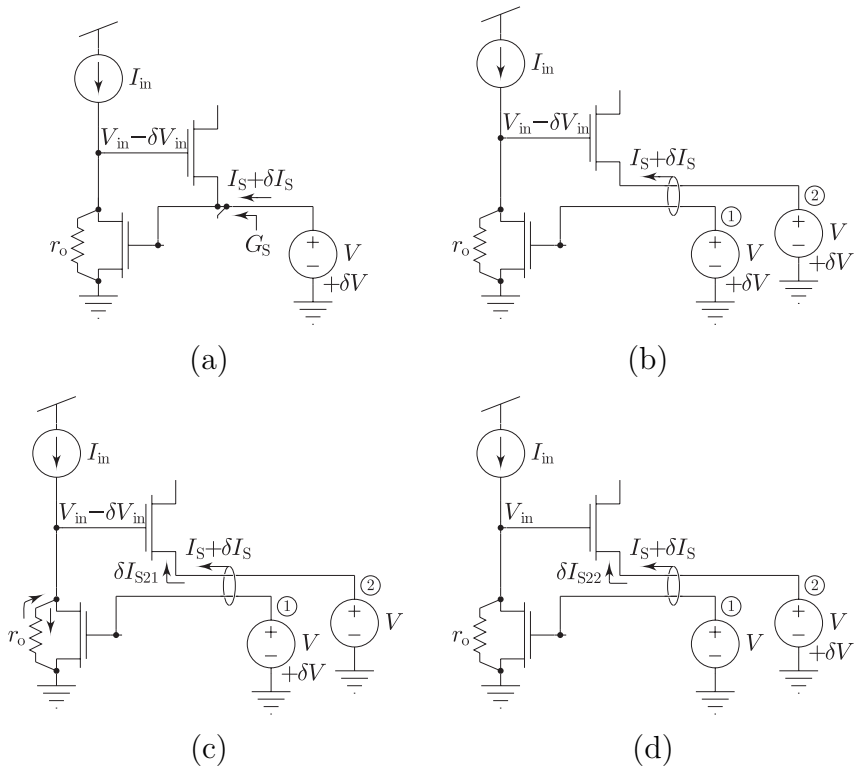


Figure 12: Auxiliary calculation of the incremental source conductance of M_3 including the effect of the changing input voltage.

gate voltage fixed, which is not the case in the Wilson mirror. The incremental current that flows through M_2 is mirrored by M_1 to the input of the circuit. Because I_{in} has not changed, V_{in}, which is the gate voltage of M_3 will decrease in response.

To compute G_{S}, we can recursively apply voltage-source splitting and superposition on the relevant part of the circuit, as shown in Fig. 12a and Fig. 12b. Each of the two replica test voltage sources elicits a single nonzero component of the current flowing into the source of M_3, I_{S}, as shown in Fig. 12c and Fig. 12d. By inspection of these circuits, we can write δI_{S} as

$$\begin{aligned}\delta I_{\text{S}} &= \underbrace{-g_{\text{m}}\underbrace{(-g_{\text{m}}r_{\text{o}}\delta V)}_{\delta V_{\text{in}}}}_{\delta I_{\text{S21}}} + \underbrace{g_{\text{s}}\delta V}_{\delta I_{\text{S22}}} \\ &= g_{\text{s}}\left(\kappa g_{\text{m}}r_{\text{o}}+1\right)\delta V,\end{aligned}$$

whence it follows that

$$G_{\text{S}} = \frac{\delta I_{\text{S}}}{\delta V} = g_{\text{s}}\left(\kappa g_{\text{m}}r_{\text{o}}+1\right) \approx \left(g_{\text{m}}r_{\text{o}}\right) g_{\text{m}},$$

where the approximation follows from $g_{\text{m}}r_{\text{o}} \gg 1$. Thus, we have that the incremental output

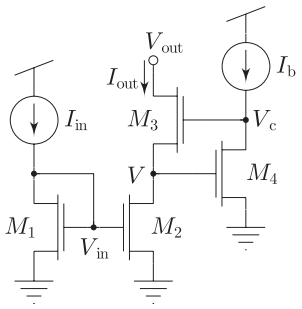


Figure 13: A simple current mirror with a regulated cascode.

resistance of the Wilson mirror is given approximately by

$$R_{\text{out}} = \frac{\delta V_{\text{out}}}{\delta I_{\text{out}}} \approx \left(\frac{G_{\text{S}}}{g_{\text{m}}} + 1\right) r_{\text{o}} \approx \left(\frac{g_{\text{m}} r_{\text{o}} \cdot g_{\text{m}}}{g_{\text{m}}} + 1\right) r_{\text{o}} = (g_{\text{m}} r_{\text{o}} + 1)\, r_{\text{o}} \approx (g_{\text{m}} r_{\text{o}})\, r_{\text{o}},$$

where all of these approximations again follow from the fact that $g_{\text{m}} r_{\text{o}} \gg 1$. Thus, the incremental output resistance of the Wilson mirror is on the same order as that of the stacked mirror. ∎

Finally, we shall calculate the incremental output resistance of the circuit shown in Fig. 13. This circuit is a simple current mirror with a *regulated cascode* on the output branch. In a regulated cascode, the cascode bias voltage, V_{c}, is not fixed, but rather is set by a simple amplifier, comprising the bias current source, I_{b}, and transistor M_4, connected in a negative feedback loop, whose goal is to regulate the voltage, V, which is the voltage across the output transistor of the simple mirror, M_2. We shall assume that all of the transistors are matched. Also, we shall assume that V_{out} is high enough to keep M_3 in saturation and that transistors M_2 and M_4 are also operating in saturation. Note that transistors M_2 and M_3 are connected in series and must passing the same saturation current. Thus, they will both have the same value of g_{m} and r_{o}. However, transistor M_4 will be passing I_{b}, which is, in general, different from I_{out}, so it will have a different set of incremental parameters, which we shall denote by g_{m4} and r_{o4}.

Example 6.5

To compute the incremental output resistance of the circuit of Fig. 13, we simply change the output voltage by a small amount, δV_{out}, and see how much additional current, δI_{out}, goes into the circuit, as shown in Fig. 14a and Fig. 14b. The ratio $\delta V_{\text{out}}/\delta I_{\text{out}}$ gives us the incremental output resistance. To facilitate the calculation, we can apply voltage source splitting to V_{out} and superposition, as shown in Fig. 14c. As with the stacked mirror and the Wilson mirror, the only nonzero components of δI_{out} occur when we change the first replica test voltage source, as shown in Fig. 11b, because the second one is connected to the drain of M_3, which we have assumed to be saturated. We can write δI_{out} as

$$\delta I_{\text{out}} = \underbrace{\frac{\delta V_{\text{out}}}{r_{\text{o}} + (1/G_{\text{S}} \| r_{\text{o}})}}_{\delta I_{\text{out11}}} \underbrace{\left(1 - \frac{G_{\text{S}}}{G_{\text{S}} + (1/r_{\text{o}})}\right)}_{\delta I_{\text{out21}}/\delta I_{\text{out11}}}$$

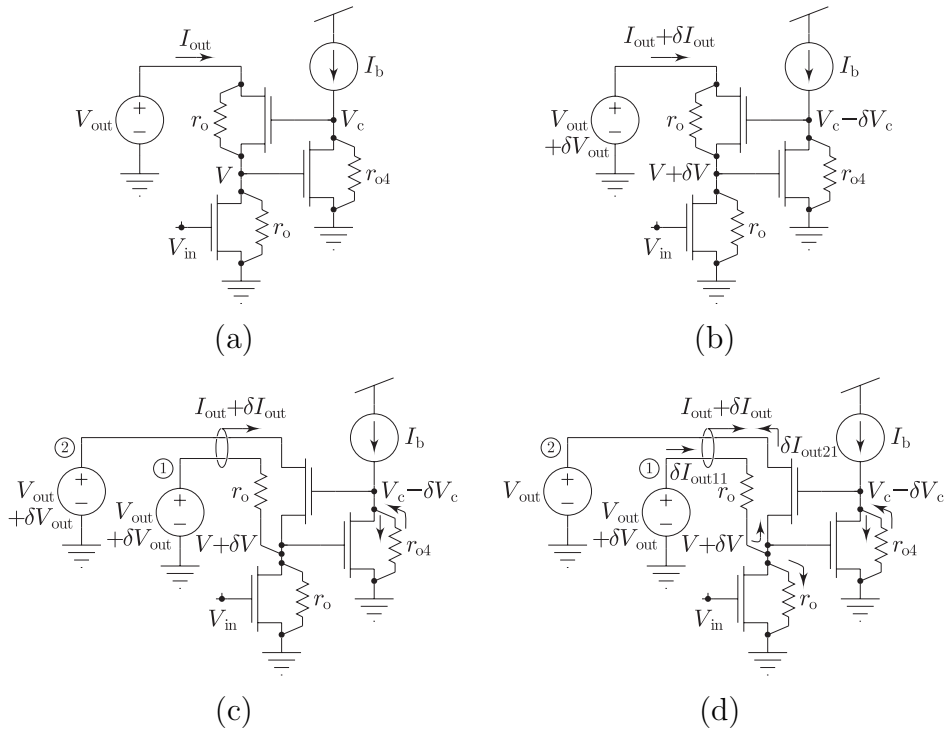


Figure 14: Calculation of the incremental output resistance of a regulated cascode.

$$
\begin{aligned}
&= \frac{\delta V_{\text{out}}}{r_{\text{o}} + (1/G_{\text{S}} \| r_{\text{o}})} \cdot \frac{1/r_{\text{o}}}{G_{\text{S}} + (1/r_{\text{o}})} \\
&= \frac{\delta V_{\text{out}}}{r_{\text{o}} + (1/G_{\text{S}} \| r_{\text{o}})} \cdot \frac{1}{G_{\text{S}} r_{\text{o}} + 1},
\end{aligned}
$$

where G_{S} again denotes the effective incremental conductance looking into the source of M_3. As with the Wilson mirror, the incremental conductance looking into the source of M_3 is not simply g_{s}, because its gate voltage, V_{c}, also changes as V changes by δV.

As we did with the Wilson mirror, to compute G_{S}, we can recursively apply voltage-source splitting and superposition on the relevant part of the circuit, as shown in Fig. 15a and Fig. 15b. Each of the two replica test voltage sources elicits a single nonzero component of the current flowing into the source of M_3, I_{S}, as shown in Fig. 15c and Fig. 15d. By inspection of these circuits, we can write δI_{S} as

$$
\begin{aligned}
\delta I_{\text{S}} &= \underbrace{-g_{\text{m}} \underbrace{(-g_{\text{m4}} r_{\text{o4}} \delta V)}_{\delta V_{\text{c}}}}_{\delta I_{\text{S21}}} + \underbrace{g_{\text{s}} \delta V}_{\delta I_{\text{S22}}} \\
&= g_{\text{s}} \left(\kappa g_{\text{m4}} r_{\text{o4}} + 1\right) \delta V,
\end{aligned}
$$

whence it follows that

$$
G_{\text{S}} = \frac{\delta I_{\text{S}}}{\delta V} = g_{\text{s}} \left(\kappa g_{\text{m4}} r_{\text{o4}} + 1\right) \approx \left(g_{\text{m4}} r_{\text{o4}}\right) g_{\text{m}},
$$

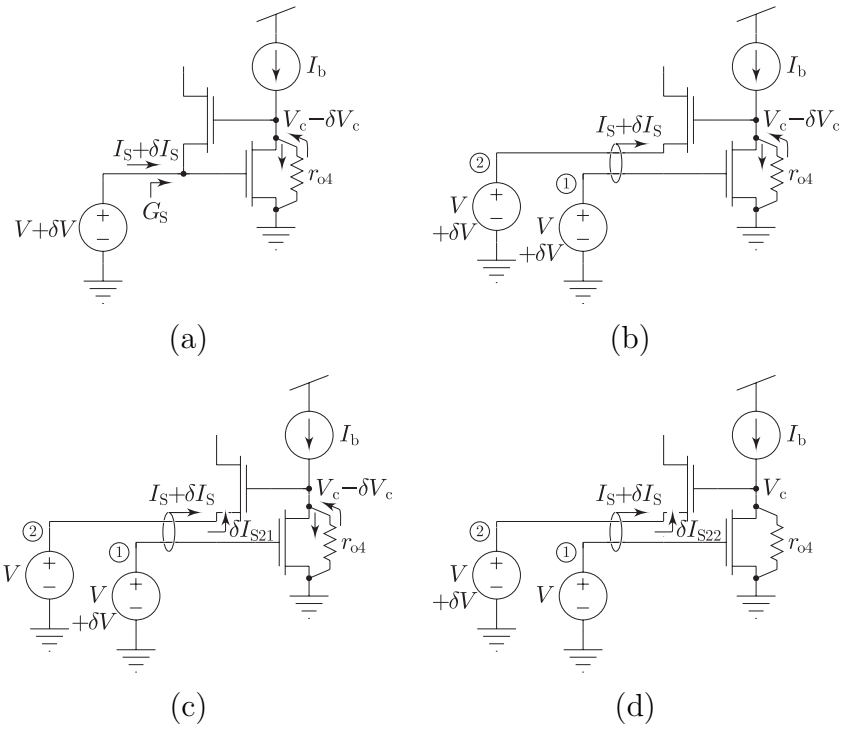


Figure 15: Auxiliary calculation of the incremental source conductance of M_3 including the effect of the changing cascode bias voltage.

where the approximation follows from $g_{m4}r_{o4} \gg 1$. Using this result, we can write the output resistance of the circuit of Fig. 13 as

$$\begin{aligned} R_{out} &= \frac{\delta V_{out}}{\delta I_{out}} \\ &= \left(r_o + \left(\frac{1}{G_S} \Big\| r_o\right)\right)(G_S r_o + 1) \\ &\approx \left(r_o + \left(\frac{1}{g_m} \cdot \frac{1}{g_{m4}r_{o4}} \Big\| r_o\right)\right)(g_m r_o \cdot g_{m4} r_{o4} + 1) \\ &\approx r_o \cdot g_m r_o \cdot g_{m4} r_{o4}, \end{aligned}$$

which is larger than the output resistance of a single transistor by a factor of the product of the intrinsic gain factors of transistors M_3 and M_4. ∎

7 Incremental Voltage Gain Calculation of CMOS Circuits by Node Fixing

In this section, we shall illustrate the node fixing technique, which we developed earlier in the semester, for calculating the incremental voltage gain of CMOS circuits with several worked examples.

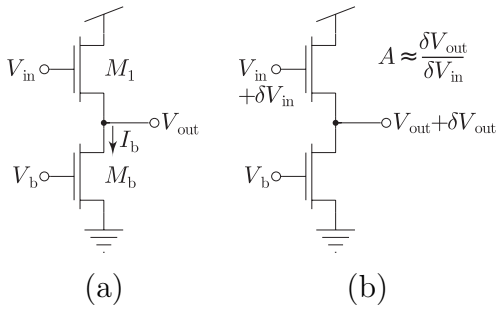


Figure 16: Source follower circuit.

For our first example of incremental gain calculation by node fixing, we shall compute the incremental voltage gain of an nMOS source follower, shown in Fig. 16. For this calculation, we shall assume that both transistors are matched. Further, we shall assume that V_{in} is far enough above ground that transistor M_{b} is saturated and that V_{in} cannot exceed V_{DD}. Under these assumptions, M_1 (i.e., the source-follower transistor) will always be saturated in this circuit. To see why, we note that the drain of the source-follower transistor is connected to V_{DD}. The smallest value that the V_{DS} of M_1 reaches for any value of I_{b} is achieved when V_{in} is equal to V_{DD}. Thus, if M_1 is saturated for this value of V_{DS}, it must be saturated for all other values of V_{in}, too. However, when V_{in} is equal to V_{DD}, both the gate and drain are at the same potential, which is equivalent to M_1 being diode connected. Because the diode-connected transistor operates in saturation for all appreciable current levels, then so will transistor M_1. Both transistors pass the same current, so both transistors will have the same small-signal parameter values. The output voltage will be just far enough below V_{in} that the saturation current of M_1 is equal to I_{b}.

Example 7.1

We begin by connecting a test voltage source to the output of the circuit whose value we have adjusted to match the quiescent output voltage, as shown in Fig. 17a. At this point, the circuit exchanges no current with the test source, as shown in Fig. 17b. We can compute the incremental output resistance of this circuit, as shown in Fig. 17c, by increasing V_{out} by δV_{out} and determining how much current flows into the circuit. Assuming that $g_{\text{s}} r_{\text{o}} \gg 1$, neither Early-effect resistor will have an impact on the value of V_{out}, because they both appear in parallel with the incremental source conductance of M_1. In this case, the incremental output resistance is simple enough that we should not need to use voltage source splitting and superposition—its value is simply given by

$$R_{\text{out}} = \frac{1}{g_{\text{s}}}.$$

To compute the incremental transconductance gain of the circuit, we restore the test source back to its original value and increase V_{in} by δV_{in}. Under these circumstances, the current in M_1 will increase by

$$\delta I_1 = g_{\text{m}} \delta V_{\text{in}},$$

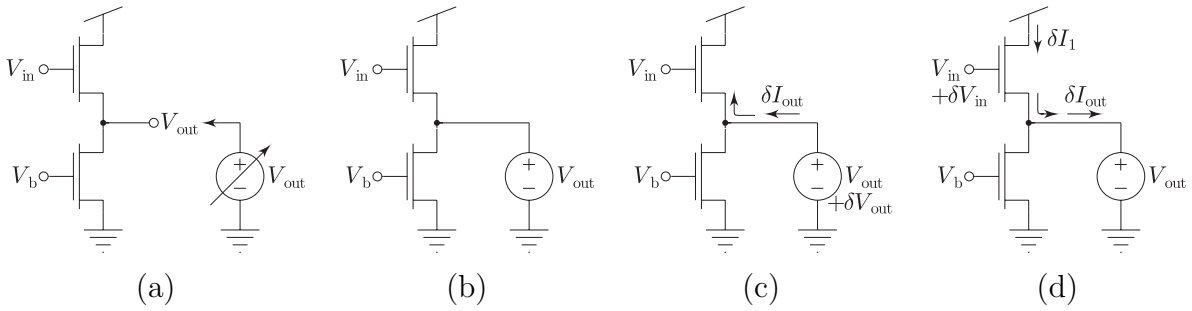


Figure 17: Calculation of the incremental voltage gain of the source follower by node fixing.

which all flows into the output test source, so

$$\delta I_{\rm out} = \delta I_1 = g_{\rm m}\delta V_{\rm in},$$

which implies that

$$G_{\rm m} = \frac{\delta I_{\rm out}}{\delta V_{\rm in}} = g_{\rm m}.$$

Thus, the incremental gain of the source follower is given by

$$A = \frac{\delta V_{\rm out}}{\delta V_{\rm in}} = G_{\rm m}R_{\rm out} = g_{\rm m} \cdot \frac{1}{g_{\rm s}} = \kappa,$$

which is what we found earlier in the course by finding $V_{\rm out}$ as a function of $V_{\rm in}$ and differentiating the resulting expression. ∎

For our next example, we shall calculate the incremental voltage gain of an improved version of the source follower, called the *super source follower*, which is shown in Fig. 18. To the simple source follower of Fig. 16, we add two pMOS transistors, which provide negative feedback that serves to reduce the incremental output resistance of the circuit over that of the simple source follower. For this calculation, we shall assume that all three nMOS transistors are matched and that both pMOS transistors are matched. We shall also assume that $V_{\rm in}$ is sufficiently far above ground that $M_{2\rm a}$ and $M_{2\rm b}$ are both saturated and that $V_{\rm in}$ cannot exceed $V_{\rm DD}$. We shall also assume that $V_{{\rm b}n}$ has been set so that the saturation currents of $M_{2\rm a}$ and $M_{2\rm b}$ are $I_{\rm b}$ and that $V_{{\rm b}p}$ has been set so that the saturation current of M_3 is also $I_{\rm b}$.

Let us start by assuming all of the transistors in the circuit are saturated. In the steady state, KCL implies that the current flowing through M_1 must equal that flowing through M_3. If M_3 operates in saturation, then this current would be $I_{\rm b}$. Moreover, if the current flowing through M_1 is $I_{\rm b}$, then KCL implies that the current flowing through M_4 must also equal $I_{\rm b}$, because a total of $2I_{\rm b}$ is sunk by the nMOS bias transistors. If M_4 is saturated and if its Early effect were not too severe, then its gate voltage, V, would have to be nearly equal to $V_{{\rm b}p}$ in order for it to pass a current of $I_{\rm b}$. From this, we can conclude that M_3 must be saturated, because its gate and drain voltages are nearly equal, making it effectively diode connected. Moreover, in order for transistor M_1 to pass $I_{\rm b}$, it must have a finite positive $V_{\rm DS}$, which implies that V must be greater than $V_{\rm out}$. This fact, in turn, implies that M_4 has

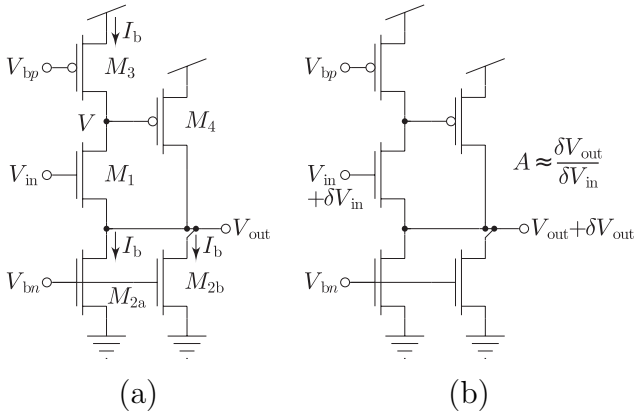


Figure 18: Super source follower circuit.

a larger $V_{\rm SD}$ than does M_3. Therefore, if M_3 is guaranteed to be saturated, then so is M_4. Transistors $M_{2\rm a}$ and $M_{2\rm b}$ are saturated by hypothesis, leaving us to consider whether or not transistor M_1 will be saturated.

If M_1 were saturated, then using the EKV model and equating the saturation currents of M_1 and $M_{2\rm a}$, we can show that

$$V_{\rm out} = \kappa_n \left(V_{\rm in} - V_{{\rm b}n} \right),$$

regardless of whether $V_{{\rm b}n} < V_{\rm T0}$, $V_{{\rm b}n} \approx V_{\rm T0}$, or $V_{{\rm b}n} > V_{\rm T0}$, just like for the simple source follower. Of course, from this result, we can compute the incremental gain of the super source follower directly by differentiating $V_{\rm out}$ with respect to $V_{\rm in}$. Nevertheless, we shall proceed to calculate the incremental gain of this circuit by node fixing in order to illustrate the technique. Now, in order for M_1 to be saturated, we must have that

$$V_{\rm DS} = V - V_{\rm out} = V_{{\rm b}p} - \kappa_n \left(V_{\rm in} - V_{{\rm b}n} \right) \geq V_{\rm DSsat},$$

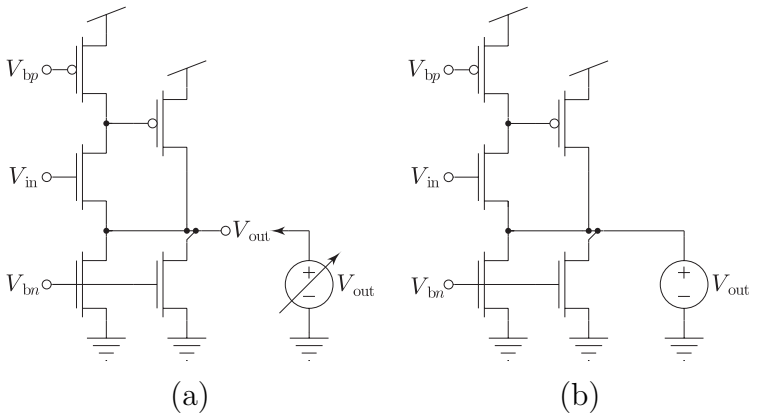


Figure 19: Fixing the output voltage of the super source follower.

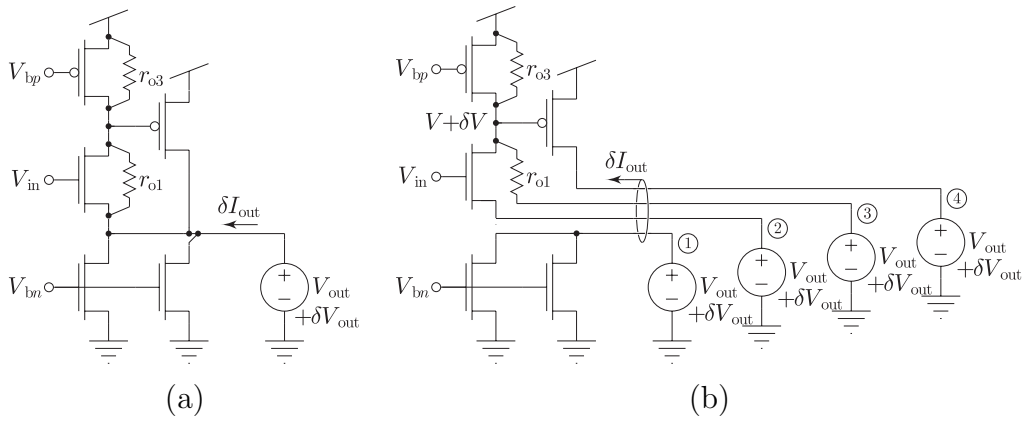


Figure 20: Calculation of the incremental output resistance of the super source follower with no applied input signal by voltage source splitting.

which translates into an upper limit on $V_{\rm in}$ given by

$$V_{\rm in} \leq V_{{\rm b}n} + \frac{V_{{\rm b}p} - V_{\rm DSsat}}{\kappa_n}.$$

For typical values of $V_{{\rm b}n}$, $V_{{\rm b}p}$, and κ_n, this upper limit exceeds $V_{\rm DD}$, which we supposed to be the upper limit on $V_{\rm in}$. Thus, under most circumstances, M_1 will operate in saturation and the quiescent output voltage will be given by the expression that we just obtained for $V_{\rm out}$.

Example 7.2

We begin by connecting a test voltage source to the output of the circuit whose value we have adjusted to match the quiescent output voltage, as shown in Fig. 19a. At this point, the circuit exchanges no current with the test source, as shown in Fig. 18b. We can compute the incremental output resistance of this circuit, as shown in Fig. 20a, by increasing $V_{\rm out}$ by $\delta V_{\rm out}$ and determining how much current flows into the circuit. As with the simple source follower, assuming that $g_{\rm s} r_{\rm o} \gg 1$, we should expect that the Early-effect resistors of $M_{2{\rm a}}$, $M_{2{\rm b}}$, and M_4, will not have a large impact on the value of $R_{\rm out}$, because they both appear in parallel with the incremental source conductance of M_1, which is saturated under most conditions, so we shall not include these in the calculation. We shall, however, include the Early-effect resistors of transistors M_1 and M_3, as shown in Fig. 20a, because if we were not to include these, there would be no place for a change in the current in M_1 to go when it gets to node V. Otherwise a change in this current, no matter how small, would drive either M_1 or M_3 into the ohmic region, depending on whether the current in M_1 increased or decreased.

Next, we split $V_{\rm out}$ into four replica sources, as shown in Fig. 20b. For convenience, we have left the drains of $M_{2{\rm a}}$ and $M_{2{\rm b}}$ tied together. Because their gate voltages are tied to a constant potential and they are saturated, they will not impact the calculation of $R_{\rm out}$. We shall compute each of the components of $\delta I_{\rm out}$ due to each of the replica test sources individually and assemble them into the total $\delta I_{\rm out}$ using superposition. The only nonzero

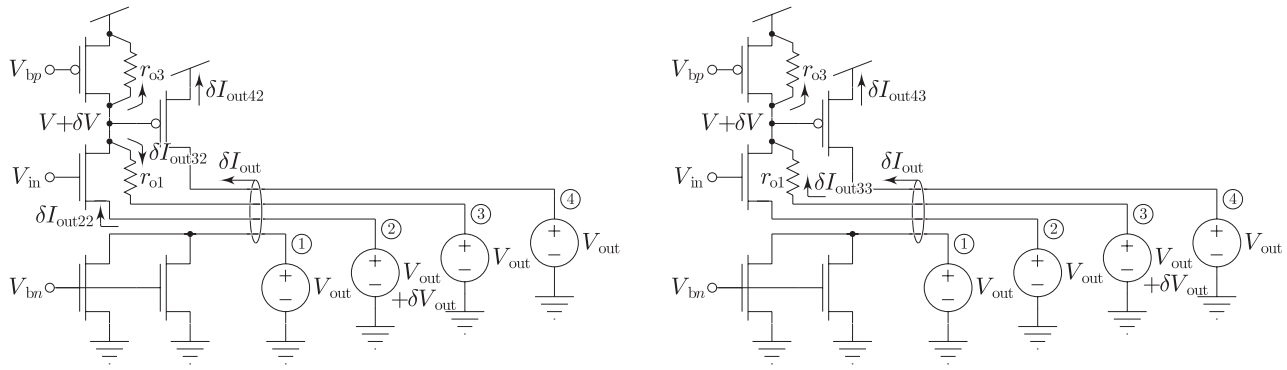


Figure 21: The only nonzero components of δI_{out} occur when we apply δV_{out} to the replica sources on (a) branch 2 and (b) branch 3.

components of δI_{out} occur when we change the value of the replica sources on branches 2 and 3, as shown in Fig. 21a and Fig. 21b. By inspection of these circuits, we can write the total output current as

$$\begin{aligned}
\delta I_{\text{out}} &= \underbrace{g_{\text{s1}}\delta V_{\text{out}}}_{\delta I_{\text{out22}}}\left(1-\underbrace{\frac{r_{\text{o3}}}{r_{\text{o1}}+r_{\text{o3}}}}_{\delta I_{\text{out32}}/\delta I_{\text{out22}}}\right)+g_{\text{m4}}\Bigg(\underbrace{\underbrace{g_{\text{s1}}\delta V_{\text{out}}}_{\delta I_{\text{out22}}}\left(r_{\text{o1}}\|r_{\text{o3}}\right)}_{\delta V}\Bigg)}_{\delta I_{\text{out42}}} \\
&\qquad +\underbrace{\frac{\delta V_{\text{out}}}{r_{\text{o1}}+r_{\text{o3}}}}_{\delta I_{\text{out33}}}+\underbrace{g_{\text{m4}}\cdot\underbrace{\frac{r_{\text{o3}}}{r_{\text{o1}}+r_{\text{o3}}}\cdot\delta V_{\text{out}}}_{\delta V}}_{\delta I_{\text{out43}}} \\
&= g_{\text{s1}}\delta V_{\text{out}}\left(\frac{r_{\text{o1}}}{r_{\text{o1}}+r_{\text{o3}}}+g_{\text{m4}}\left(r_{\text{o1}}\|r_{\text{o3}}\right)\right)+\frac{r_{\text{o3}}}{r_{\text{o1}}+r_{\text{o3}}}\cdot\delta V_{\text{out}}\left(\frac{1}{r_{\text{o3}}}+g_{\text{m4}}\right) \\
&= g_{\text{s1}}\left(r_{\text{o1}}\|r_{\text{o3}}\right)\delta V_{\text{out}}\left(\frac{1}{r_{\text{o3}}}+g_{\text{m4}}\right)+\frac{r_{\text{o1}}\|r_{\text{o3}}}{r_{\text{o1}}}\cdot\delta V_{\text{out}}\left(\frac{1}{r_{\text{o3}}}+g_{\text{m4}}\right) \\
&= \left(r_{\text{o1}}\|r_{\text{o3}}\right)\left(\frac{1}{r_{\text{o3}}}+g_{\text{m4}}\right)\left(g_{\text{s1}}+\frac{1}{r_{\text{o1}}}\right)\delta V_{\text{out}} \\
&\approx g_{\text{s1}}g_{\text{m4}}\left(r_{\text{o1}}\|r_{\text{o3}}\right)\delta V_{\text{out}},
\end{aligned}$$

where the approximation follows from the fact that $g_{\text{s1}}r_{\text{o1}} \gg 1$ and that $g_{\text{m3}}r_{\text{o4}} \gg 1$. Transistors M_3 and M_4 are matched and carrying the same quiescent current, so their g_{m} and r_{o} values will be equal, so if $g_{\text{m3}}r_{\text{o3}} \gg 1$ and $g_{\text{m4}}r_{\text{o4}} \gg 1$ then it also follows that $g_{\text{m3}}r_{\text{o4}} \gg 1$. Thus, the incremental output resistance of the circuit is given by

$$R_{\text{out}} = \frac{\delta V_{\text{out}}}{\delta I_{\text{out}}} = \frac{1}{g_{\text{s1}}}\cdot\frac{1}{g_{\text{m4}}\left(r_{\text{o1}}\|r_{\text{o3}}\right)} \ll \frac{1}{g_{\text{s1}}},$$

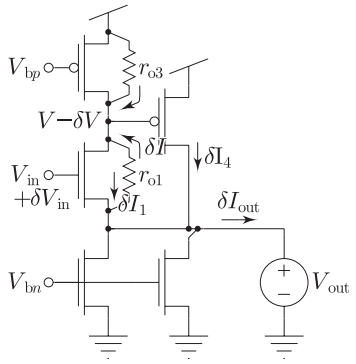


Figure 22: Calculation of the incremental transconductance gain of the super source follower with the output voltage fixed.

which was the incremental output resistance of the simple source follower. Note that this result also validates our assumption that the Early-effect resistors of M_{2a}, M_{2b}, and M_4 would have a negligible impact on the calculation, because they would have appeared in parallel with this very small output resistance.

Next, we must determine the incremental transconductance gain of the circuit from input to output with the output voltage fixed, as shown in Fig. 22.

$$\begin{aligned}
\delta I_{out} &= \underbrace{g_{m1}\delta V_{in}}_{\delta I_1}\left(1-\frac{r_{o3}}{\underbrace{r_{o1}+r_{o3}}_{\delta I/\delta I_1}}\right)+g_{m4}\underbrace{\left(\underbrace{g_{m1}\delta V_{in}}_{\delta I_1}\left(r_{o1}\|r_{o3}\right)\right)}_{\delta V}}_{\delta I_4} \\
&= g_{m1}\delta V_{in}\left(\frac{r_{o1}}{r_{o1}+r_{o3}}+g_{m4}\left(r_{o1}\|r_{o3}\right)\right) \\
&= g_{m1}\left(r_{o1}\|r_{o3}\right)\delta V_{in}\left(\frac{1}{r_{o3}}+g_{m4}\right) \\
&\approx g_{m1}g_{m4}\left(r_{o1}\|r_{o3}\right)\delta V_{in},
\end{aligned}$$

where the approximation follows from the fact that $g_{m4}r_{o3} \gg 1$, as we just argued was the case. Thus, we have that the incremental transconductance gain of the circuit is given by

$$G_m = \frac{\delta I_{out}}{\delta V_{in}} \approx g_{m1}g_{m4}\left(r_{o1}\|r_{o3}\right),$$

so the incremental voltage gain of the circuit is given by

$$A = \frac{\delta V_{out}}{\delta V_{in}} = G_m R_{out} = \frac{g_{m1}g_{m4}\left(r_{o1}\|r_{o3}\right)}{g_{s1}g_{m4}\left(r_{o1}\|r_{o3}\right)} = \frac{g_{m1}}{g_{s1}} = \kappa_n,$$

which is what we would have found originally by differentiating V_{out} with respect to V_{in}. ∎

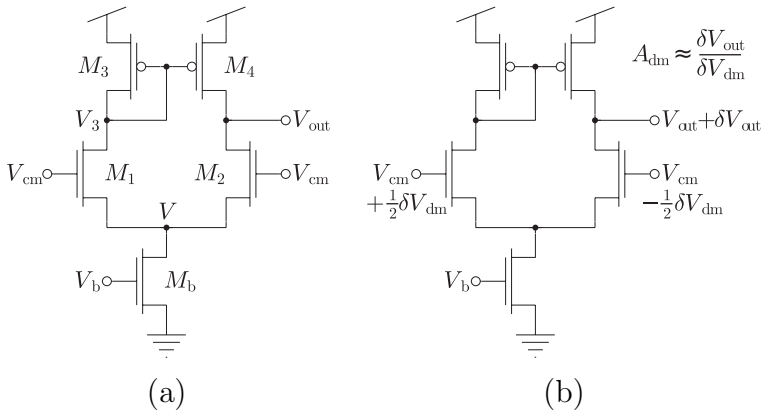


Figure 23: Simple differential amplifier circuit.

For our next example, we shall calculate the incremental differential-mode voltage gain of the simple five-transistor differential amplifier, shown in Fig. 23. For this calculation, we shall assume that all three nMOS transistors are matched, that the pMOS transistors are matched, and that $V_{\rm cm}$ is high enough to ensure that the bias transistor operates in saturation. Also, we shall assume that M_1 always operates in saturation, which will usually be the case. Because M_3 is diode connected, the question of whether or not M_1 is saturated is very similar to the one we addressed for M_1 in the super source follower example. We would like to determine what the quiescent output voltage of the circuit shall be under these conditions in order to decide whether or not M_2 and M_4 will operate in saturation. If there were no Early effect, the output voltage would be indeterminate for this circuit, because any value of $V_{\rm out}$ for which both M_2 and M_4 are saturated will satisfy KCL. To determine the actual quiescent output voltage, we must consider the Early effect in our reasoning process.

We know that the sources of M_1 and M_2 are tied together and that their gates are at the same potential; thus, they operate on the same drain characteristic. If one of these transistors has a larger voltage across it, it will be biased further into saturation and, because of the Early effect, will have a larger channel current. The only point at which both transistors will pass the same current is the one at which they have the same drain-to-source voltage. Likewise, the gates of M_3 and M_4 are tied together as are their sources, which means that they too operate on the same drain characteristic. Consequently, the one with the larger voltage across it must also pass a larger channel current and the only point at which their channel currents are equal is that at which they have equal source-to-drain voltages.

Because M_3 is diode connected, we know that V_3 will adjust itself so that the current flowing through M_1 is equal to that flowing through M_3 in the steady state. Now, if $V_{\rm out}$ were larger than V_3, then M_2 would have more voltage across it than would M_1, and we know that the current flowing through M_2 would exceed that flowing through M_1. Under these circumstances, we also know that M_4 would have less voltage across it than would M_3, which means that the current flowing through M_4 would be less than that flowing through M_3. Therefore, if $V_{\rm out}$ were higher than V_3, M_2 would be sinking more current from the output node than M_4 would be supplying and $V_{\rm out}$ would have to decrease as the output node is discharged, reducing the difference between $V_{\rm out}$ and V_3. On the other hand, if $V_{\rm out}$

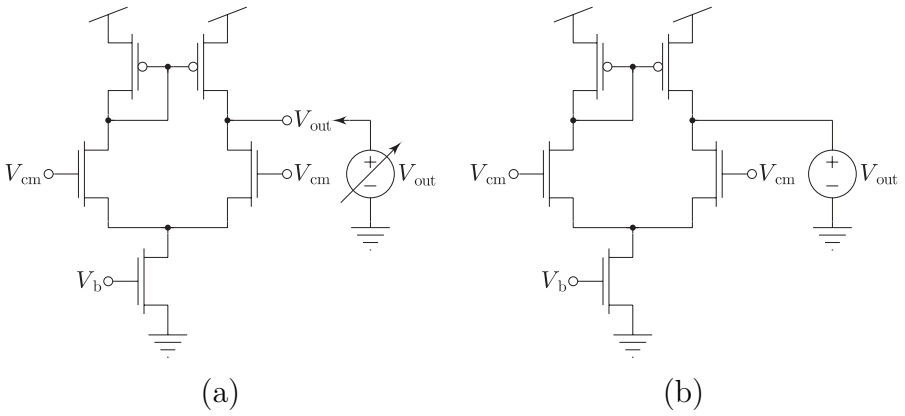


Figure 24: Fixing the output voltage of the simple differential amplifier.

were lower than V_3, M_2 would have less voltage across it than would M_1 and, thus, M_2 would be passing less current than M_1. Also, M_4 would have more voltage across it than would M_3, so M_4 would be passing a larger current than M_3. Consequently, M_4 would be passing a larger current than M_2. Thus, if V_{out} were lower than V_3, M_4 would be sourcing more current onto the output node than M_2 would be sinking, and V_{out} would increase, again reducing the difference between V_{out} and V_3. So, we have that if V_{out} were different from V_3, that situation would not persist, and V_{out} would eventually become equal to V_3. Now, if M_1 is saturated, then so is M_2, because they each have the same drain-to-source voltage. Likewise, if M_3 is saturated, then so is M_4. So, M_2 and M_4 both operate in saturation under these circumstances.

Example 7.3

We begin the node-fixing process by connecting a test voltage source to the output of

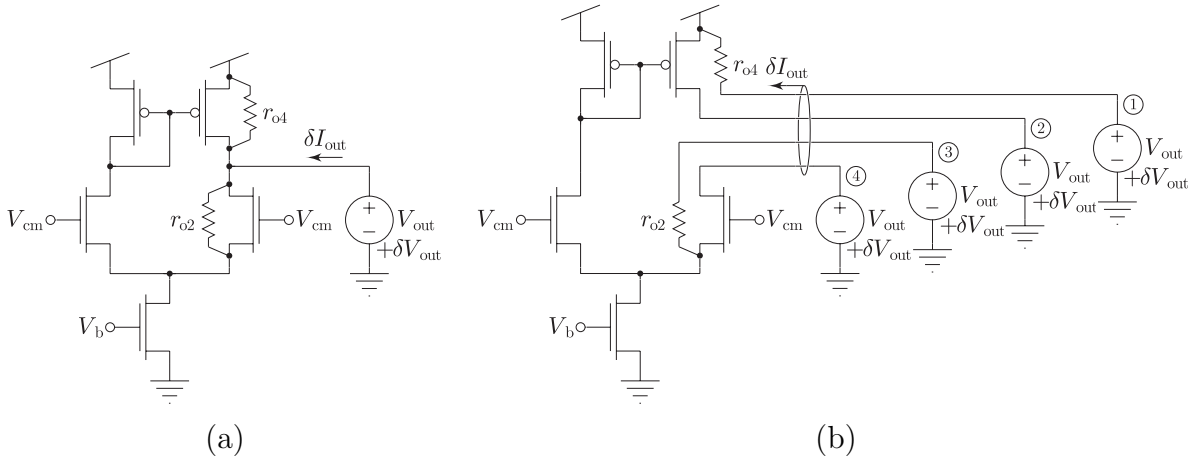


Figure 25: Calculation of the incremental output resistance of the differential amplifier with no applied input signal by voltage source splitting.

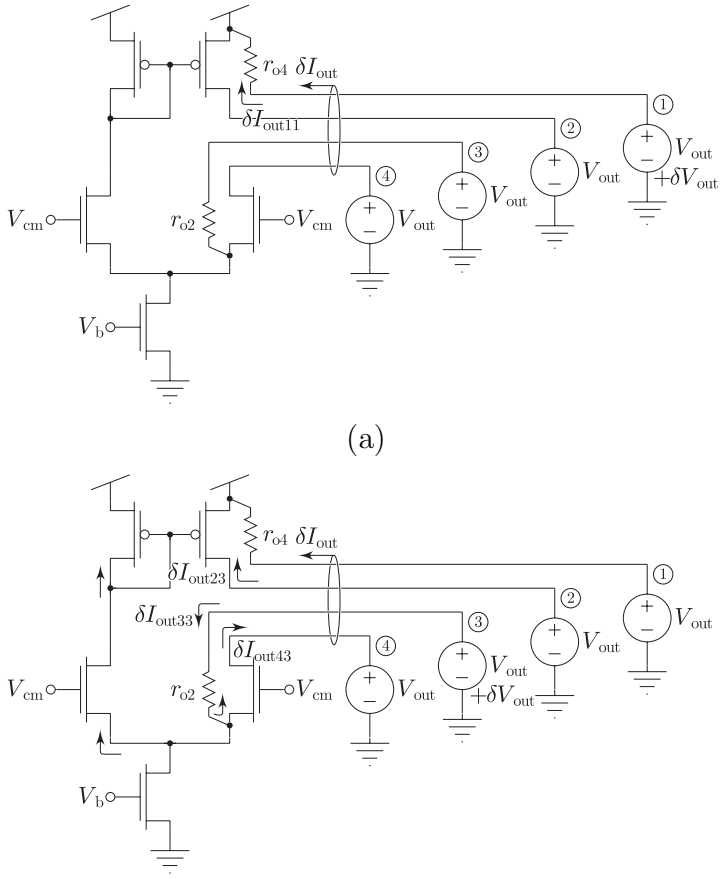


Figure 26: The only nonzero components of δI_{out} occur when we apply δV_{out} to the replica sources on (a) branch 1 and (b) branch 3.

the circuit whose value we have adjusted to match the quiescent output voltage, which we have just established is equal to the value of V_3, as shown in Fig. 24a. At this point, the circuit exchanges no current with the test source, as shown in Fig. 24b. We can compute the incremental output resistance of this circuit, as shown in Fig. 25a, by increasing V_{out} by δV_{out} and determining how much current flows into the circuit. Because M_2 and M_4 are both saturated and their drains are the only things connected to the output node, we must include Early-effect resistors for these transistors, as shown in Fig. 25a, in our calculation of the amplifier's output resistance, otherwise we should conclude that the output resistance, and, therefore, the circuit's differential-mode gain is infinite. All of the other Early-effect resistors would appear in parallel with device terminals which have a comparably high incremental conductance, which means that the Early-effect resistors would shunt away a negligible amount of current from these other terminals, and, therefore, we should expect that they will have a negligible effect on the calculation.

Next, we split V_{out} into four replica sources, as shown in Fig. 25b. We shall compute each of the components of δI_{out} due to each of the replica test sources individually and assemble

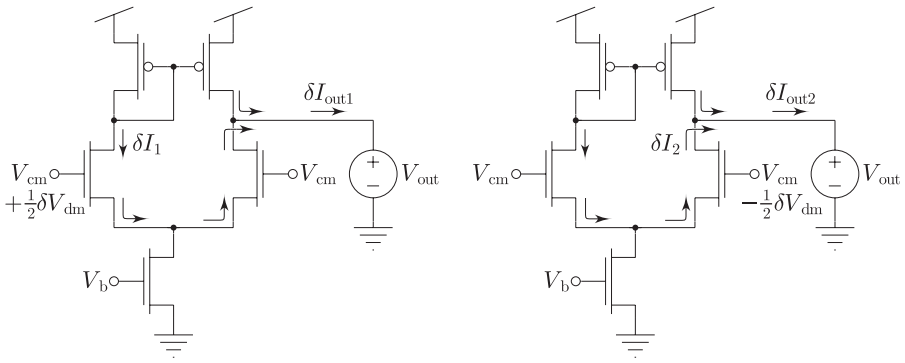


Figure 27: Calculation of the incremental transconductance gain of the simple differential amplifier with the output voltage fixed by superposition.

them into the total δI_{out} using superposition. The only nonzero components of δI_{out} occur when we change the value of the replica sources on branches 1 and 3, as shown in Fig. 26a and Fig. 26b. By inspection of these circuits, we can write the total output current as

$$\begin{aligned}
\delta I_{\text{out}} &= \underbrace{\frac{\delta V_{\text{out}}}{r_{\text{o4}}}}_{\delta I_{\text{out11}}} + \underbrace{\frac{\delta V_{\text{out}}}{r_{\text{o2}} + (1/g_{\text{s1}} \| 1/g_{\text{s2}})}}_{\delta I_{\text{out33}}} \left(1 - \underbrace{\frac{g_{\text{s2}}}{g_{\text{s1}} + g_{\text{s2}}}}_{\delta I_{\text{out43}}/\delta I_{\text{out33}}} + \overbrace{\frac{g_{\text{s1}}}{g_{\text{s1}} + g_{\text{s2}}}}^{\delta I_{\text{out23}}/\delta I_{\text{out33}}} \right) \\
&= \frac{\delta V_{\text{out}}}{r_{\text{o4}}} + \frac{\delta V_{\text{out}}}{r_{\text{o2}} + (1/2g_{sn})} \left(1 - \frac{g_{sn}}{2g_{sn}} + \frac{g_{sn}}{2g_{sn}} \right) \\
&\approx \frac{\delta V_{\text{out}}}{r_{\text{o4}}} + \frac{\delta V_{\text{out}}}{r_{\text{o2}}},
\end{aligned}$$

where we have made use of the fact that, at the quiescent operating point, $g_{\text{s1}} = g_{\text{s2}} = g_{sn}$, because M_1 and M_2 are matched and both have a quiescent channel current of $I_{\text{b}}/2$, and the approximation follows from the fact that $g_{\text{s2}} r_{\text{o2}} \gg 1$. Thus, the incremental output resistance of the circuit is given approximately by

$$R_{\text{out}} = \frac{\delta V_{\text{out}}}{\delta I_{\text{out}}} \approx r_{\text{o2}} \| r_{\text{o4}}.$$

Next, we must determine the incremental transconductance gain of the circuit from input to output with the output voltage fixed, as shown in Fig. 27. Because the output voltage source maintains the voltage across r_{o4} constant, the current flowing through it will not change for this calculation, so it will have no impact on the calculation whatsoever. Because the source conductances of M_1 and M_2 are much larger than $1/r_{\text{o2}}$, any current diverted by r_{o2} from the sources of M_1 and M_2 would represent a negligible loss from that which flows into the sources of M_1 and/or M_2, so we would expect it too to have a negligible impact on this calculation. Consequently, we shall omit both in calculating the circuit's incremental transconductance gain, as shown in Fig. 27. Also, as indicated in Fig. 23b, we

shall apply a pure differential-mode input to the circuit for this calculation, which means that we apply half of $\delta V_{\rm dm}$ to the noninverting input and half of $\delta V_{\rm dm}$ to the inverting input so that the common-mode input voltage remains unchanged. To compute $\delta I_{\rm out}$, we shall apply superposition, considering the effect of each half of $\delta V_{\rm dm}$ separately and superposing the resulting components of $\delta I_{\rm out}$, as shown in Fig. 27.

First, we consider increasing the gate of M_1 by $\delta V_{\rm dm}/2$, as shown in Fig. 27a. This increase in the gate voltage of M_1 results in an increase in its channel current, δI_1, given by

$$\delta I_1 = \frac{g_{\rm m1}\delta V_{\rm dm}/2}{1 + g_{\rm s1}\,(1/g_{\rm s2})} = \frac{g_{\rm mn}}{4} \cdot \delta V_{\rm dm},$$

where we have again made use of the fact that the incremental source conductances and transconductance gains of M_1 and M_2 are equal to one another under quiescent conditions. Now, this incremental current flowing into the drain of M_1 also flows out of the gate/drain of M_3 and is reflected to the output by the pMOS current mirror, as shown in Fig. 27a. It also flows out of the source of M_1 and into the the source of M_2 and out of the circuit, as shown. Note that the total current in M_2 still flows from drain to source. By indicating that the incremental current flows up into the source of M_2 is that the total current in M_2 is decreasing relative to its quiescent value. Recall that KCL implies that, in the steady state, the sum of the currents flowing through M_1 and M_2 must equal the bias current $I_{\rm b}$. If the current in M_1 has increased by some amount, the current flowing through M_2 by an equal amount so that their sum remains unchanged. Thus, the first component of the incremental output current is given by

$$\delta I_{\rm out1} = 2\delta I_1 = \frac{g_{\rm mn}}{2} \cdot \delta V_{\rm dm}.$$

Next, we consider decreasing the gate of M_2 by $\delta V_{\rm dm}/2$, as shown in Fig. 27b. This decrease in the gate of M_2 results in a decrease in its channel current, δI_2, whose magnitude is given by

$$\delta I_2 = \frac{g_{\rm m2}\delta V_{\rm dm}/2}{1 + g_{\rm s2}\,(1/g_{\rm s1})} = \frac{g_{\rm mn}}{4} \cdot \delta V_{\rm dm},$$

where we have once again made use of the fact that the incremental source conductances and transconductance gains of M_1 and M_2 are equal to one another under quiescent conditions. This decrease in the current flowing through M_2 again can be thought of as a positive incremental current flowing from source of M_2 to its drain and out of the circuit, as shown in Fig. 27b. This incremental current must come from the source of M_1. It also flows through the channel of M_1 and from the input of the pMOS current mirror, which reflects the current increase to the output through M_4, as shown in Fig. 27b. Thus, the second component of $\delta I_{\rm out}$ is given by

$$\delta I_{\rm out2} = 2\delta I_2 = \frac{g_{\rm mn}}{2} \cdot \delta V_{\rm dm}.$$

Superposing these two components of the output currents, we obtain the total incremental output current as

$$\delta I_{\rm out} = \delta I_{\rm out1} + \delta I_{\rm out2} = g_{\rm mn}\delta V_{\rm dm},$$

which implies that the incremental transconductance gain of the circuit with the output voltage held fixed is given by

$$G_{\rm m} = \frac{\delta I_{\rm out}}{\delta V_{\rm dm}} = g_{\rm mn}.$$

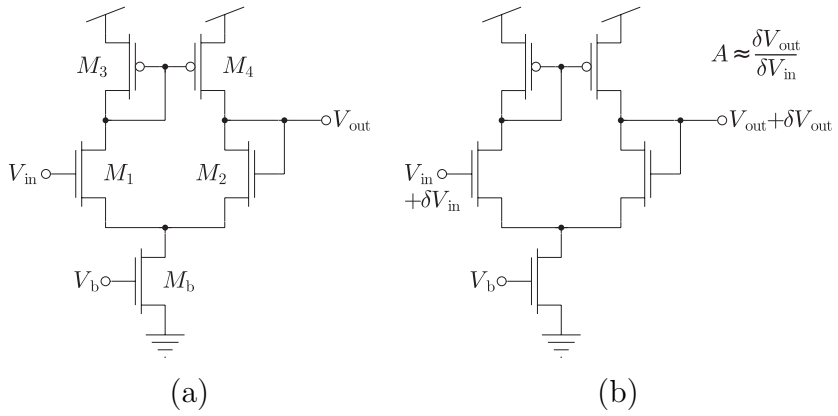


Figure 28: Simple differential amplifier connected as a unity-gain follower.

Therefore, the incremental differential-mode gain of the circuit is given approximately by

$$A_{\text{dm}} = \frac{\delta V_{\text{out}}}{\delta V_{\text{dm}}} = G_{\text{m}} R_{\text{out}} \approx g_{\text{m}n} \left(r_{\text{o}2} \| r_{\text{o}4} \right).$$

■

For our next example, we shall use node fixing to calculate the incremental voltage gain of the simple five-transistor differential amplifier configured as a unity-gain follower with its output connected to its inverting input, as shown in Fig. 28. As with the last example, we shall assume that all three nMOS transistors are matched, that the pMOS transistors are matched, and that V_{in} is high enough to ensure that the bias transistor operates in saturation. Also, we shall assume that M_1 and M_3 operate in saturation for all possible values of V_{in}. In this circuit, M_2 is diode connected and so operates in saturation. Moreover, the output voltage (i.e., the drain/gate of transistor M_2), adjusts itself relative to the common-source node voltage so that M_2 passes the current being supplied by M_4. If M_4 operates in saturation, then this current is a mirror copy of the channel current of M_1. If the Early effect is small, then these currents will be equal. Because M_1 and M_2 are matched and are both operating in saturation, they must have nearly equal gate-to-source voltages if they pass the same channel current. Because their sources are shorted together, nearly equal gate-to-source voltages also translates into nearly equal gate voltages. So, V_{out} will be very nearly equal to V_{in}. The story will be somewhat different if V_{in} is within a saturation voltage of V_{DD}. In this case, M_4 will not be saturated, and so the current flowing M_2 will be smaller than that flowing in M_1, because the current flowing in M_4 will be smaller than that flowing in M_3. However, we shall not consider this case any further in this example. Instead, we shall assume that M_4 operates in saturation and that M_1 and M_2 each carry half of the bias current being sunk by M_{b}.

Example 7.4

We begin the node-fixing process by connecting a test voltage source to the output of the circuit whose value we have adjusted to match the quiescent output voltage, which we have just established is equal to the quiescent value of V_{in}, as shown in Fig. 29a. At this point,

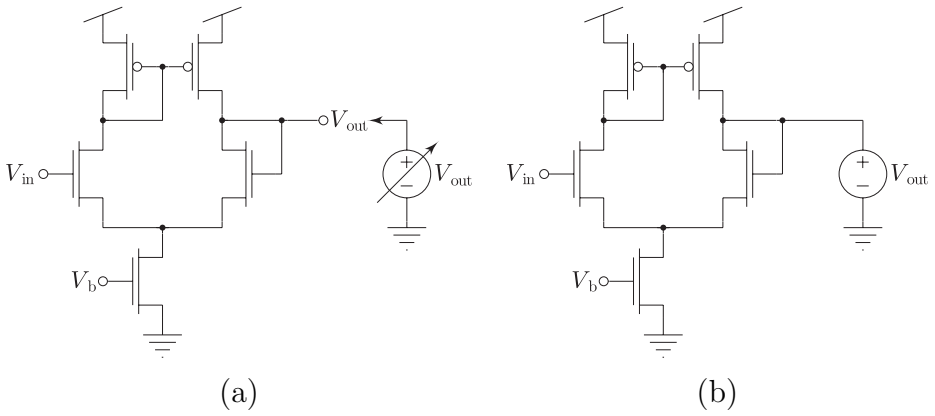


Figure 29: Fixing the output voltage of the follower-connected differential amplifier.

the circuit exchanges no current with the test source, as shown in Fig. 29b. We can compute the incremental output resistance of this circuit, as shown in Fig. 30a, by increasing V_{out} by δV_{out} and determining how much current flows into the circuit. In this case, because we have connected the output back to the inverting input of the amplifier, if we change the output voltage, the amplifier will draw in a relatively large amount of current, which would be on the order of that which flowed out of the differential amplifier when we computed its incremental transconductance gain in the last example. This current would be much larger than that which flowed into the the amplifier due to the Early-effect resistors of M_2 and M_4 when we changed the output voltage in the last example. So, we should expect that the Early-effect resistors of M_2 and M_4 will have a negligible impact on the calculation of the incremental output resistance of the unity-gain follower. To illustrate this point, we shall perform the calculation using source splitting and superposition both without and with these Early-effect resistors.

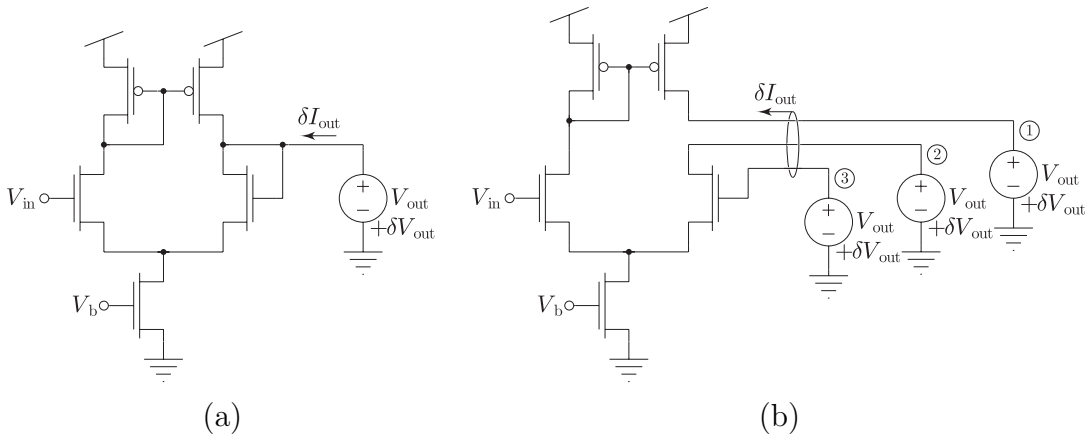


Figure 30: Calculation of the incremental output resistance of the follower-connected differential amplifier with no applied input signal by voltage-source splitting and superposition.

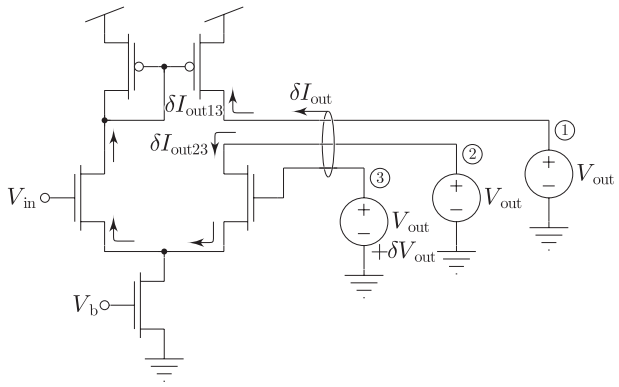


Figure 31: The only nonzero components of δI_{out} occur when we apply δV_{out} to the replica source on branch 3.

Without the Early-effect resistors of M_2 and M_4, we have the situation depicted in Fig. 30a. In this case, we split V_{out} into three replica sources, as shown in Fig. 30b. We shall compute each of the components of δI_{out} due to each of the replica test sources individually and assemble them into the total δI_{out} using superposition. The only nonzero components of δI_{out} occur when we change the value of the replica source on branch 3, as shown in Fig. 31. By inspection of this circuit, we can write the total output current as

$$\delta I_{\text{out}} = \underbrace{\frac{g_{\text{m2}}\delta V_{\text{out}}}{1 + g_{\text{s2}}\,(1/g_{\text{s1}})}}_{\delta I_{\text{out23}}}\,(1+1) = g_{mn}\delta V_{\text{out}},$$

where we have once again made use of the fact that the incremental source conductances and transconductance gains of M_1 and M_2 are equal to one another under quiescent conditions. Note that the first 1 in parentheses accounts for δI_{out23} and the second one accounts for δI_{out13}. In this case, we have that the incremental output resistance of the circuit is given by

$$R_{\text{out}} = \frac{\delta V_{\text{out}}}{\delta I_{\text{out}}} = \frac{1}{g_{mn}}.$$

With the Early-effect resistors of M_2 and M_4, we have the situation shown in Fig. 32a. In this case, we split V_{out} into five replica sources, as shown in Fig. 32b. We shall again compute each of the components of δI_{out} due to each of the replica test sources individually and assemble them into the total δI_{out} using superposition. The only nonzero components of δI_{out} occur when we change the value of the replica sources on branch 1, branch 3, and branch 5, as shown in Fig. 33a, Fig. 33b, and Fig. 33c, respectively. By inspection of these circuits, we can write the total output current as

$$\delta I_{\text{out}} = \underbrace{\frac{\delta V_{\text{out}}}{r_{\text{o4}}}}_{\delta I_{\text{out11}}} + \underbrace{\frac{\delta V_{\text{out}}}{r_{\text{o2}} + (1/g_{\text{s1}} \| 1/g_{\text{s2}})}}_{\delta I_{\text{out33}}} \left(1 - \underbrace{\frac{g_{\text{s2}}}{g_{\text{s1}} + g_{\text{s2}}}}_{\delta I_{\text{out43}}/\delta I_{\text{out33}}} + \overbrace{\frac{g_{\text{s1}}}{g_{\text{s1}} + g_{\text{s2}}}}^{\delta I_{\text{out23}}/\delta I_{\text{out33}}}\right)$$

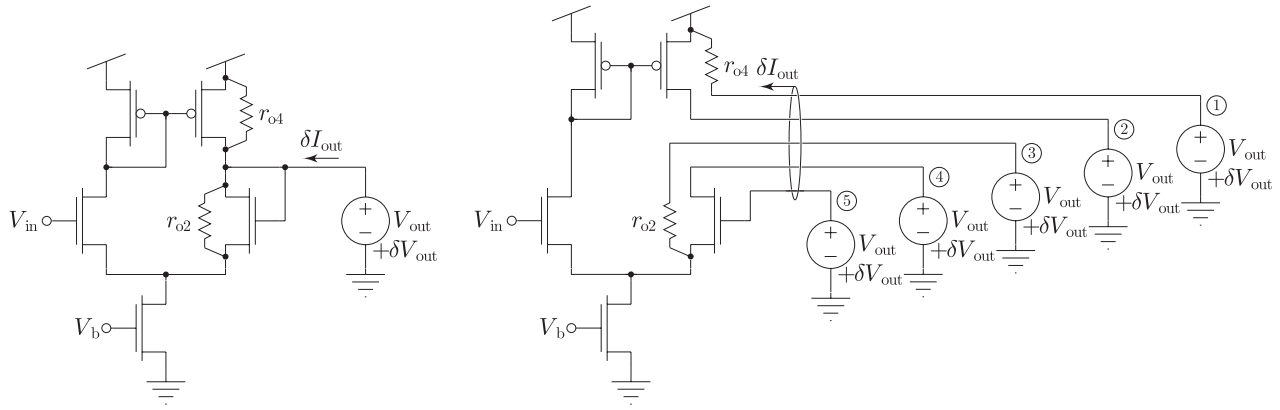


Figure 32: Calculation of the incremental output resistance of the follower-connected differential amplifier with no applied input signal by voltage source splitting including the Early-effect resistors of M_2 and M_4.

$$
\begin{aligned}
& + \underbrace{\frac{g_{m2}\delta V_{out}}{1+g_{s2}\left(1/g_{s1}\|r_{o2}\right)}}_{\delta I_{out45}} \left(1 - \underbrace{\frac{1/r_{o2}}{g_{s1}+1/r_{o2}}}_{\delta I_{out35}/\delta I_{out45}} + \underbrace{\frac{g_{s1}}{g_{s1}+1/r_{o2}}}_{\delta I_{out25}/\delta I_{out45}}\right) \\
= \;& \frac{\delta V_{out}}{r_{o4}} + \frac{\delta V_{out}}{r_{o2}+(1/2g_{sn})}\left(1 - \frac{g_{sn}}{2g_{sn}} + \frac{g_{sn}}{2g_{sn}}\right) + \frac{g_{mn}\delta V_{out}}{1+(g_{sn}/g_{sn})} \cdot \frac{2g_{sn}r_{o2}}{g_{sn}r_{o2}+1} \\
\approx \;& \frac{\delta V_{out}}{r_{o4}} + \frac{\delta V_{out}}{r_{o2}} + g_{mn}\delta V_{out} \\
\approx \;& g_{mn}\delta V_{out},
\end{aligned}
$$

where we again have made use of the fact that incremental source conductances and transconductance gains of M_1 and M_2 are equal to one another under quiescent conditions, and the approximations follow from the fact that $g_{s2}r_{o2} \gg 1$. We have also assumed that $g_{s2}r_{o4} \gg 1$, which will be the case if the Early voltages of the pMOS transistors are not too different from those of the nMOS transistors, because M_2 and M_4 both carry equal quiescent channel currents. Thus, the incremental output resistance of the circuit is given approximately by

$$R_{out} = \frac{\delta V_{out}}{\delta I_{out}} \approx \frac{1}{g_{mn}},$$

which is precisely what we found with substantially less effort when we omitted r_{o2} and r_{o4}.

Next, we must determine the incremental transconductance gain of the circuit from input to output with the output voltage fixed, as shown in Fig. 34. As with the incremental output resistance calculation, none of the Early-effect resistors will matter for this one either. We increase the gate of M_1 by δV_{in}, as shown in Fig. 34. This increase in the gate voltage of M_1 results in an increase in its channel current, δI_1, given by

$$\delta I_1 = \frac{g_{m1}\delta V_{in}}{1+g_{s1}\left(1/g_{s2}\right)} = \frac{g_{mn}}{2} \cdot \delta V_{in},$$

where we have again made use of the fact that the incremental source conductances and transconductance gains of M_1 and M_2 are equal to one another under quiescent conditions. Now, this incremental current flowing into the drain of M_1 also flows out of the gate/drain of M_3 and is reflected to the output by the pMOS current mirror, as shown in Fig. 34. It also flows out of the source of M_1 and into the the source of M_2 and out of the circuit, as shown. Thus, the incremental output current is given by

$$\delta I_{\text{out}} = 2\delta I_1 = g_{\text{m}n}\delta V_{\text{in}},$$

so the incremental voltage gain of the unity-gain follower is given by

$$A = \frac{\delta V_{\text{out}}}{\delta V_{\text{in}}} = G_{\text{m}} R_{\text{out}} = g_{\text{m}n} \cdot \frac{1}{g_{\text{m}n}} = 1.$$

■

For our final example, we shall use the node fixing technique to compute the incremental differential-mode gain of the simplified folded-cascode differential amplifier, shown in Fig. 35. For this calculation, we shall assume that all of the nMOS transistors are matched, that all of the pMOS transistors are matched, and that V_{cm} is sufficiently far above ground that M_{b} operates in saturation. Additionally, we shall assume that the cascode bias voltage, V_{c}, is set low enough that M_3 and M_4 are saturated, but high enough that M_1 and M_2 are saturated for all allowable values of V_{cm}. Transistor M_7 is diode connected, and thus operates in saturation. The question of whether or not M_5 operates in saturation is again very similar to the one that we addressed for M_1 in the super source follower example.

By a similar line of reasoning to that which we followed for the simple five-transistor differential amplifier, the quiescent output voltage of this circuit will be equal to the drain/gate voltage of M_7. When $V_{\text{out}} = V_7$, the currents flowing in M_7 and M_8 will be identical as will be the currents flowing in M_5 and M_6. Also, at this point, if M_5 and M_7 are both saturated under these conditions, then so are M_6 and M_8. If M_5 and M_6 are both saturated and both have the same drain and gate voltage, then their source voltages, V_5 and V_6 must also be equal to one another. Under these conditions, M_1 and M_2 have the same gate, source, and drain voltages, and must therefore be passing the same current. Likewise, M_3 and M_4 have the same gate, source, and drain voltages, and so must also pass the same amount of current. With the circuit in such a state, KCL is satisfied everywhere.

Example 7.5

We begin the node fixing process by connecting a test voltage source to the output of the circuit whose value we have adjusted to match the quiescent output voltage of the amplifier, which we have just established is equal to the value of V_7, as shown in Fig. 36a. At this point, the amplifier exchanges no current with the test source, as indicated in Fig. 35b. We can compute the incremental output resistance of the amplifier, as shown in Fig. 37a, by increasing V_{out} by δV_{out} and determining how much current flows into the circuit as a result. In doing so, we shall account for the Early effect of transistors M_2, M_4, M_6, and M_8, as shown in Fig. 37a. Given that the name *folded cascode* contains the word *cascode*, we might expect that the incremental resistance seen looking into the drain of M_6 (i.e., the cascode transistor connected to the output) would be much larger than that looking into the drain of

M_8, which is the output of a simple nMOS mirror, and hence r_{o8} would dominate the parallel combination of the two. As we shall see, this does turn out to be the case. Nevertheless, we shall proceed with the calculation to illustrate the techniques involved.

To compute δI_{out}, we split V_{out} into four replica sources, as shown in Fig. 37b. We shall compute each of the components of δI_{out} due to each of the replica test sources individually and assemble them into the total δI_{out} by superposition. As shown in Fig. 38a and Fig. 38b, the only nonzero components of δI_{out} occur when we change the value of the replica source on branches 1 and 4. The only component of the output current excited by the voltage change on branch 1 flows into r_{o8}, as shown in Fig. 38a. The voltage change on branch 4 causes current components to flow in branches 2, 3, and 4, as shown in Fig. 38b.

In order to compute how the current components divide at the source of M_6, we need to know the incremental resistance seen looking into the drain of M_2 in parallel with its Early-effect resistor, as shown in Fig. 39a. To determine the equivalent incremental resistance, R_{eq}, indicated in Fig. 39a, we can recursively apply source splitting and superposition, by excising the differential pair from the circuit. Then, we apply a test voltage source to the drain of M_2 whose value is adjusted to match the quiescent drain voltage of M_2 in the original circuit. Finally, we compute the additional current that flows into the drain of M_2 when we change the test voltage source by a small amount. The only nonzero components of δI_2 occur when we change the replica source on branch 2, as shown in Fig. 39b. We can compute the change in I_2 as

$$\begin{aligned}
\delta I_2 &= \underbrace{\frac{\delta V}{r_{o2} + (1/g_{s1} \| 1/g_{s2})}}_{\delta I_{222}} \left(1 - \underbrace{\frac{g_{s2}}{g_{s1} + g_{s2}}}_{\delta I_{212}/\delta I_{222}} \right) \\
&= \frac{\delta V}{r_{o2} + (1/g_{s1} \| 1/g_{s2})} \cdot \frac{g_{s1}}{g_{s1} + g_{s2}} \\
&= \frac{\delta V}{2r_{o2} + 1/g_{sn}},
\end{aligned}$$

if $g_{s1} = g_{s2} = g_{sn}$. Thus, we have that the incremental resistance seen looking into the right side of the differential pair is given by

$$R_{\text{eq}} = \frac{\delta V}{\delta I_2} = 2r_{o2} + 1/g_{sn} \approx 2r_{o2}.$$

With this result, we can write the total current flowing into the output of the amplifier in response to a small change in V_{out} by inspection of the circuits shown in Fig. 38a and Fig. 38b as

$$\begin{aligned}
\delta I_{\text{out}} = \underbrace{\frac{\delta V_{\text{out}}}{r_{o8}}}_{\delta I_{\text{out11}}} + \underbrace{\frac{\delta V_{\text{out}}}{r_{o6} + (1/g_{s6} \| r_{o4} \| 2r_{o2})}}_{\delta I_{\text{out44}}} \Bigg(1 - \underbrace{\frac{g_{s6}}{g_{s6} + 1/r_{o4} + 1/2r_{o2}}}_{\delta I_{\text{out34}}/\delta I_{\text{out44}}} \\
+ \underbrace{\frac{1/2r_{o2}}{g_{s6} + 1/r_{o4} + 1/2r_{o2}}}_{\delta I_{\text{out24}}/\delta I_{\text{out44}}} \Bigg)
\end{aligned}$$

$$
\begin{aligned}
&= \frac{\delta V_{\text{out}}}{r_{\text{o}8}} + \frac{\delta V_{\text{out}}}{r_{\text{o}6} + (1/g_{\text{s}6} \| r_{\text{o}4} \| 2r_{\text{o}2})} \cdot \frac{1/r_{\text{o}4} + 1/r_{\text{o}2}}{g_{\text{s}6} + 1/r_{\text{o}4} + 1/2r_{\text{o}2}} \\
&= \frac{\delta V_{\text{out}}}{r_{\text{o}8}} + \frac{\delta V_{\text{out}}}{r_{\text{o}6} + (1/g_{\text{s}6} \| r_{\text{o}4} \| 2r_{\text{o}2})} \cdot \frac{1}{g_{\text{s}6} (r_{\text{o}2} \| r_{\text{o}4})} \cdot \frac{1}{1 + 1/g_{\text{s}6} (r_{\text{o}4} \| 2r_{\text{o}2})} \\
&\approx \frac{\delta V_{\text{out}}}{r_{\text{o}8}} + \frac{\delta V_{\text{out}}}{g_{\text{s}6} r_{\text{o}6} (r_{\text{o}2} \| r_{\text{o}4})},
\end{aligned}
$$

which means that the incremental output resistance of the folded-cascode amplifier is given approximately by

$$R_{\text{out}} = r_{\text{o}8} \| (g_{\text{s}6} r_{\text{o}6} (r_{\text{o}2} \| r_{\text{o}4})) \approx r_{\text{o}8}.$$

Next, we must determine the incremental transconductance gain of the circuit from input to output with the output voltage fixed, as shown in Fig. 40. Because the output voltage source maintains the voltage across $r_{\text{o}8}$ constant, the current flowing through it will not change for this calculation, so it will have no impact on the calculation whatsoever. Because the source conductances of M_1 and M_2 are much larger than $1/r_{\text{o}2}$, any current diverted by $r_{\text{o}2}$ from the sources of M_1 and M_2 would represent a negligible loss from that which flows into the sources of M_1 and/or M_2, so we would expect it too to have a negligible impact on this calculation. The same can be said for $1/r_{\text{o}4}$ and $1/r_{\text{o}6}$ in comparison to $g_{\text{s}6}$. Consequently, we shall omit all four Early-effect resistors in calculating the circuit's incremental transconductance gain, as shown in Fig. 40. Also, as indicated in Fig. 35b, we shall apply a pure differential-mode input to the circuit for this calculation, which means that we apply half of δV_{dm} to the noninverting input and half of δV_{dm} to the inverting input so that the common-mode input voltage remains unchanged. To compute δI_{out}, we shall apply superposition, considering the effect of each half of δV_{dm} separately and superposing the resulting components of δI_{out}, as shown in Fig. 40.

First, we consider increasing the gate of M_1 by $\delta V_{\text{dm}}/2$, as shown in Fig. 40a. This increase in the gate voltage of M_1 results in an increase in its channel current, δI_1, given by

$$\delta I_1 = \frac{g_{\text{m}1} \delta V_{\text{dm}}/2}{1 + g_{\text{s}1} (1/g_{\text{s}2})} = \frac{g_{\text{m}n}}{4} \cdot \delta V_{\text{dm}},$$

where we have again made use of the fact that the incremental source conductances and transconductance gains of M_1 and M_2 are equal to one another under quiescent conditions. This increase in the current flowing through M_1 results in an equal decrease in the current flowing through M_5, which we can think of as an incremental current flowing out of the source of M_5, as shown in Fig. 40a. In turn, this current flows from the input of the current mirror and is reflected to the output through M_8, as shown in Fig. 40a. The original increase in I_1 also flows back up through M_2 and into the source of M_6 (i.e., the decrease in I_2 is compensated by an equal increase in the current flowing through M_6) and out of the circuit, as shown in Fig. 40a. Thus, the first component of the incremental output current is given by

$$\delta I_{\text{out}1} = 2\delta I_1 = \frac{g_{\text{m}n}}{2} \cdot \delta V_{\text{dm}}.$$

Next, we consider decreasing the gate of M_2 by $\delta V_{\text{dm}}/2$, as shown in Fig. 40b. This decrease in the gate of M_2 results in a decrease in its channel current, δI_2, whose magnitude

is given by

$$\delta I_2 = \frac{g_{\mathrm{m}2}\delta V_{\mathrm{dm}}/2}{1 + g_{\mathrm{s}2}\,(1/g_{\mathrm{s}1})} = \frac{g_{\mathrm{m}n}}{4} \cdot \delta V_{\mathrm{dm}},$$

where we have once again made use of the fact that the incremental source conductances and transconductance gains of M_1 and M_2 are equal to one another under quiescent conditions. This decrease in the current flowing through M_2 again can be thought of as a positive incremental current flowing from source of M_2 to its drain and out of the circuit through M_6, as shown in Fig. 40b. This incremental current must come from the source of M_1. It also flows through the channel of M_1 and from the source of M_5. It also flows through M_5 and from the input of the nMOS mirror, which reflects it to the output of the circuit, as shown in Fig. 40b. Thus, the second component of δI_{out} is given by

$$\delta I_{\mathrm{out}2} = 2\delta I_2 = \frac{g_{\mathrm{m}n}}{2} \cdot \delta V_{\mathrm{dm}}.$$

Superposing these two components of the output currents, we obtain the total incremental output current as

$$\delta I_{\mathrm{out}} = \delta I_{\mathrm{out}1} + \delta I_{\mathrm{out}2} = g_{\mathrm{m}n}\delta V_{\mathrm{dm}},$$

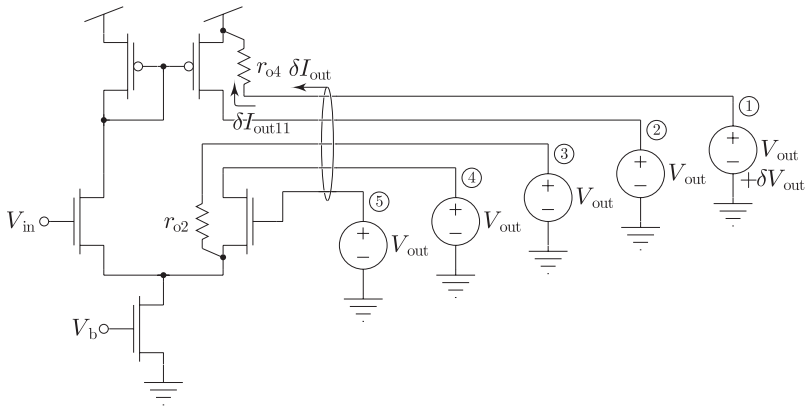
which implies that the incremental transconductance gain of the circuit with the output voltage held fixed is given by

$$G_{\mathrm{m}} = \frac{\delta I_{\mathrm{out}}}{\delta V_{\mathrm{dm}}} = g_{\mathrm{m}n}.$$

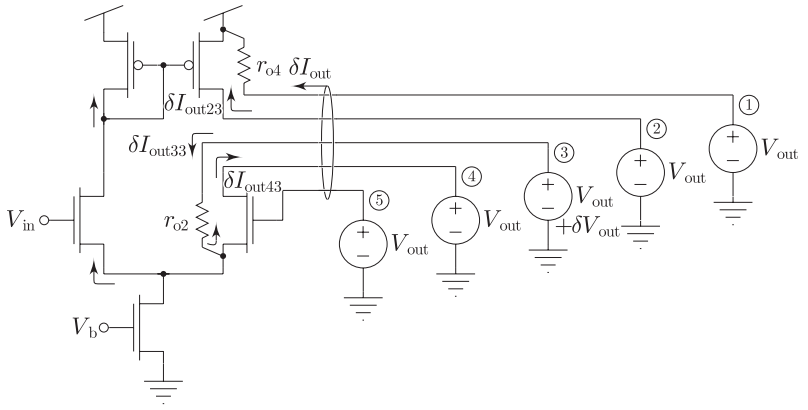
Therefore, the incremental differential-mode gain of the circuit is given approximately by

$$A_{\mathrm{dm}} = \frac{\delta V_{\mathrm{out}}}{\delta V_{\mathrm{dm}}} = G_{\mathrm{m}} R_{\mathrm{out}} \approx g_{\mathrm{m}n} r_{\mathrm{o}8} = g_{\mathrm{m}n} r_{\mathrm{o}n},$$

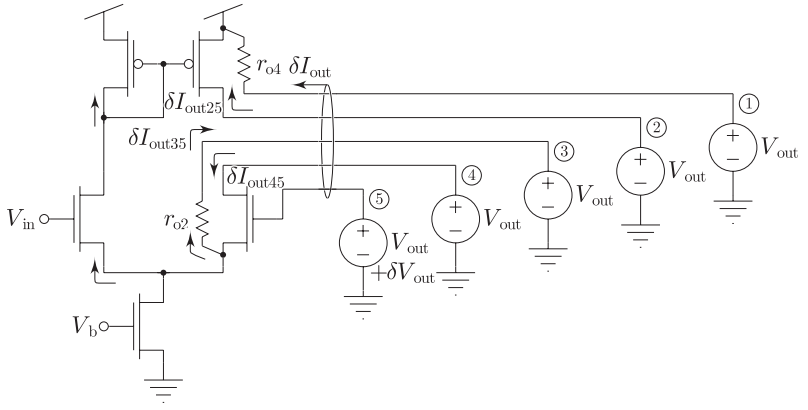
which is the intrinsic gain of each of the nMOS transistors in the circuit except for M_{b}, which carries a different current from the rest. ∎



(a)



(b)



(c)

Figure 33: The only nonzero components of δI_{out} occur when we apply δV_{out} to the replica sources on (a) branch 1, (b) branch 3, and (c) branch 5.

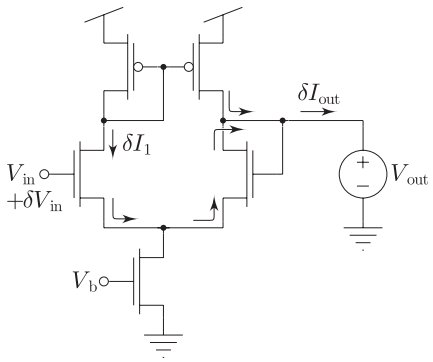


Figure 34: Calculation of the incremental transconductance gain of the follower-connected differential amplifier with the output voltage fixed.

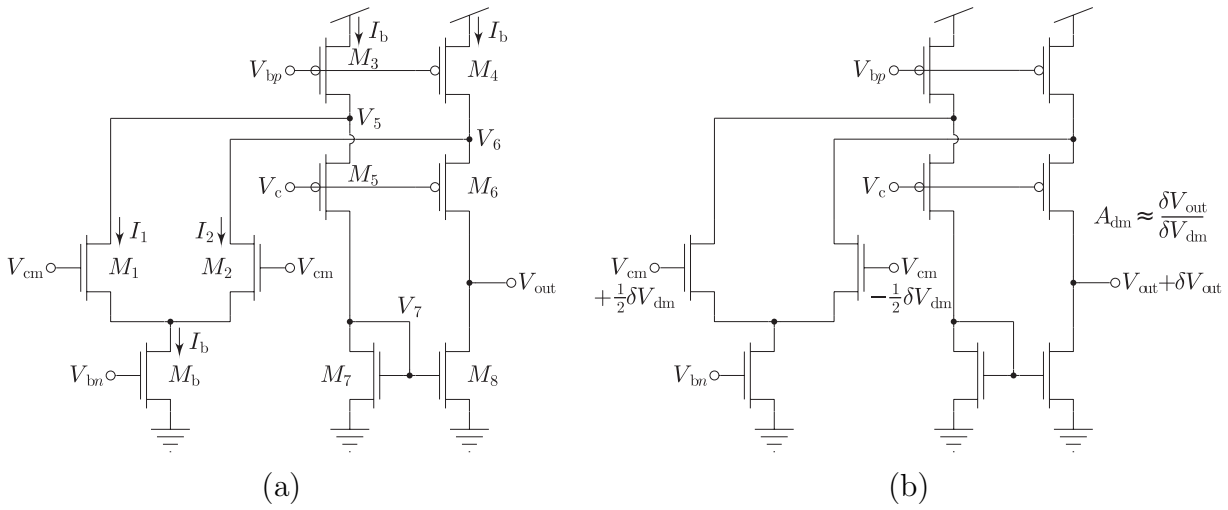


Figure 35: Folded-cascode differential amplifier.

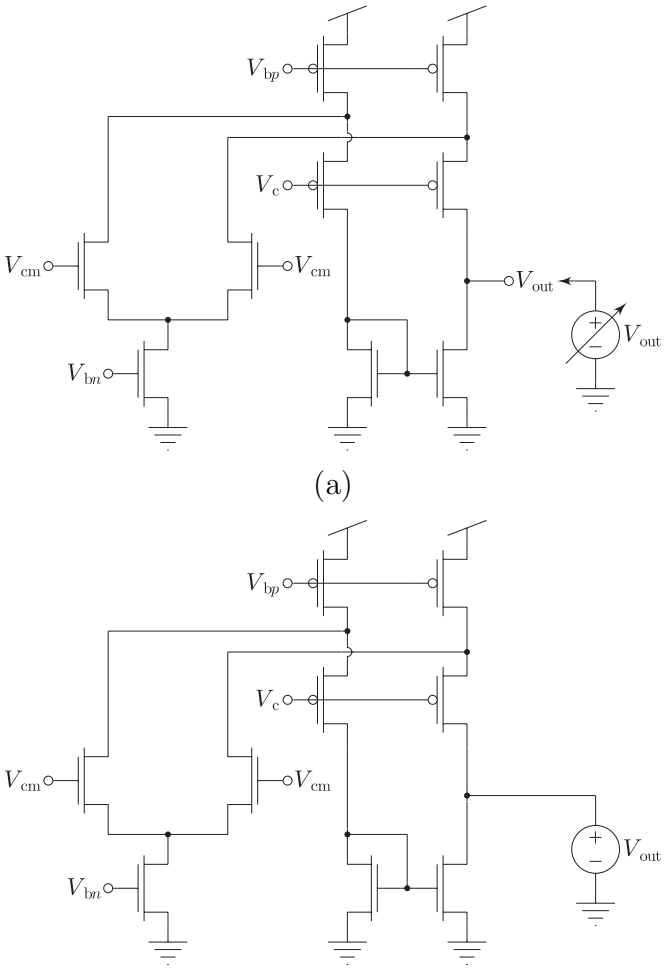


Figure 36: Fixing the output voltage of the folded-cascode differential amplifier.

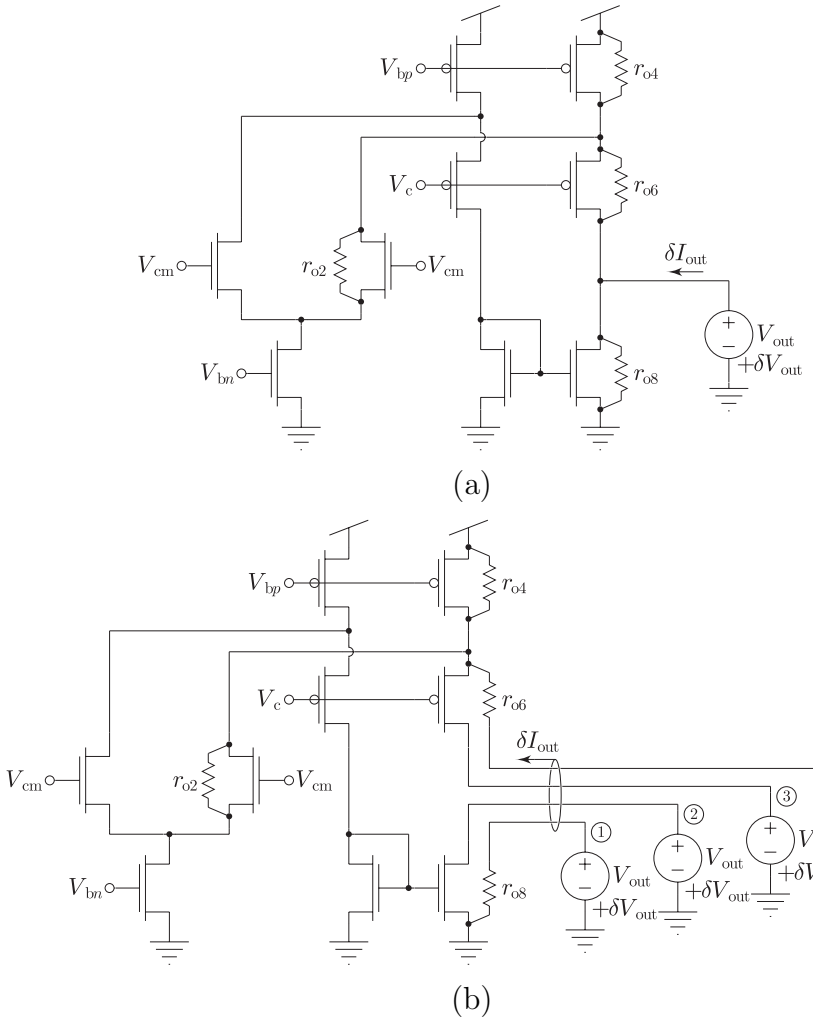


Figure 37: Calculation of the incremental output resistance of the folded-cascode differential amplifier with no applied input signal by voltage source splitting.

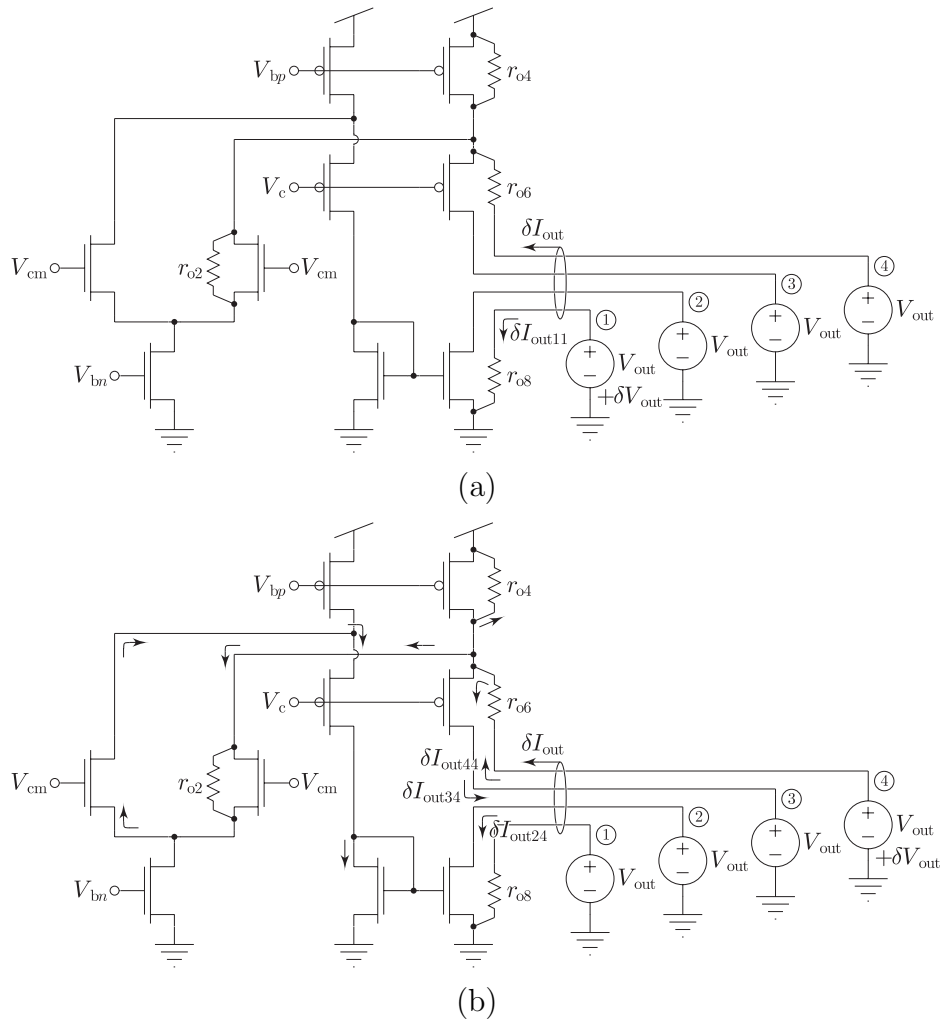


Figure 38: The only nonzero components of δI_{out} occur when we apply δV_{out} to the replica sources on (a) branch 1 and (b) branch 4.

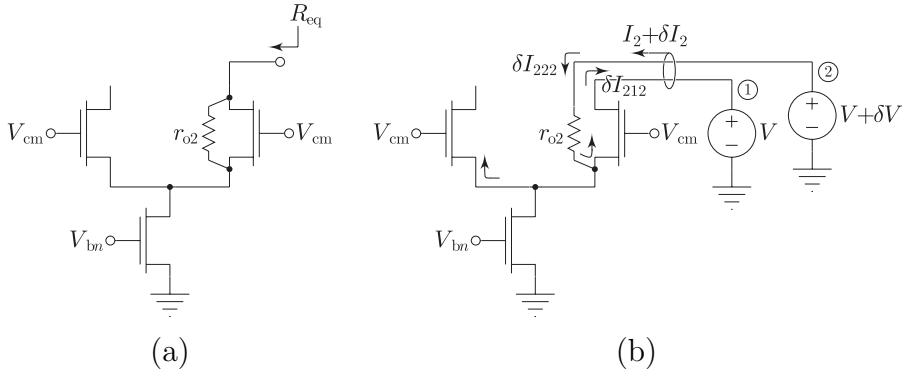


Figure 39: Auxiliary calculation of the incremental resistance seen looking into the drain of M_2 by voltage source splitting and superposition.

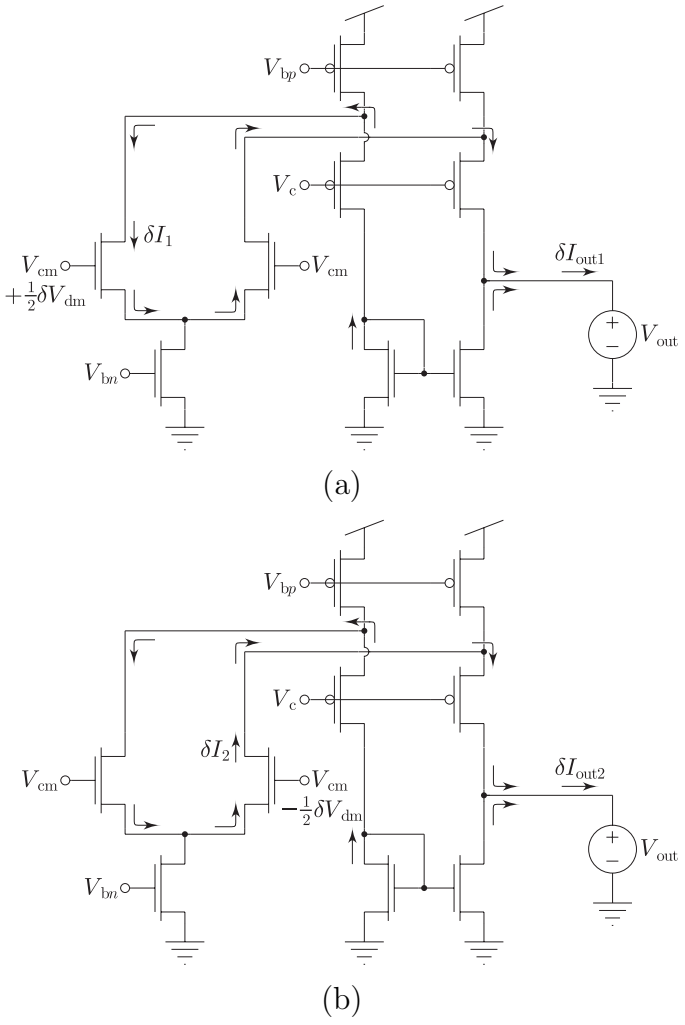


Figure 40: Calculation of the incremental transconductance gain of the folded-cascode differential amplifier with the output voltage fixed by superposition.