A Simple MOS Differential Amplifier

8.1 Objectives

In this lab, you will examine the voltage transfer characteristics and output-voltage swing of a simple MOS differential amplifier comprising an *n*MOS differential pair and a simple *p*MOS current mirror. You will also measure its incremental voltage gain, its incremental transconductance gain, and its output incremental output resistance. You will also examine the voltage tansfer characteristics of your amplifier configured as a unity-gain follower.

8.2 Prelab

The following prelab questions have been constructed to help you prepare to do the lab efficiently. Unless otherwise stated, you should assume that like transistors are matched and that the Early effect is negligible. Please complete these questions *before* you come to lab. While you may discuss the prelab questions with your lab partner or with other students in the class, each student in a lab group should complete the prelab assignment individually, so that you each understand the circuit that you will be testing and what you will be doing in the lab.

1. Consider the five-transistor circuit, shown in Fig. 8.1, comprising an *n*MOS differential pair and a simple *p*MOS current mirror. This circuit is arguably the simplest differential voltage amplifier that can be made. As with the differential pair, V_1 and V_2 are the inputs to the circuit, and V_b is a constant bias voltage that sets up the current flowing in the circuit. Suppose that transistors M_1 and M_2 are well matched and that transistors M_3 and M_4 are also matched. Also, suppose that the Early effect is negligible. If V_1 and V_2 were high enough to keep M_b saturated and we were to hold V_out with a voltage source so that M_2 and M_4 are also saturated, what would be the output current, I_out?

2. If we were to let go of the output by disconnecting the voltage source, in what direction would V_out go if I_out were (a) positive, (b) negative, and (c) zero?

3. Which input is the noninverting input (i.e., the one that causes the output to move in the same direction)? Which input is the inverting input?

4. If the Early effect were negligible, if $V_1 = V_2 = V_\mathrm{cm}$ and if V_out were fixed as explained in the first question, what would I_out be? If we were to change V_cm, what would I_out be? Under these circumstances, what would be the incremental common-mode

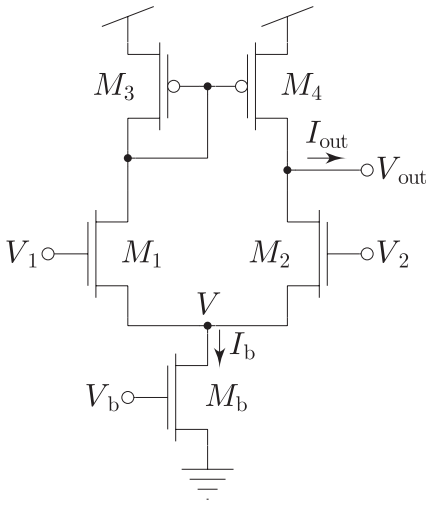

Figure 8.1: A simple MOS differential amplifier.

voltage gain of the circuit (i.e., $A_{\text{cm}} \approx \delta V_{\text{out}}/\delta V_{\text{cm}}$)? If we were to increase V_{dm} by a small amount, what would happen to I_{out}? If we were to let go of the output by disconnecting the voltage source, to what value would V_{out} eventually move? Instead, if we were to decrease V_{dm} by a small amount, what would happen to V_{out} under these circumstances? Under these circumstances, what would be the incremental differential-mode voltage gain of the circuit (i.e., $A_{\text{dm}} \approx \delta V_{\text{out}}/\delta V_{\text{dm}}$)?

8.3 Experiments

You will be doing three experiments in this lab. In the first experiment, you will examine the behavior of the differential amplifier in response to changes in the common-mode input voltage and the differential-mode input voltage. In the second experiment, you will measure the incremental output resistance of the differential amplifier and its incremental transconductance gain. You will also compute find the differential-mode voltage gain of the circuit in two different ways. In the third experiment, you will examine the voltage transfer characteristic of your amplifier configured as a unity-gain follower. You will be constructing your circuits from transistors on an ALD1106 quad nMOS transistor array or from transistors on an ALD1107 quad pMOS transistor array. Please note that these are CMOS chips, so you should follow good ESD practices so that these chips survive from one lab to the next. Also, please recall that MOS transistors are four-terminal devices and you will need to connect ground to pin 4 and V_{dd} to pin 11 of both the ALD1106 and the ALD1107 to establish the proper bulk voltage each type of chip.

8.3.1 Experiment 1: Voltage Transfer Characteristics

Construct a differential amplifier with an nMOS differential pair and a pMOS current mirror. Set the bias voltage so that your bias current is just at threshold.

Connect V_2 to a constant voltage source and sweep V_1 from one rail to the other, measuring V_{out} for at least three different values of V_2 that are above the bias voltage. In your report, include a single plot showing all of these voltage transfer characteristics (VTCs). Repeat this experiment for an above-threshold bias current. Does the behavior of the circuit differ substantially when biased in strong inversion compared to that which it exhibits in weak or moderate inversion?

8.3.2 Experiment 2: Transconductance, Output Resistance, and Gain

For a single value of V_2, sweep V_1 around V_2 in fine increments while measuring V_{out}. You should try to get several points in the high-gain region. Fit a straight line to the steep part of the curve and determine the differential-mode voltage gain of your circuit from the slope

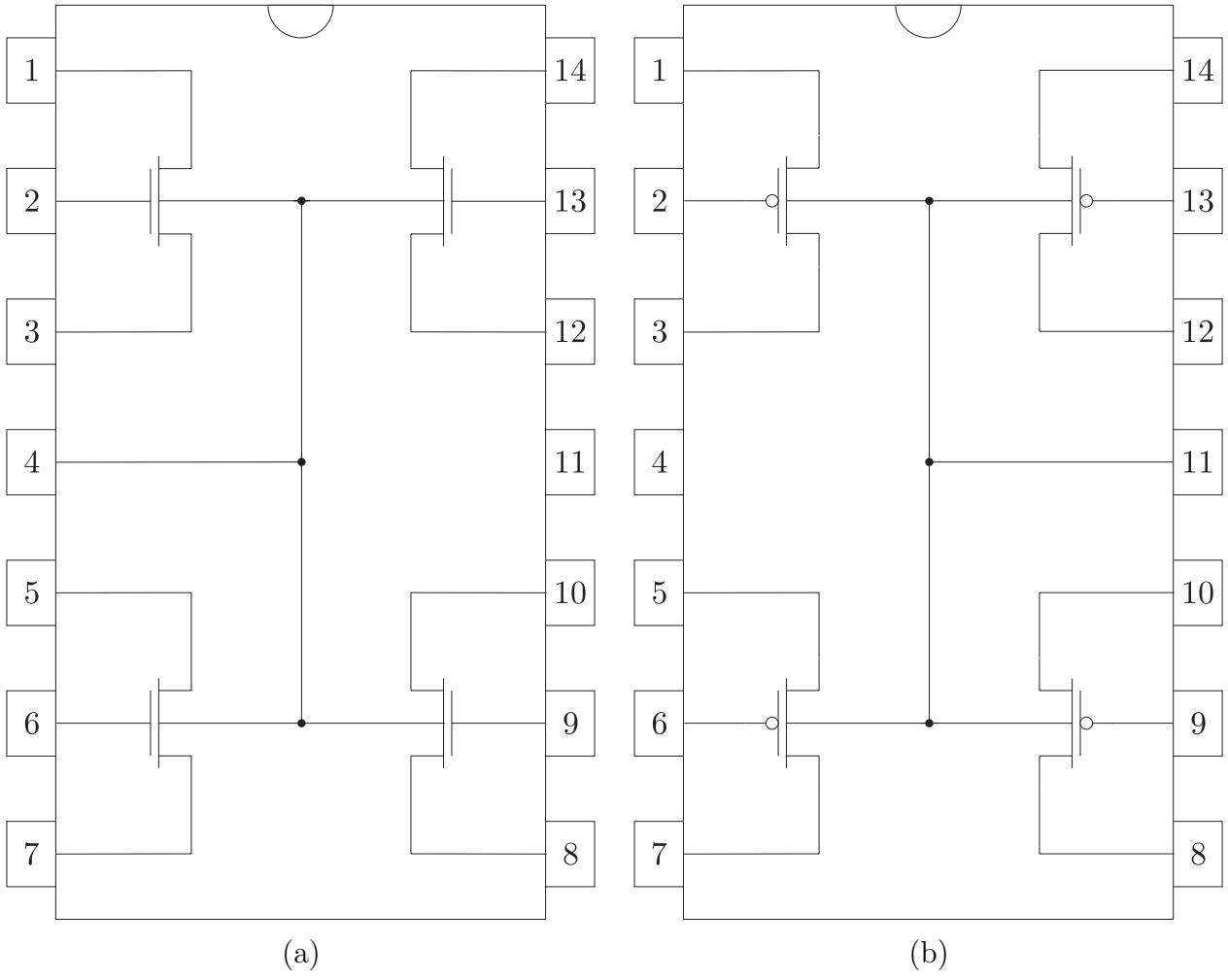

Figure 8.2: Pinouts of (a) the ALD1106 quad nMOS transistor array and (b) the ALD1107 quad pMOS transistor array.

of the best-fit line. In your report, include a plot showing V_{out} versus V_{dm} along with the best-fit line.

Next, set the differential-mode input voltage to zero and measure the current flowing into the output of the amplifier as you sweep V_{out} from one rail to the other. Fit a straight line to the shallow part of this output current–voltage characteristic, which should correspond to the range of output voltages over which the gain of the circuit is large, and determine the incremental output resistance of the circuit from the slope of the best-fit line. In your report, include a plot showing the output current-voltage characteristic along with the best-fit line.

Finally, fix the output voltage somewhere in the middle of the range of output voltages for which the circuit's gain is large and measure the current flowing out of the amplifier as you sweep V_1 around V_2. Fit a straight line to the curve around where $V_1 = V_2$ and extract a value of the incremental transconductance gain of the circuit with the output voltage fixed from the slope of the best-fit line. In your report, include a plot showing I_{out} versus V_{dm} along with the best-fit line.

The incremental differential-mode voltage gain of the circuit can be written as

$$A_{\text{dm}} = \frac{\partial V_{\text{out}}}{\partial V_{\text{dm}}} = \frac{\partial V_{\text{out}}}{\partial I_{\text{out}}} \cdot \frac{\partial I_{\text{out}}}{\partial V_{\text{dm}}} = R_{\text{out}} \cdot G_{\text{m}}.$$

From your incremental output resistance and your incremental transconductance gain, compute the differential-mode voltage gain of your circuit. How does this value of for the differential-mode gain compare to that which you obtained directly from the slope of the VTC?

8.3.3 Experiment 3: Unity-Gain Follower

Configure your amplifier as a unity-gain follower by connecting the output to the inverting input terminal. Measure V_{out} as you sweep V_{in} from one rail to the other. Fit a straight line to the VTC that you obtain. Is the incremental gain close to unity? In your report, include a plot showing V_{out} versus V_{in} along with the best-fit line. Repeat the sweep of V_{in} while measuring $V_{\text{out}} - V_{\text{in}}$ directly. Include a plot of $V_{\text{out}} - V_{\text{in}}$ versus V_{in} in your report. This plot represents the *offset voltage* of your amplifier. How does the offset voltage change as V_{in} changes?

8.4 Postlab

In Experiment 1, you swept V_1 from one rail to the other while measuring V_{out} for different values of V_2. You probably noticed that the output was able to get fairly close to V_{dd} when V_1 became slightly greater than V_2. However, you probably also observed that this circuit cannot pull its output voltage below approximately $\kappa\,(V_1 - V_{\text{b}})$. In this postlab assignment, you get to think about why that is the case. The VTC had four distinct regions:

1. $V_{\text{out}} \approx 0\,\text{V}$ for $0\,\text{V} \leq V_1 < V_{\text{b}} + V_{\text{DSsat}}/\kappa$,
2. $V_{\text{out}} \approx \kappa\,(V_1 - V_{\text{b}})$ for $V_{\text{b}} + V_{\text{DSsat}}/\kappa \leq V_1 < V_2$,

3. $V_{\text{out}} \approx V_{\text{out0}} + A\,(V_1 - V_2)$ for $V_1 \approx V_2$, and

4. $V_{\text{out}} \approx V_{\text{dd}}$ for $V_1 > V_2$.

For regions 2, 3, and 4, make a table that indicates for each of the five transistors in the circuit whether it is ohmic or saturated, whether it is in weak, moderate, or strong inversion, and approximately how much current flows through it (e.g., relative to I_{b}). You should assume that the bias current is just at threshold (i.e., $V_{\text{b}} = V_{\text{T0}}$ so that, if M_{b} is saturated, $I_{\text{b}} \approx \frac{1}{2} S I_{\text{s}}$).

Provide a concise (e.g., in a couple of sentences) explanation of the VTC in region 2. Would the story be any different for an above-threshold bias current?