The MOS Differential Pair

7.1 Objectives

In this lab, you will examine the current–voltage characteristics of a MOS *differential pair*, which is widely used as an input stage in operational amplifiers and in many other types of circuits as well. This venerable circuit has a relatively large response to a change in the difference between its two input voltages, but a relatively small response to a change in the average value of its two input voltages.

The differential pair had its origin in the days of the vacuum tube—it can be traced back to Fig. 3 of British Patent Specification 482,740 filed by A. D. Blumlein on July 4, 1936. Several years ago, the differential pair was informally chosen as the top analog circuit of all time in a top-ten list of analog circuits at the *International Solid-State Circuits Conference* during an evening panel discussion.

7.2 Prelab

The following prelab questions have been constructed to help you prepare to do the lab efficiently. Unless otherwise stated, you should assume that like transistors are matched and that the Early effect is negligible. Please complete these questions *before* you come to lab. While you may discuss the prelab questions with your lab partner or with other students in the class, each student in a lab group should complete the prelab assignment individually, so that you each understand the circuit that you will be testing and what you will be doing in the lab.

1. *The* n*MOS Differential Pair.* Consider the circuit shown in Fig. 7.1a, comprising three *n*MOS transistors. The sources of M_1 and M_2, which are called the *differential-pair transistors*, are connected together at node V. The third transistor, M_b, which is called the *bias transistor*, is supposed to sink a constant bias current, I_b, from node V. The gate voltages of M_1 and M_2 are the inputs to this circuit and the currents I_1 and I_2 are its outputs. For a circuit like the differential pair, we often express each of the two input voltages, V_1 and V_2, in terms of a *common-mode* input voltage, $V_\mathrm{cm} \equiv \frac{1}{2}(V_1 + V_2)$, and a *differential-mode* input voltage, $V_\mathrm{dm} \equiv V_1 - V_2$. Analogously, we also often express the two output currents, I_1 and I_2, in terms of a common-mode output current, $I_\mathrm{cm} \equiv \frac{1}{2}(I_1 + I_2)$, and a differential-mode output current, $I_\mathrm{dm} \equiv I_1 - I_2$. Suppose that M_1 and M_2 are well matched, that V_out1 and V_out2 are high enough to keep M_1 and M_2 in saturation, that V should be high enough to keep M_b in saturation, and that the Early effect is negligible.

   (a) What relationship holds in general among I_1, I_2, and I_b?

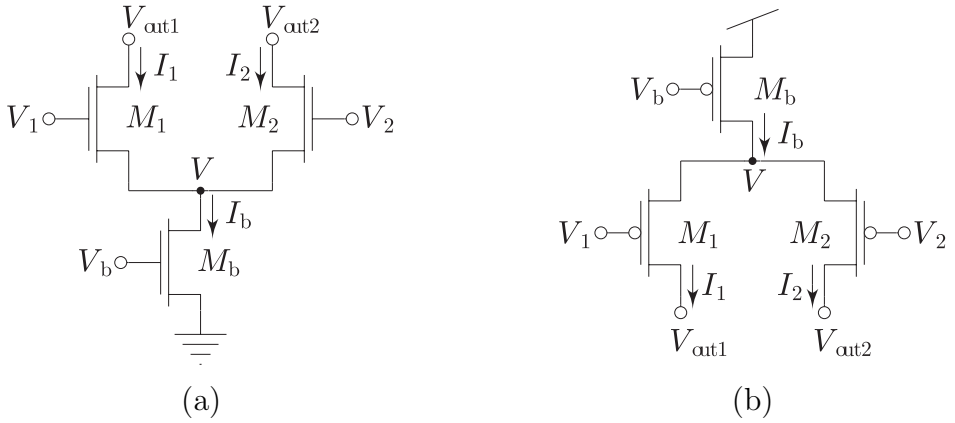

Figure 7.1: Differential pairs made from (a) *n*MOS and (b) *p*MOS transistors.

(b) Suppose that $V_1 = V_2 = V_{cm}$. What can be said about the relationship between I_1 and I_2? What will be the values of I_1 and I_2 under these circumstances?

(c) Suppose that V_1 exceeds V_2 by several tenths of a volt. What can be said about the relationship between I_1 and I_2? What will be the approximate values of I_1 and I_2 under these circumstances? Assuming that V is high enough to keep M_b in saturation, what will be the value of V under these circumstances?

(d) Suppose that V_2 exceeds V_1 by several tenths of a volt. What can be said about the relationship between I_1 and I_2? What will be the approximate values of I_1 and I_2 under these circumstances? Assuming that V is high enough to keep M_b in saturation, what will be the value of V under these circumstances?

(e) What approximate relationship describes how V depends on V_1, V_2, and V_b if V were high enough for M_b to remain saturated? What constraint exists on V_1 and V_2 to ensure that M_b remains saturated.

2. *The* p*MOS Differential Pair.* Consider the circuit shown in Fig. 7.1b, comprising three *p*MOS transistors. Again, the sources of M_1 and M_2 are connected together at node V. The bias transistor, M_b, is supposed to source a constant bias current, I_b, onto node V. The gate voltages of M_1 and M_2 are the inputs to this circuit and the currents I_1 and I_2 are its outputs. Suppose that M_1 and M_2 are well matched, that V_{out1} and V_{out2} are low enough to keep M_1 and M_2 in saturation, that V should be low enough to keep M_b in saturation, and that the Early effect is negligible.

(a) What relationship holds in general among I_1, I_2, and I_b?

(b) Suppose that $V_1 = V_2 = V_{cm}$. What can be said about the relationship between I_1 and I_2? What will be the values of I_1 and I_2 under these circumstances?

(c) Suppose that V_1 exceeds V_2 by several tenths of a volt. What can be said about the relationship between I_1 and I_2? What will be the approximate values of I_1 and I_2 under these circumstances? Assuming that V is low enough to keep M_b in saturation, what will be the value of V under these circumstances?

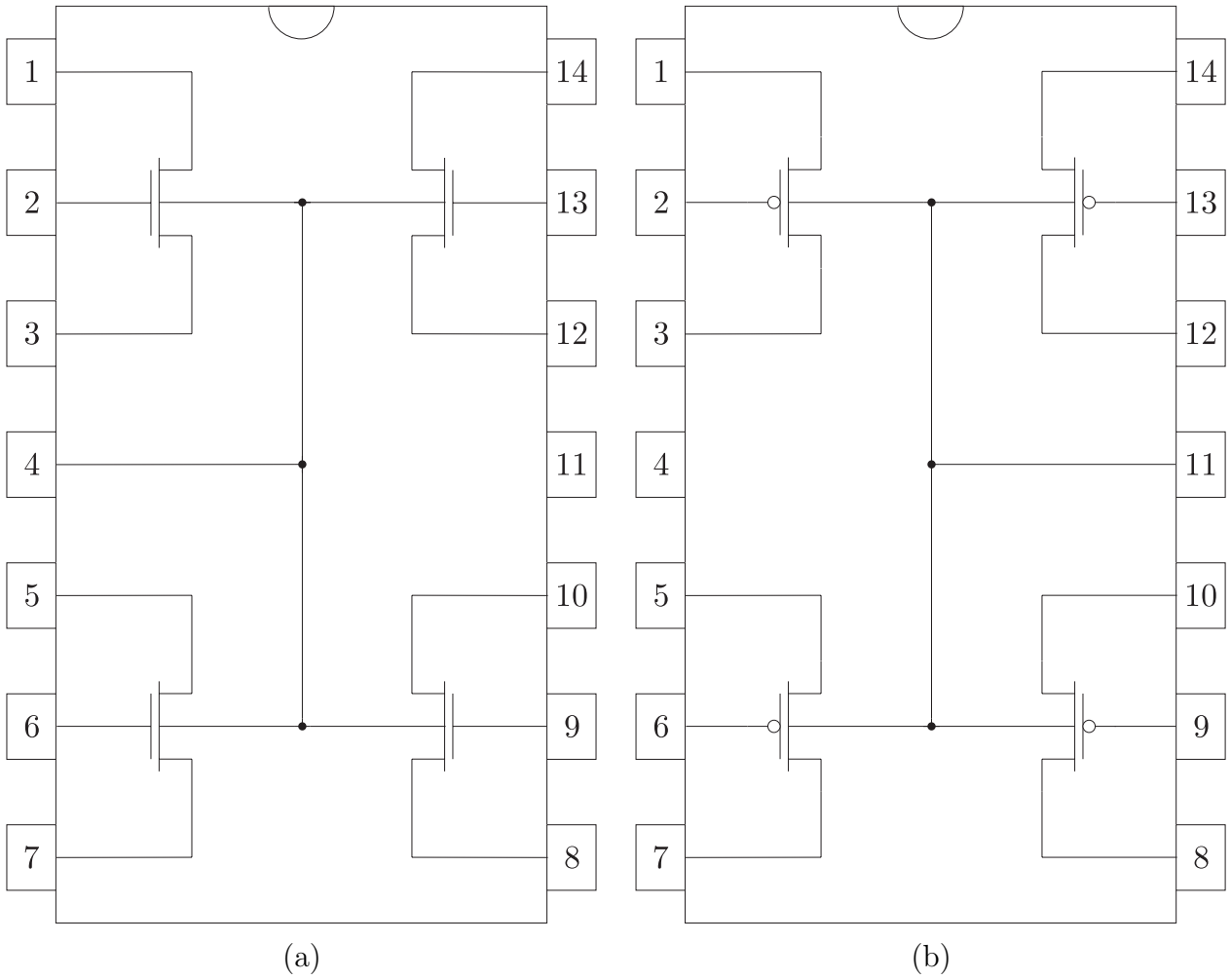

Figure 7.2: Pinouts of (a) the ALD1106 quad nMOS transistor array and (b) the ALD1107 quad pMOS transistor array.

(d) Suppose that V_2 exceeds V_1 by several tenths of a volt. What can be said about the relationship between I_1 and I_2? What will be the approximate values of I_1 and I_2 under these circumstances? Assuming that V is low enough to keep M_b in saturation, what will be the value of V under these circumstances?

(e) What approximate relationship describes how V depends on V_1, V_2, and V_b if V were low enough for M_b to remain saturated? What constraint exists on V_1 and V_2 to ensure that M_b remains saturated.

7.3 Experiments

You will be doing one experiment in this lab. You will measure the current–voltage characteristics of a differential pair for different values of the common-mode input voltage and as a

function of the bias current level. You will also examine the behavior of the common-source node voltage. You will be constructing your circuits from transistors on an ALD1106 quad nMOS transistor array or from transistors on an ALD1107 quad pMOS transistor array. Please note that these are CMOS chips, so you should follow good ESD practices so that these chips survive from one lab to the next. Also, please recall that MOS transistors are four-terminal devices and you will need to connect ground to pin 4 and V_{dd} to pin 11 of both the ALD1106 and the ALD1107 to establish the proper bulk voltage each type of chip.

7.3.1 Experiment 1: Differential Pair Current–Voltage Characteristics

Construct an nMOS differential pair, as shown in Fig. 7.1a, or a pMOS differential pair, as shown in Fig. 7.1b. Set the bias voltage, V_{b}, so that the bias current is just at or slightly below threshold, and set V_2 to a value sufficiently far away from the appropriate power supply rail so that the bias transistor is saturated. With the full power supply across the differential pair, measure each of the output currents, I_1 and I_2, and the common-source node voltage, V, as you sweep V_1 from a few tenths of a volt below V_2 to a few tenths of a volt above V_2. Repeat these measurements for at least two additional values of V_2 that are still sufficiently far away from the power supply rail to keep the bias transistor saturated. In your report, include a single plot showing I_1, I_2, $I_1 - I_2$, and $I_1 + I_2$, as a function of $V_1 - V_2$ for all three values of V_2 that you used. Do these current–voltage characteristics change significantly as V_2 changes? Also include a plot showing the common-source node voltage, V, as a function of $V_1 - V_2$ for all three values of V_2. How does the value of V change as V_1 goes from below V_2 to above it?

For each of the three values of V_2 that you used, fit a straight line to the plot of $I_1 - I_2$ as a function of $V_1 - V_2$ around the region where $V_1 \approx V_2$ (i.e., where $V_1 - V_2 \approx 0$). The slope of this line is approximately equal to the (incremental) *differential-mode transconductance gain* of the differential pair, which is formally given by

$$G_{\mathrm{dm}} \equiv \left.\frac{\partial I_{\mathrm{dm}}}{\partial V_{\mathrm{dm}}}\right|_{V_{\mathrm{dm}}=0} = \left.\frac{\partial\left(I_1 - I_2\right)}{\partial\left(V_1 - V_2\right)}\right|_{V_1=V_2}.$$

Does the value of the differential-mode transconductance gain change significantly as V_2 changes?

Now, set the bias voltage, V_{b}, so that the bias current is above threshold. For a single value of V_2 that is far enough away from the power supply rail to keep the bias transistor saturated, perform these same measurements. You might want to increase slightly the range over which you sweep $V_1 - V_2$ for these measurements. Make plot similar to the ones that you made for the lower bias current. How does the behavior of the circuit change as the bias current changes from weak or moderate inversion to strong inversion?

7.4 Postlab

Pick whichever version of the differential pair (i.e., nMOS or pMOS) you did not choose in Experiment 1 and repeat in simulation using LTspice the measurements that you did

in Experiment 1 on it. You do not need to perform any of the fits or the analysis on the simulation results that you did on the measured results. You just need to turn in your schematics and plots showing your simulation results. Briefly compare and contrast the behavior of the nMOS differential pair and that of the pMOS differential pair based on your experimental and simulation results.