# Series/Parallel MOS Networks and MOS Current Dividers

## 6.1 Objectives

In this lab, you will examine the characteristics of closely matched MOS transistors connected in series and in parallel. You will examine the characteristics of simple MOS current divider circuits, which are made from closely matched MOS transistors.

## 6.2 Prelab

The following prelab questions have been constructed to help you prepare to do the lab efficiently. Please complete these questions *before* you come to lab. While you may discuss the prelab questions with your lab partner or with other students in the class, each student in a lab group should complete the prelab assignment individually, so that you each understand the circuit(s) that you will be testing and what you will be doing in the lab.

1. *MOS Transistors in Series and Parallel.* Consider the pair of *matched* $n$MOS transistors, shown on the left in each part of Fig. 6.1. By calling these transistors matched, we mean that their properties are identical (e.g., they have the same width, length, threshold voltage, and threshold current, and they are operating at the same temperature), so that, if the same terminal voltages were applied to both devices, their channel currents would be identical. For this question, we shall assume that the Early effect is negligible. Recall that we can express the channel current of an MOS transistor in a *source/drain symmetric* form given by

$$I = I_{\mathrm{s}} \left( \mathrm{f}(V_{\mathrm{GB}}, V_{\mathrm{SB}}) - \mathrm{f}(V_{\mathrm{GB}}, V_{\mathrm{DB}}) \right), \tag{1}$$

   where $I_{\mathrm{s}}$ is related to the channel current of the transistor at threshold and $\mathrm{f}(\cdot)$ is a function that assumes an exponential form in weak inversion and a quadratic one in strong inversion. For an $n$MOS transistor, the bulk is connected to ground, so the three potentials in the model would simply be $V_{\mathrm{G}}$, $V_{\mathrm{D}}$, and $V_{\mathrm{S}}$.

   (a) Use the source/drain-symmetric model to show that two identical $n$MOS transistors with the same gate voltage connected in parallel, as shown in Fig. 6.1a, behave as a single $n$MOS transistor with twice the channel current of either single device for any combination of $V_{\mathrm{G}}$, $V_{\mathrm{S}}$, and $V_{\mathrm{D}}$.

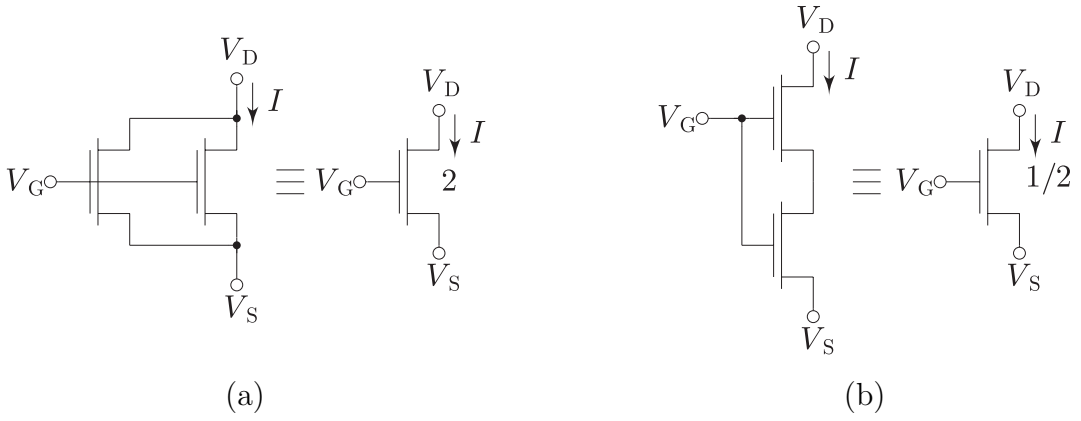


**Figure 6.1:** Two matched *n*MOS transistors connected with their channels connected in (a) parallel and (b) series. The parallel connection behaves just as if it were a single *n*MOS transistor whose current is twice as large as either of the individual devices. The series connection behaves as if it were a single *n*MOS transistor with half the current of either device. The same is true for *p*MOS transistors.

(b) Use the source/drain-symmetric model to show that two identical *n*MOS transistors with the same gate voltage connected in series, as shown in Fig. 6.1b, behave as a single *n*MOS transistor whose channel current is half that of either single device for any combination of $V_G$, $V_S$, and $V_D$.

*Hint*: Assume the form given in Eq. 1 for the current flowing through each device, apply Kirchhoff's current law at the intermediate node, and try to eliminate the intermediate node voltage from the equations. Note that you don't need to know the form of $f(\cdot)$ in order to accomplish this feat.

2. *MOS Current Dividers.* Figure 6.2 shows two simple two-way current dividers made with *n*MOS transistors. The transistors are matched in every way except that they have different strength ratios (i.e., $W/L$ ratios). For the divider of Fig. 6.2a, the input current is sunk from the sources of the two transistors and the output currents are taken at their drains. For the divider of Fig. 6.2b, the input current is sourced into the drains of the two transistors, and the output currents are taken at their sources.

   (a) For both current dividers, how are $I_{in}$, $I_1$, and $I_2$ related?

   (b) Under the assumption that $V_1 = V_2$, determine the current divider ratios $I_1/I_{in}$ and $I_2/I_{in}$ for each circuit.

   (c) For the current divider of Fig. 6.2a, suppose that $V_1$ and $V_2$ are sufficiently far above $V$ to guarantee that the transistors are operating in saturation and that the Early effect is negligible. Do the divider ratios that you found in part b hold if $V_1 \neq V_2$? Why or why not?

   (d) What is the maximum input current that each of these circuits can accept? For each one, what would happen if we were to exceed this limit?

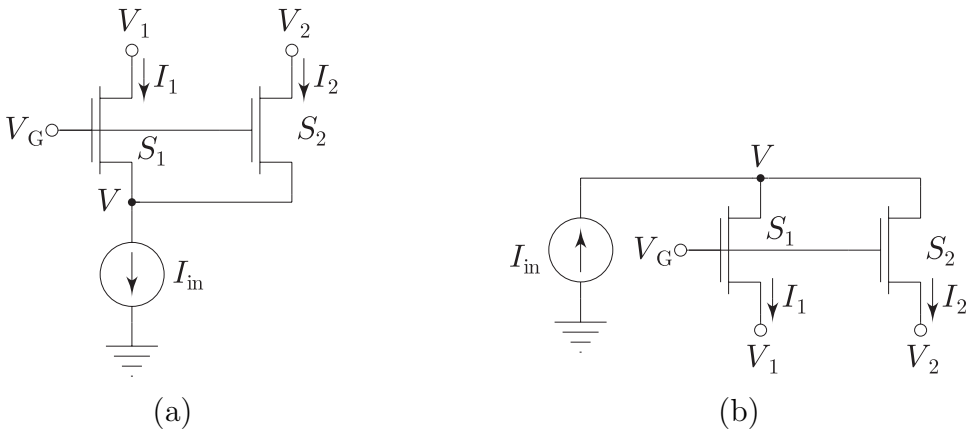


**Figure 6.2:** Two-way current dividers made from two $n$MOS transistors in which (a) the input current is sunk from their sources and the output currents are taken at their drains and (b) the input current is sourced into their drains and the output currents are taken at their sources.

## 6.3 Experiments

You will be doing three experiments in this lab. In the first experiment, you will examine the current–voltage characteristics of each of the four transistors on one of your chips to see how well their characteristics match one another. In the second experiment, you will examine the current–voltage characteristics of pairs of matched transistors in series and in parallel in various operating regimes. In the third experiment, you will construct current dividers out of MOS transistors and examine their current transfer characteristics.

You will be constructing your circuits from transistors on an ALD1106 quad $n$MOS transistor array or from transistors on an ALD1107 quad $p$MOS transistor array. The experiments are all written for $n$MOS transistors, but you can perform analogous experiments on $p$MOS transistors on your ALD1107 chip, if you would prefer. Please note that these are CMOS chips, so you should follow good ESD practices so that these chips survive from one lab to the next. Also, please recall that MOS transistors are four-terminal devices and you will need to connect ground to pin 4 and $V_{\mathrm{dd}}$ to pin 11 of both the ALD1106 and the ALD1107 to establish the proper bulk voltage each type of chip.

### 6.3.1 Experiment 1: Transistor Matching

For each of the four transistors on your ALD1106 chip, measure channel current as a function of gate voltage with the source voltage at ground and the drain voltage at $V_{\mathrm{dd}}$. Fit the EKV model to each of these characteristics and extract a value of $I_{\mathrm{s}}$, $\kappa$, and $V_{\mathrm{T0}}$. In your report, include a table showing these extracted parameter values for all four transistors. Also, make a single semilog plot for your report showing all four current–voltage characteristics along with the fits. Also, make a semilog (i.e., make the $x$-axis log) plot showing the percentage difference between each transistor's channel current and the mean value of all four channel currents as a function of the mean value of all four channel currents. How well do the

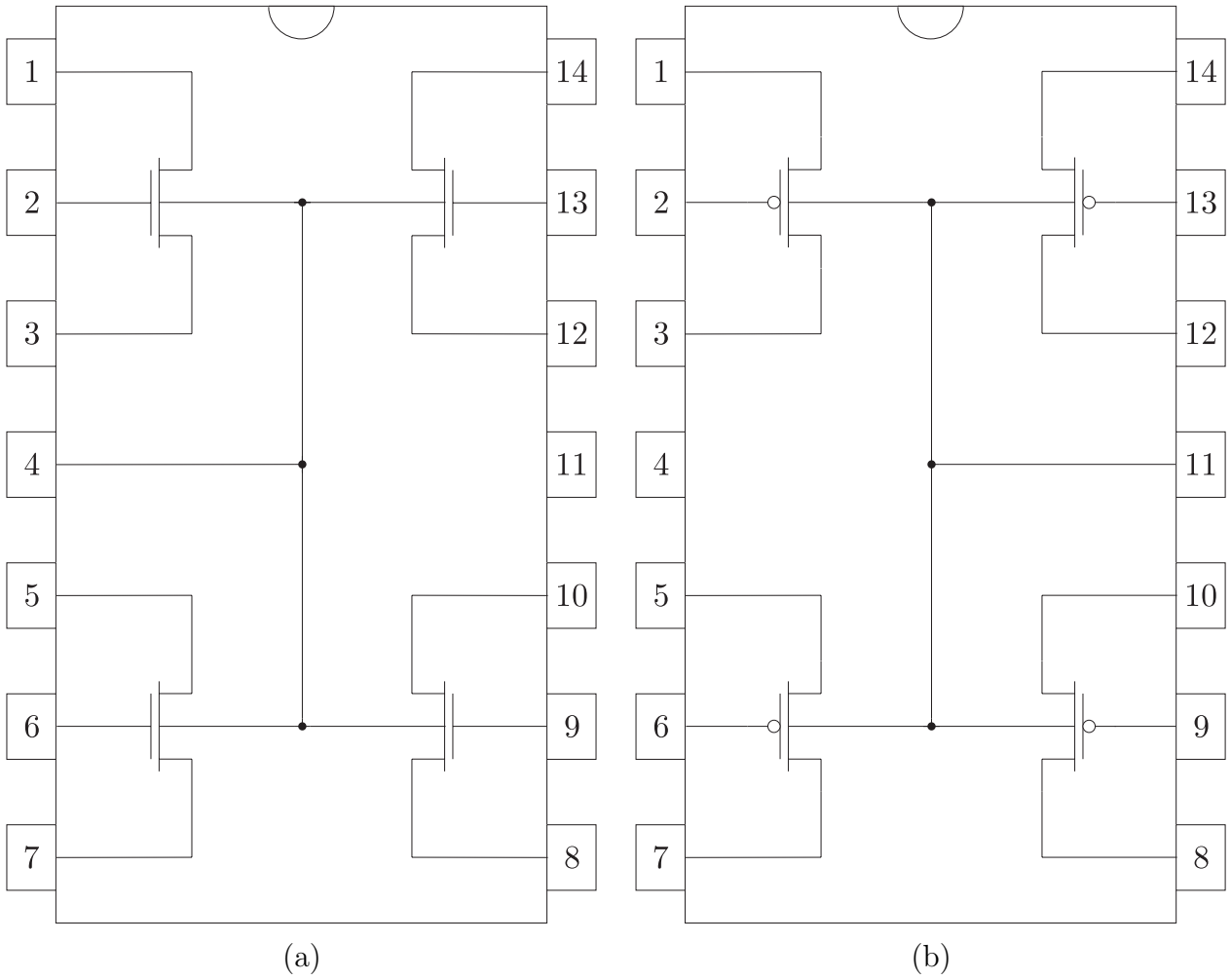


**Figure 6.3:** Pinouts of (a) the ALD1106 quad *n*MOS transistor array and (b) the ALD1107 quad *p*MOS transistor array.

transistors match each other? Do you notice any systematic trends? For instance, do the devices match better as a function of the level of inversion? Do certain devices match each other better than others?

### 6.3.2 Experiment 2: MOS Transistors in Series and Parallel

For a single *n*MOS transistor, measure channel current as a function of gate voltage both for $V_{\mathrm{DS}} = 10\,\mathrm{mV}$ and for $V_{\mathrm{DS}} = V_{\mathrm{dd}}$. Next, connect a matched pair of *n*MOS transistors in parallel with each other, as shown in Fig. 6.1a, and repeat the measurements that you just did one of the devices by itself. Is the channel current consistently about twice that of the individual transistor? Next, connect the same pair of transistors in series with each other, as shown in Fig. 6.1b, and repeat the same set of measurements. Is the channel current consistently half that of the individual transistor? In your report, include a single semilog plot showing data from the individual transistor, the parallel connection, and the

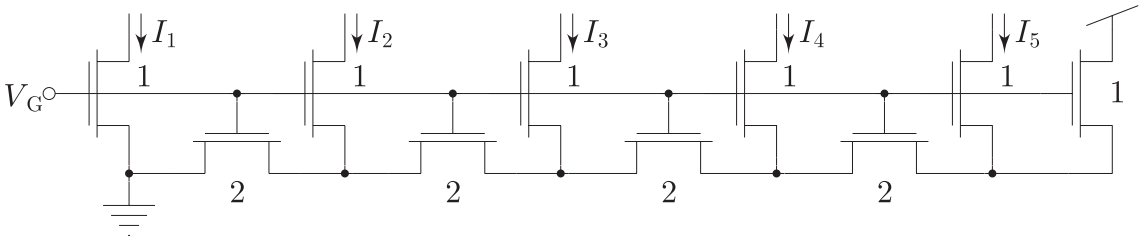


**Figure 6.4:** A ladder network of *n*MOS transistors.

series connection, for each of the two experimental situations. Also, include plots showing the ratio of the measurements from the parallel connection to those from the individual transistor and the ratio of the individual transistor measurements to those from the series connection. How well do the series/parallel equivalences work for MOS transistors? Are they better in certain regions of operation than others?

### 6.3.3 Experiment 3: MOS Current Dividers

Construct the two-way current divider of Fig. 6.2a in which the divider ratio is a ratio of two small integers from the *n*MOS transistors in your ALD1106 array by connecting them in series or in parallel. With one channel of the SMU, apply an input current to the divider as you measure one of the output currents with the other channel of the SMU. You can set the gate voltage to $V_{\rm dd}$ or with a potentiometer. You should set the drain voltages high enough to guarantee that the transistors are saturated. Measure the output current as a function of input current. Fit a straight line to the divider's current transfer characteristic and extract the value of the divider ratio. Make a plot showing both the measured data and the theoretical fit along with the extracted value of the divider ratio. How does the actual divider ratio compare to the theoretical one?

Next, construct the two-way current divider of Fig. 6.2b from the *n*MOS transistors in your ALD1106 array. With one channel of the SMU, apply an input current to the divider as you measure one of the output currents with the other channel of the SMU. You can set the gate voltage to $V_{\rm dd}$ or with a potentiometer. You should set the source voltages to ground and the gate voltage sufficiently high that the transistors can accomodate the maximum input current that you will use in your sweep. Measure the output current as a function of input current. Once again, fit a straight line to the divider's current transfer characteristic and extract the value of the divider ratio. Make a plot showing both the measured data and the theoretical fit along with the extracted value of the divider ratio. How does the actual divider ratio compare to the theoretical one?

## 6.4 Postlab

Consider the ladder network of matched *n*MOS transistors, shown in Fig. 6.4, comprising some devices with a unit strength ratio and others with twice that strength ratio. In doing your analysis, you should assume that the output voltages are high enough to saturate that

output transistors and that the Early effect is negligible. What relationship holds among the output currents? Does this relationship depend on whether the currents are in weak, moderate, or strong inversion? Can this ladder circuit be extended to have more outputs while maintaining any general relationship that you found? If so, show how. If not, explain why not.

*Hints*: Start from the right end of the circuit and work your way back toward the left end, successively applying KCL and the series/parallel equivalencies that you established in the prelab section. Also, think about whether or not the parallel equivalence depends on the drains being connected together if the transistors are saturated. You should not have to assume anything about the form of the channel current, beyond that given in Eq. 1.