MOS Transistor Characteristics

5.1 Objectives

In this lab, you will examine the current–voltage characteristics of the *n*MOS and of the *p*MOS transistor in various regions of operation. You will also examine several important incremental characteristics of these transistors.

5.2 Prelab

The following prelab questions have been constructed to help you prepare to do the lab efficiently. Please complete these questions *before* you come to lab. While you may discuss the prelab questions with your lab partner or with other students in the class, each student in a lab group should complete the prelab assignment individually, so that you each understand the circuit(s) that you will be testing and what you will be doing in the lab.

1. Draw three-terminal symbols for both an *n*MOS and a *p*MOS transistor and label all of the terminals; use S for source, D for drain, and G for gate. Indicate the direction of current flow through the channel that is consistent with your choice of drain and source.

2. Choose the word or phrase that best completes each of the following statements about an *n*MOS transistor.

   (a) The power supply rail that provides the proper reference for all of the terminal voltage is **(ground**|V_{dd}**)**.

   (b) The channel current flows from **(source to drain**|**drain to source)**.

   (c) The channel current is carried by **(electrons**|**holes)**.

   (d) To increase the channel current, we should **(increase**| **decrease)** the gate voltage.

   (e) The drain is always at a **(higher**|**lower)** potential than is the source.

3. Choose the word or phrase that best completes each of the following statements about a *p*MOS transistor.

   (a) The power supply rail that provides the proper reference for all of the terminal voltage is **(ground**|V_{dd}**)**.

   (b) The channel current flows from **(source to drain**|**drain to source)**.

   (c) The channel current is carried by **(electrons**|**holes)**.

(d) To increase the channel current, we should **(increase| decrease)** the gate voltage.

(e) The drain is always at a **(higher|lower)** potential than is the source.

4. For each transistor type, obtain an expression for saturation current as a function of gate voltage and source voltage that are valid in weak inversion, moderate inversion, and strong inversion. Show how each expression behaves in the weak-inversion limit and in the strong-inversion limit.

5. For each transistor type, obtain an expression both for the transistor's incremental transconductance gain and for its incremental source conductance that are valid for weak, moderate, and strong inversion. Express these in terms of the transistor's saturation current. Show how each expression behaves in the weak-inversion limit and in the strong-inversion limit.

6. The products $g_{\mathrm{m}}r_{\mathrm{o}}$ and $g_{\mathrm{s}}r_{\mathrm{o}}$ arise again and again in incremental analyses of circuits involving MOS transistors. Here, g_{m} denotes the incremental transconductance of the MOS transistor in saturation, g_{s} denotes the incremental conductance of the source terminal in saturation, and r_{o} denotes the incremental output resistance of the MOS transistor in saturation. These groupings of small-signal parameters are both referred to as *intrinsic gains* of an MOS transistor. The former product is the theoretical maximum incremental voltage gain of the transistor configured as a common-source amplifier. The latter product is the maximum incremental voltage gain of the transistor configured as a common-gate amplifier.

   (a) For any given current level, how are the two intrinsic gains of an MOS transistor related to each other?

   (b) Explain how the $g_{\mathrm{s}}r_{\mathrm{o}}$ intrinsic gain of an MOS transistor can be extracted from a drain characteristic.

5.3 Experiments

You will be doing three experiments in this lab. In the first experiment, you will measue channel current as a function of gate voltage for both an nMOS and a pMOS transistor. In the second experiment, you will measure channel current as a function of source voltage for both an nMOS and a pMOS transistor. In the third experiment, you will measure the channel current as a function of drain voltage for both an nMOS and a pMOS transistor.

For this lab, you will be characterizing transistors on an ALD1106 quad nMOS transistor array on an ALD1107 quad pMOS transistor array. Please note that these are CMOS chips, so you should follow good ESD practices so that these chips survive from one lab to the next. Also, please recall that MOS transistors are four-terminal devices and you will need to connect ground to pin 4 and V_{dd} to pin 11 of both the ALD1106 and the ALD1107 to establish the proper bulk voltage each type of chip. For the pMOS measurements, you will probably obtain the best results if you reference your voltages to V_{dd} (i.e., connect the black lead of the SMU channels to V_{dd}).

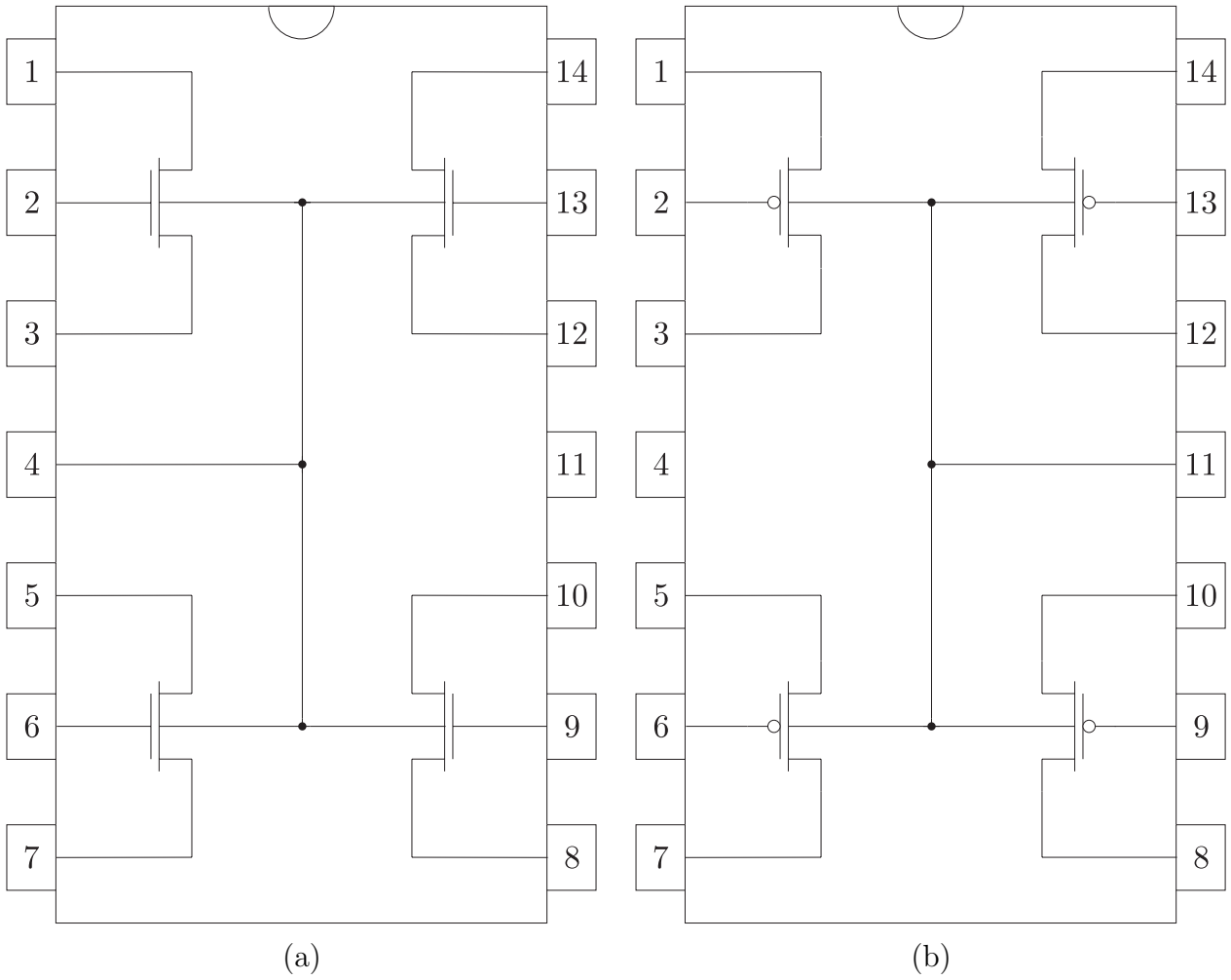

Figure 5.1: Pinouts of (a) the ALD1106 quad nMOS transistor array and (b) the ALD1107 quad pMOS transistor array.

5.3.1 Experiment 1: Gate Characteristics

Obtain an ALD1106 nMOS transistor array and an ALD1107 pMOS transistor array. For one of the four nMOS transistors on your chip, measure channel current as a function of gate voltage with the source voltage at ground and the drain voltage set sufficiently far enough above ground to guarantee that the transistor remains in saturation. In a corresponding manner, for one of the pMOS transistors on your other chip, measure channel current as a function of gate voltage with the source voltage set to V_{dd} and the drain voltage sufficiently far enough below V_{dd} to guarantee that the transistor remains in saturation. For each of these sweeps, be sure you get a good number of points (e.g., at least 20) in the weak, moderate, and strong inversion regions. Fit the EKV model to each of these current–voltage characteristics, extracting a values of I_{s}, κ, and V_{T0} for each type of transistor. In your report, include a single semilog (i.e., y-axis logarithmic) plot for both transistor types along with the theoretical fits.

From your measured characteristics, extract each transistor's incremental transconductance gain. As you did in Lab 2, you should be able to use `diff` and `./` in MATLAB to obtain a crude finite-difference approximation to the partial derivative of the channel current with respect to the gate voltage. For your report, make a log-log plot showing the incremental transconductance gain of each transistor as a function of the current flowing through it, along with a theoretical fit to each curve in the weak-inversion region and in the strong-inversion region. Do the theoretical fits match the data in the weak-inversion region and in the strong-inversion region?

5.3.2 Experiment 2: Source Characteristics

For your nMOS transistor, measure channel current as a function of source voltage with the gate and drain voltages both set at V_{dd}. Correspondingly, for your pMOS transistor, measure channel current as a function of source voltage with the gate and drain voltages both set at ground. For each type of transistor, make a semilog plot showing the current as a function of the source voltage along with a fits to the weak-inversion regions of each curve. What is the slope of the exponential in this regime? How do these characteristics compare to the gate characteristics that you obtained in Experiment 1?

From these characteristics, extract each transistor's incremental source conductance. For your report, make a log-log plot showing the incremental source conductance of each transistor as a function of the current flowing through it, along with a theoretical fit to each curve in the weak-inversion region and in the strong-inversion region. Do the theoretical fits match the data in the weak-inversion region and in the strong-inversion region?

5.3.3 Experiment 3: Drain Characteristics

For your nMOS transistor, measure channel current as a function of drain voltage for three values of gate voltage: about 100 mV below the threshold voltage (weak inversion), the threshold voltage (moderate inversion), and V_{dd} (strong inversion). For each of these sweeps, you should set the source voltage to ground. For your pMOS transistor, measure channel current as a function of drain voltage for three values of gate voltage: about 100 mV from the threshold (weak inversion), the threshold (moderate inversion), and ground (strong inversion). For each of these sweeps, you should set the source voltage to V_{dd}.

From each of your drain characteristics, extract values of the Early voltage, the saturation current, and the transistor's intrinsic gain (i.e., $g_{\mathrm{s}}r_{\mathrm{o}}$). In your report, include a single semilog plot (y-axis logarithmic) showing all of the nMOS drain characteristics that you took and a single semilog plot (y-axis logarithmic) showing all of the pMOS drain characteristics that you took. Also, include a single semilog (x-axis logarithmic) plot showing Early voltage as a function of saturation current for both types of transistors. Finally, include a single loglog plot showing intrinsic gain as a function of saturation current for both types of transistors. In many incremental analyses of CMOS circuits, we would like to invoke several kinds of approximations that are based on the assumption that a transistor's intrinsic gain is much larger than unity. From your experimental measurements, does it seem that this assumption is generally a good one? What can you say about $g_{\mathrm{m}}r_{\mathrm{o}}$ from your data?

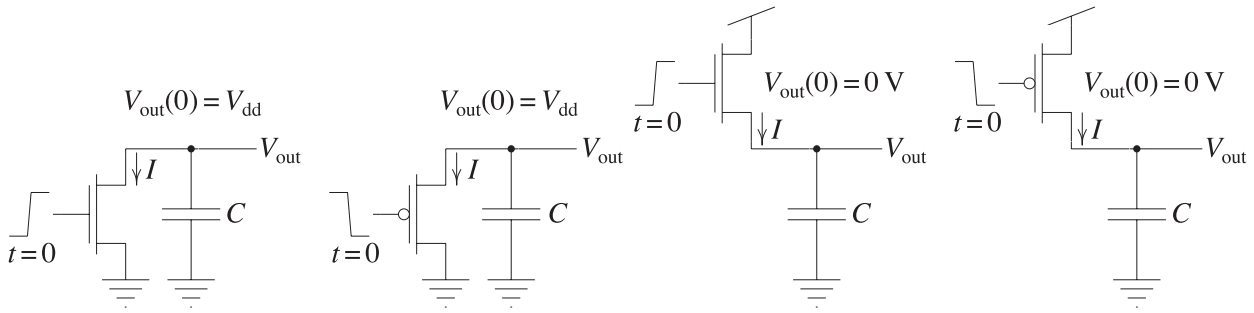

Figure 5.2: Using nMOS and pMOS transistors to pass 1s and 0s. On an integrated circuit, a typical value of C is on the order of 100 fF.

5.4 Postlab

When we build logic gates out of MOS transistors, we want to treat these devices as voltage-controlled switches. We would like to treat the nMOS transistor as if it were a closed switch when its gate voltage is at V_{dd}, which we usually take to be the representation of a logical 1, and we would like to treat it as if it were an open switch when its gate voltage is at ground, which we usually take to be the representation of a logical 0. Correspondingly, we would like to treat the pMOS transistor as if it were an open switch when its gate voltage is at V_{dd}, and we would like to treat it as if it were a closed switch when its gate voltage is at ground. The nMOS transistor and the pMOS transistor behave in just the opposite ways; their functions are complementary to one another.

It turns out that, when its gate voltage is V_{dd}, an nMOS transistor can pull a node all the way down to ground, but it cannot pull a node all the way up to V_{dd}. We sometimes express this fact by saying that an nMOS transistor can pass a *strong* 0, but only a *weak* 1. A weak 1 is a sort of half-hearted logic high. On the other hand, when its gate voltage is at ground, a pMOS transistor can pull a node all the way up to V_{dd}, but it cannot pull a node all the way down to ground. We sometimes express this fact by saying that a pMOS transistor can pass a *strong* 1, but only a *weak* 0. In this context, a strong 0 is a voltage very close to ground, and a strong 1 is a voltage very close to V_{dd}. A weak 0 would be a voltage that is a sort of half-hearted logic low, perhaps 1 V or 1.5 V above ground, and a weak 1 would be a voltage that is a sort of half-hearted logic high, perhaps 1 V or 1.5 V below V_{dd}. Because of these facts, when we design CMOS logic gates, we usually use nMOS transistors exclusively to produce logical 0s and we use pMOS transistors exclusively to produce logical 1s. Using your data from Experiments 2 and 3, explain why it is that nMOS transistors pass strong 0s and weak 1s and why it is that pMOS transistors pass weak 0s and strong 1s.

Hints: Consider each of the four situations depicted in Fig. 5.2 and determine what the value of V_{out} is after a long time. Recall that, for a logic gate in this day and age, one microsecond is a long time and one second is virtually an eternity. In each case, think about which terminal is the source and which is the drain and think about what it is that makes V_{out} go up or down.