Folding the Differential Pair for Low-Voltage Applications

Bradley A. Minch

Mixed Analog-Digital VLSI Circuits and Systems Laboratory
School of Electrical and Computer Engineering
Cornell University
Ithaca, NY 14853–5401

minch@ece.cornell.edu
http://people.ece.cornell.edu/minch
Conventional MOS Differential Pairs

The differential pair is widely used as an input stage for operational amplifiers, comparators, mixers, and many other circuits.

This circuit does not function well with a low power-supply voltage, because transistor $M_b$ shuts off if $V_1$ and $V_2$ get too close to the appropriate rail.
Conventional MOS Differential Pairs

Differential-pair intuition:

- $I_1 = f(V_1, -V)$ and $I_2 = f(V_2, -V)$, where $f$ is expansive.
- $V$ adjusts itself so that $I_1 + I_2 \rightarrow I_b$. 
Capacitive Voltage Dividers

The voltage on the middle node is a weighted sum of the two input voltages.

If node $V$ is really floating, then the inputs couple into the floating node all the way down to DC!

The charge $Q$ linearly offsets the $V$. The charge can be adjusted either optically or electronically.

\[-C_1(V_1 - V) - C_2(V_2 - V) = Q\]

\[(C_1 + C_2)V = C_1V_1 + C_2V_2 + Q\]

\[V = \frac{C_1}{C_1 + C_2} V_1 + \frac{C_2}{C_1 + C_2} V_2 + \frac{Q}{C_1 + C_2}\]
Floating-Gate MOS Transitors

The capacitors $C_1$ and $C_2$ are called control gates.

If floating-gate voltage, $V$, is a weighted sum of the control-gate voltages.

The floating-gate charge, $Q$, can be thought of as giving us a programmable threshold voltage.
A Folded Floating-Gate Differential Pair

Differential-pair intuition:

$\mathbf{I}_1 = f(V_1, V)$ and $\mathbf{I}_2 = f(V_2, V)$, where $f$ is expansive.

$V$ adjusts itself so that $\mathbf{I}_1 + \mathbf{I}_2 \rightarrow \mathbf{I}_b$. 
A Folded Floating-Gate Differential Pair

Differential-pair intuition:

\[ I_1 = f(V_1, V) \] and \[ I_2 = f(V_2, V) \], where \( f \) is expansive.

\[ V \text{ adjusts itself so that } I_1 + I_2 \rightarrow I_b. \]

Sign difference permits us to \( \text{fold} \) \( M_b \) relative to \( M_1 \) and \( M_2 \).
A Folded Floating-Gate Differential Pair

\[ V_1 \to V_2 \to V \]

\[ M_{1b} \quad C_2 \quad M_{1a} \quad I_1 \quad I_2 \quad M_{2a} \quad C_2 \quad M_{2b} \]

\[ V_b \to M_b \]

\[ I_1 \quad I_2 \quad I_b \]

\[ V_1 \quad V_2 \]

Differential-pair intuition:

- \[ I_1 = f(V_1, V) \] and \[ I_2 = f(V_2, V) \], where \( f \) is expansive.

- \( V \) adjusts itself so that \[ I_1 + I_2 \to I_b \].

\( M_{1b} \) and \( M_{2b} \) provide mirror copies of \( I_1 \) and \( I_2 \).
A Folded Floating-Gate Differential Pair

Differential-pair intuition:

- $I_1 = f(V_1, V)$ and $I_2 = f(V_2, V)$, where $f$ is expansive.
- $V$ adjusts itself so that $I_1 + I_2 \to I_b$.

$M_{1c}$ and $M_{2c}$ mitigate the $C_{gd}$’s of transistors $M_{1b}$ and $M_{2b}$.
A Folded Floating-Gate Differential Pair

- $C_1$ sets the linear range and transconductance gain.
- $C_2$ controls by how much $V$ changes in response to changes in either $V_{\text{cm}}$ or $I_b$.
- Input and output voltage ranges are from rail-to-rail.
- Transconductance gain nearly constant with $V_{\text{cm}}$. 

\[ V_1 \quad V \quad V_2 \]

\[ M_{1b} \quad C_2 \quad M_{1a} \quad V \quad M_{2a} \quad C_2 \quad M_{2b} \]

\[ M_{1c} \quad I_1 \quad V_b \quad M_b \quad I_b \quad V_c \quad M_{2c} \quad I_2 \]
Output Currents vs. $V_{dm}$ ($I_b = 316 \text{ pA}$)

$I_1, I_2, I_1 - I_2, I_1 + I_2$ (pA)

$V_{cm} = 1.2 \text{ V}$

$V_{cm} = 0 \text{ V}$
Output Currents vs. $V_{dm}$ ($I_b = 31.6 \mu A$)
Transconductance Gain vs. $V_{cm}$

![Graph showing transconductance gain vs. $V_{cm}$ with various current levels.

$g_{dm} (A/V)$ vs. $V_{cm} (V)$

- $100 \mu A$
- $31.6 \mu A$
- $10.0 \mu A$
- $3.16 \mu A$
- $1.00 \mu A$
- $316 \text{nA}$
- $100 \text{nA}$
- $31.6 \text{nA}$
- $10.0 \text{nA}$
- $3.16 \text{nA}$
- $1.00 \text{nA}$
- $316 \text{pA}$

$I_b = 100 \text{pA}$

MAD VLSI
Circuits & Systems Lab
Output Currents vs. $V_{out}$ ($I_b = 300$ pA)
Output Currents vs. $V_{\text{out}}$ ($I_b = 31.6 \, \mu\text{A}$)
Common-Mode Output Current vs. $V_{out}$
Add resistive feedback to the floating gates in parallel with $C_2$ controlled by $V_r$.

Resistive path introduces a first-order low-frequency roll-off whose corner frequency is set by $C_T$ and $V_r$.

At DC, the circuit is a pair of current mirrors sharing $I_b$ equally. Above the corner, it acts as the FG circuit.
Variations on a Theme...

Use feedback transistors as switches gated by a clock signal, $\phi$.

- When $\phi$ is high, the circuit rebalances itself. When $\phi$ is low, the circuit acts just like the FG circuit.

- Injected charge is rejected as a common-mode signal if it matches on both sides.
Variations on a Theme...

Rail-to-rail input common-mode range, wide output voltage swing.

Acts very much like an emitter-degenerated bipolar differential pair.

Input resistance primarily determined by $R$ because base nodes are basically clamped by shunt feedback.
Given that $g_m \left( r_{on} \parallel 2 r_{op} \right) \gg 1$ and $C_3 \ll C_2$, we can show that

$$i_{dm} \equiv i_1 - i_2 = g_m \frac{C_1}{C_T} \frac{1 - sC_3/g_m}{1 + s(C_3 + C_4)/g_s} v_{dm}$$

where $C_T \equiv C_1 + C_2 + C_3 + C_b$. 
...and that

\[ i_{cm} \equiv \frac{i_1 + i_2}{2} \]

\[ = \frac{C_1/C_2}{r_{on} \| 2r_{op}} \frac{(1 - sC_3/g_m)(1 + s(r_{on} \| 2r_{op}))(C_2 + C/2)}{(1 + s(C_3 + C_4)/g_s)(1 + s(C_2\| (C_1 + C_3 + C_b))/(g_m C_2/C_T))} v_{cm} \]
Incremental High-Frequency Analysis

...and so

\[
\text{CMRR} \equiv \frac{i_{\text{dm}}/v_{\text{dm}}}{i_{\text{cm}}/v_{\text{cm}}} = g_m \left( r_{\text{on}} \| 2r_{\text{op}} \right) \frac{C_2}{C_T} \frac{1 + s \left( C_2 \| (C_1 + C_3 + C_b) \right)}{\left( 1 + s \left( r_{\text{on}} \| 2r_{\text{op}} \right) \left( C_2 + C/2 \right) \right)}
\]
Folded FGMOS Differential Pair Layout
Chip Photomicrograph