Folding the Differential Pair for Low-Voltage Applications

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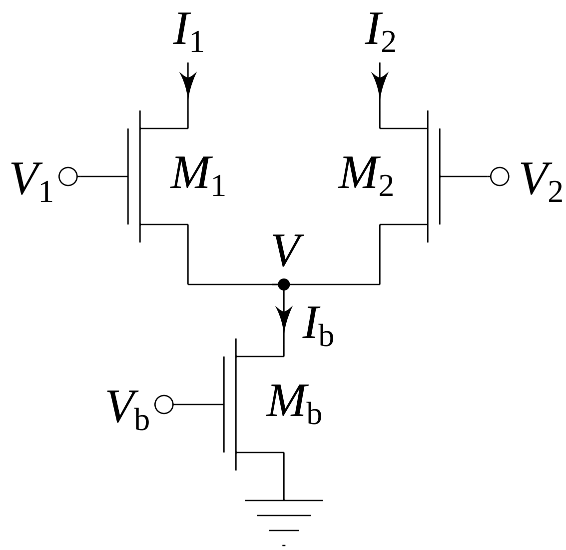
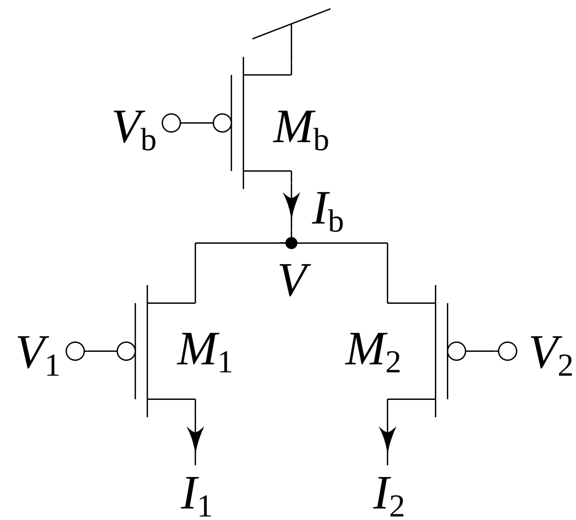
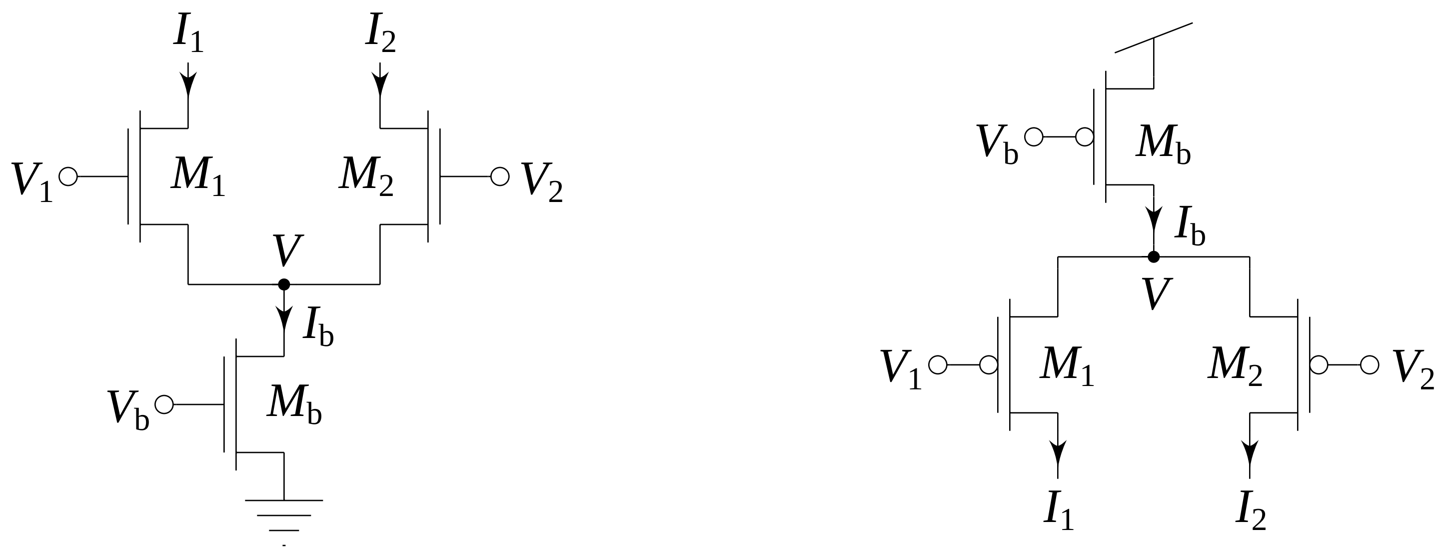
Conventional MOS Differential Pairs





- The differential pair is widely used as an input stage for operational amplifiers, comparators, mixers, and many other circuits.
- This circuit does not function well with a low power-supply voltage, because transistor M_b shuts off if V_1 and V_2 get too close to the appropriate rail.

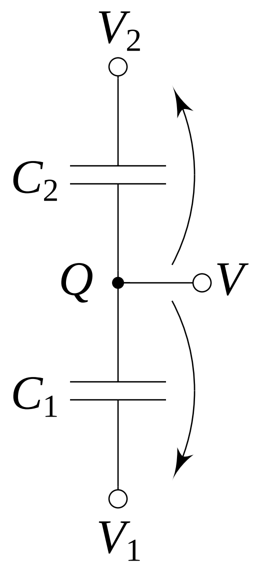
Conventional MOS Differential Pairs



Differential-pair intuition:

- $I_1 = f(V_1, \text{-}V)$ and $I_2 = f(V_2, \text{-}V)$, where f is expansive.
- V adjusts itself so that $I_1 + I_2 \to I_b$.

Capacitive Voltage Dividers



$$-C_1(V_1 - V) - C_2(V_2 - V) = Q$$

$$\Rightarrow (C_1 + C_2)V = C_1V_1 + C_2V_2 + Q$$

$$\Rightarrow \boxed{V = \frac{C_1}{C_1 + C_2}V_1 + \frac{C_2}{C_1 + C_2}V_2 + \frac{Q}{C_1 + C_2}}$$

- The voltage on the middle node is a weighted sum of the two input voltages.
- If node V is really floating, then the inputs couple into the floating node all the way down to DC!
- The charge Q linearly offsets the V. The charge can be adjusted either optically or electronically.

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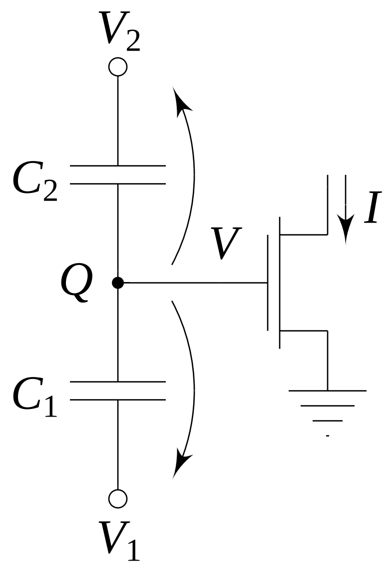
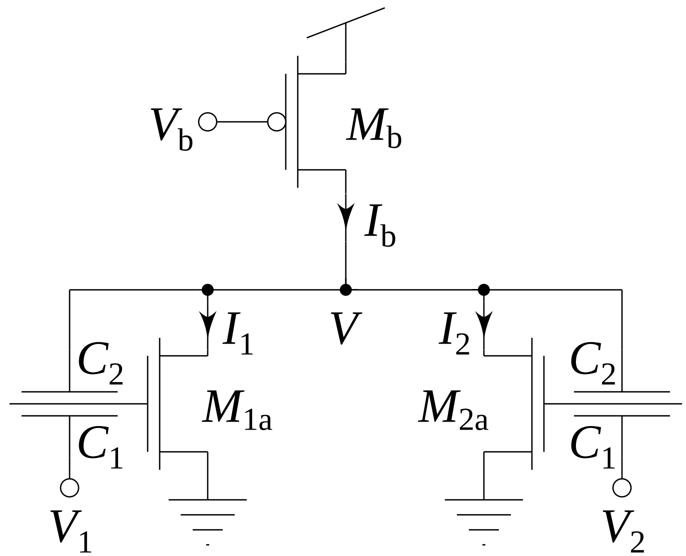
Floating-Gate MOS Transitors



- The capacitors C_1 and C_2 are called *control gates*.
- If floating-gate voltage, V, is a weighted sum of the control-gate voltages.
- The floating-gate charge, Q, can be thought of as giving us a programmable threshold voltage.

A Folded Floating-Gate Differential Pair



Differential-pair intuition:

- $I_1 = f(V_1, V)$ and $I_2 = f(V_2, V)$, where f is expansive.
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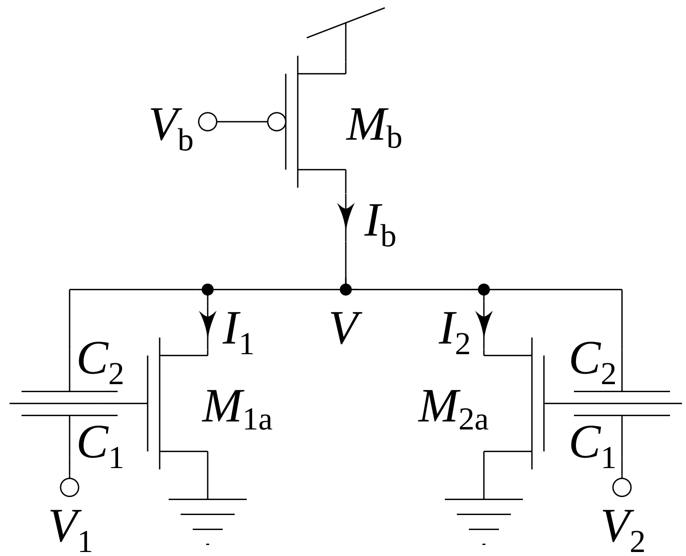
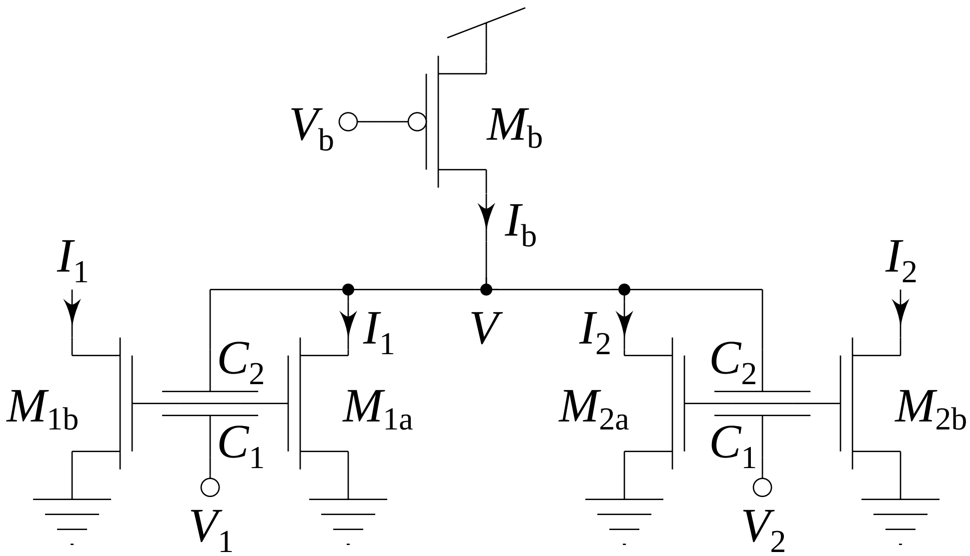


Differential-pair intuition:

- $I_1 = f(V_1, V)$ and $I_2 = f(V_2, V)$, where f is expansive.
- V adjusts itself so that $I_1 + I_2 \to I_b$.

Sign difference permits us to *fold* M_b relative to M_1 and M_2.

A Folded Floating-Gate Differential Pair



Differential-pair intuition:

- $I_1 = f(V_1, V)$ and $I_2 = f(V_2, V)$, where f is expansive.
- V adjusts itself so that $I_1 + I_2 \to I_b$.

M_{1b} and M_{2b} provide mirror copies of I_1 and I_2.

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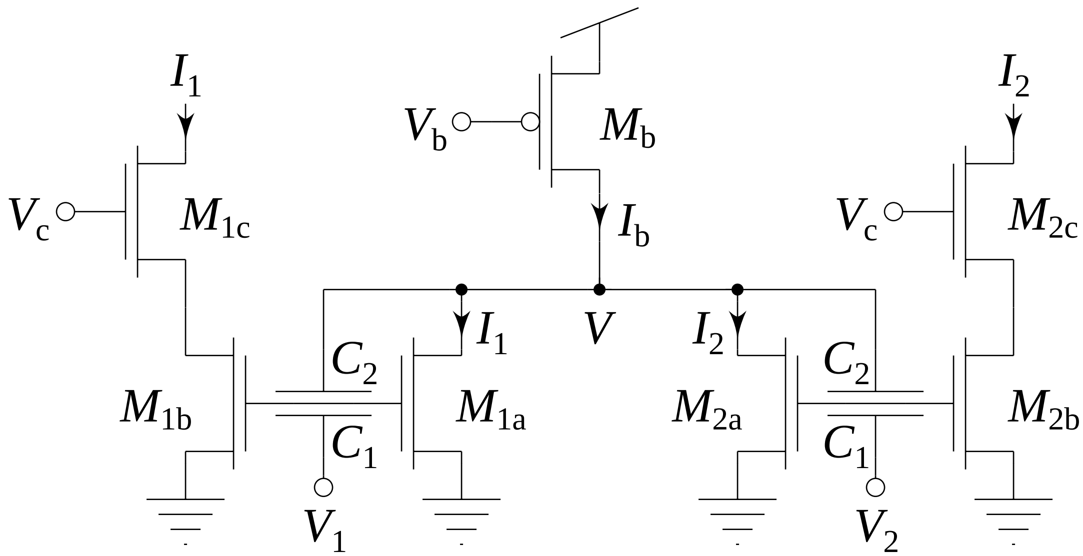
A Folded Floating-Gate Differential Pair

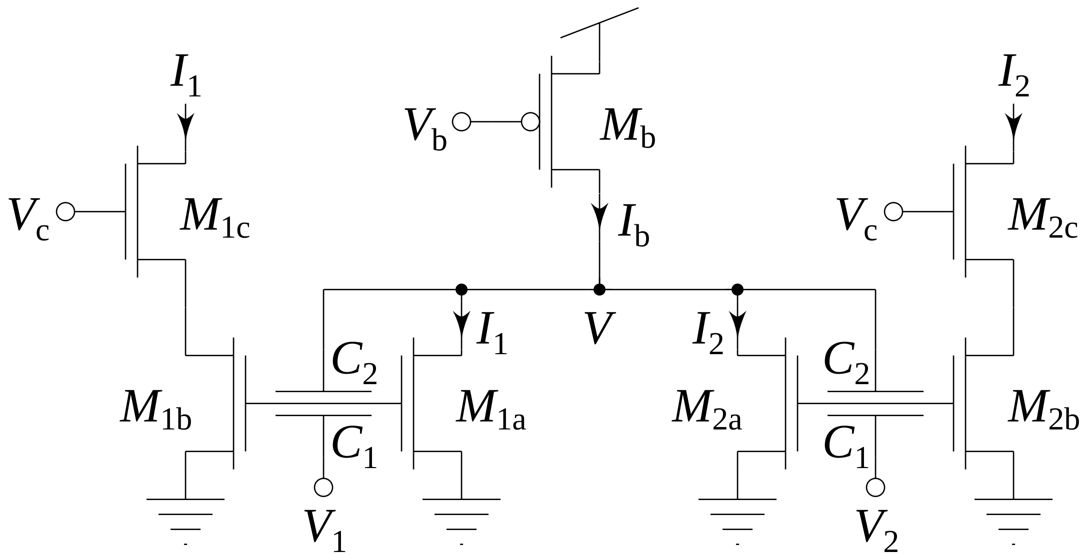


Differential-pair intuition:

- $I_1 = f(V_1, V)$ and $I_2 = f(V_2, V)$, where f is expansive.
- V adjusts itself so that $I_1 + I_2 \rightarrow I_b$.

M_{1c} and M_{2c} mitigate the C_{gd}'s of transistors M_{1b} and M_{2b}.

A Folded Floating-Gate Differential Pair



- C_1 sets the linear range and transconductance gain.
- C_2 controls by how much V changes in response to changes in either V_{cm} or I_b.
- Input and output voltage ranges are from rail-to-rail.
- Transconductance gain nearly constant with V_{cm}.

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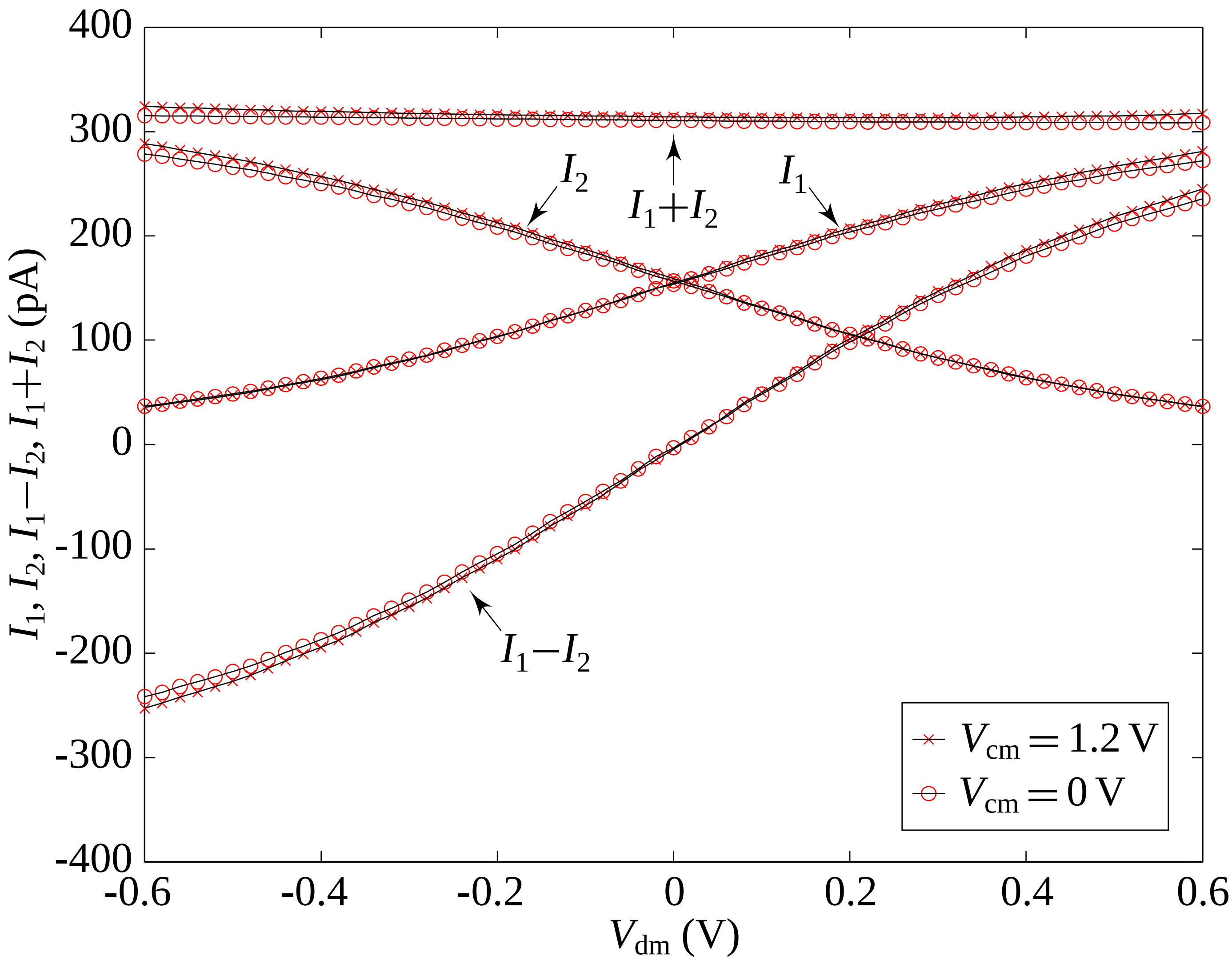
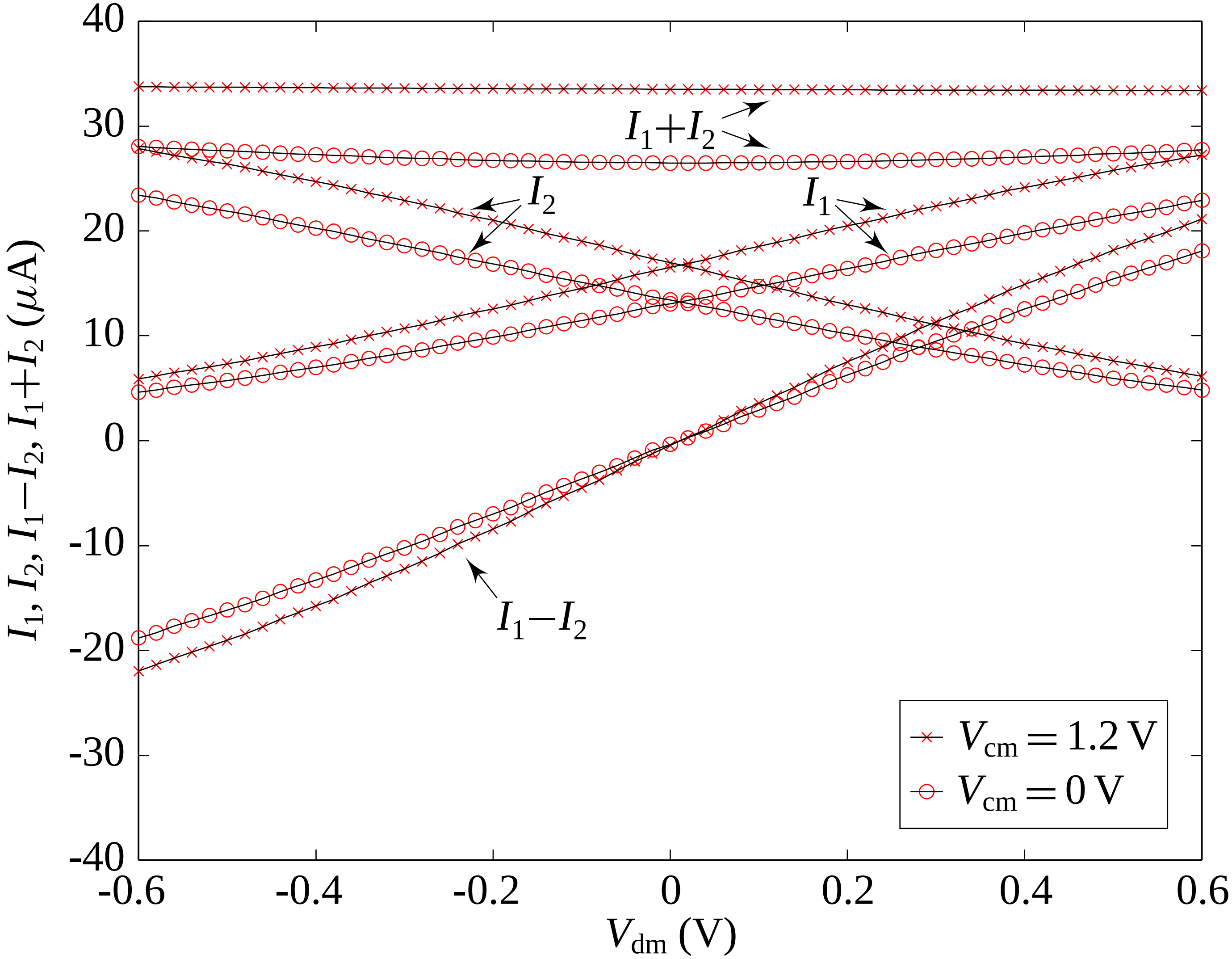
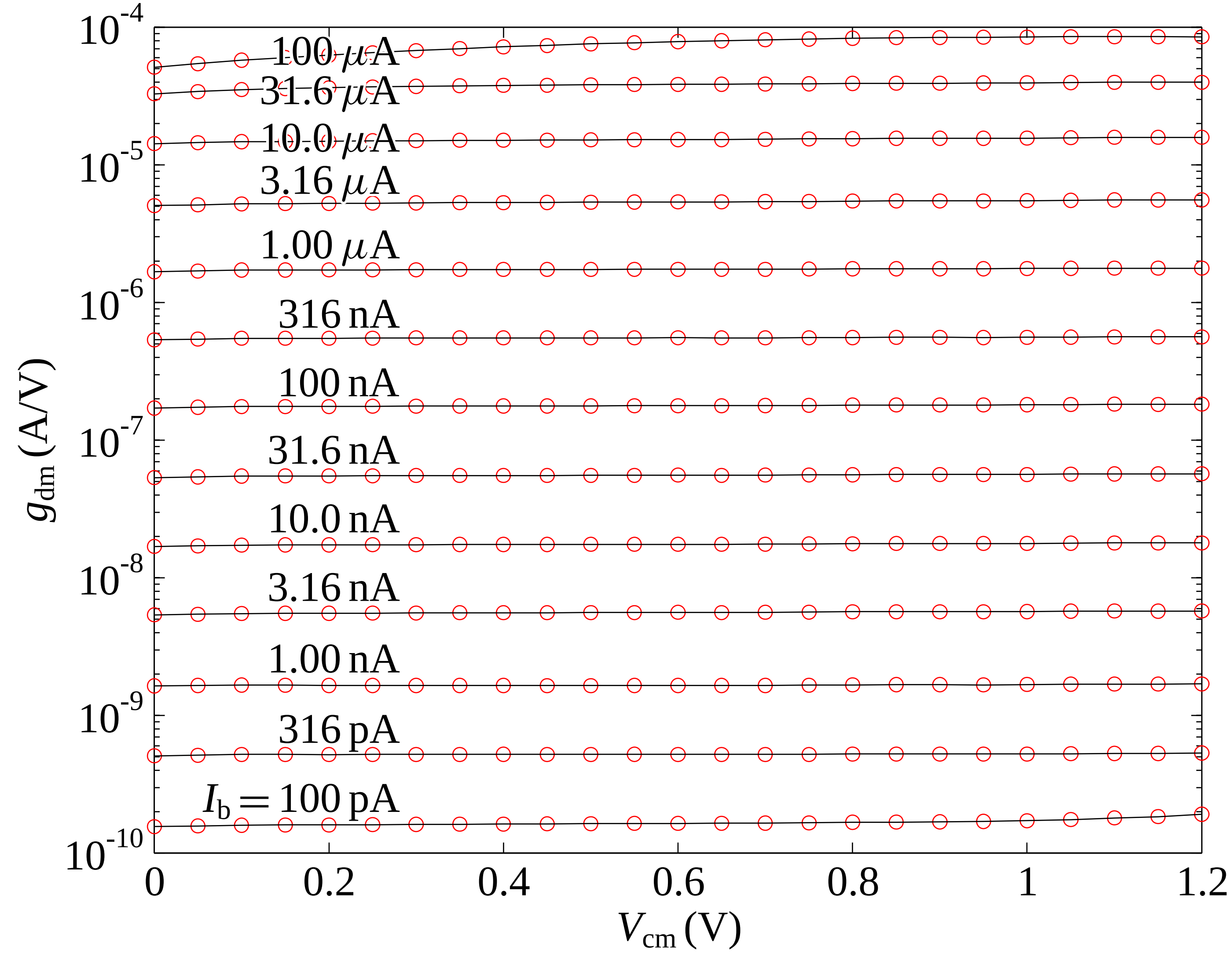
Output Currents vs. V_{dm} ($I_b = 316\,\mathrm{pA}$)



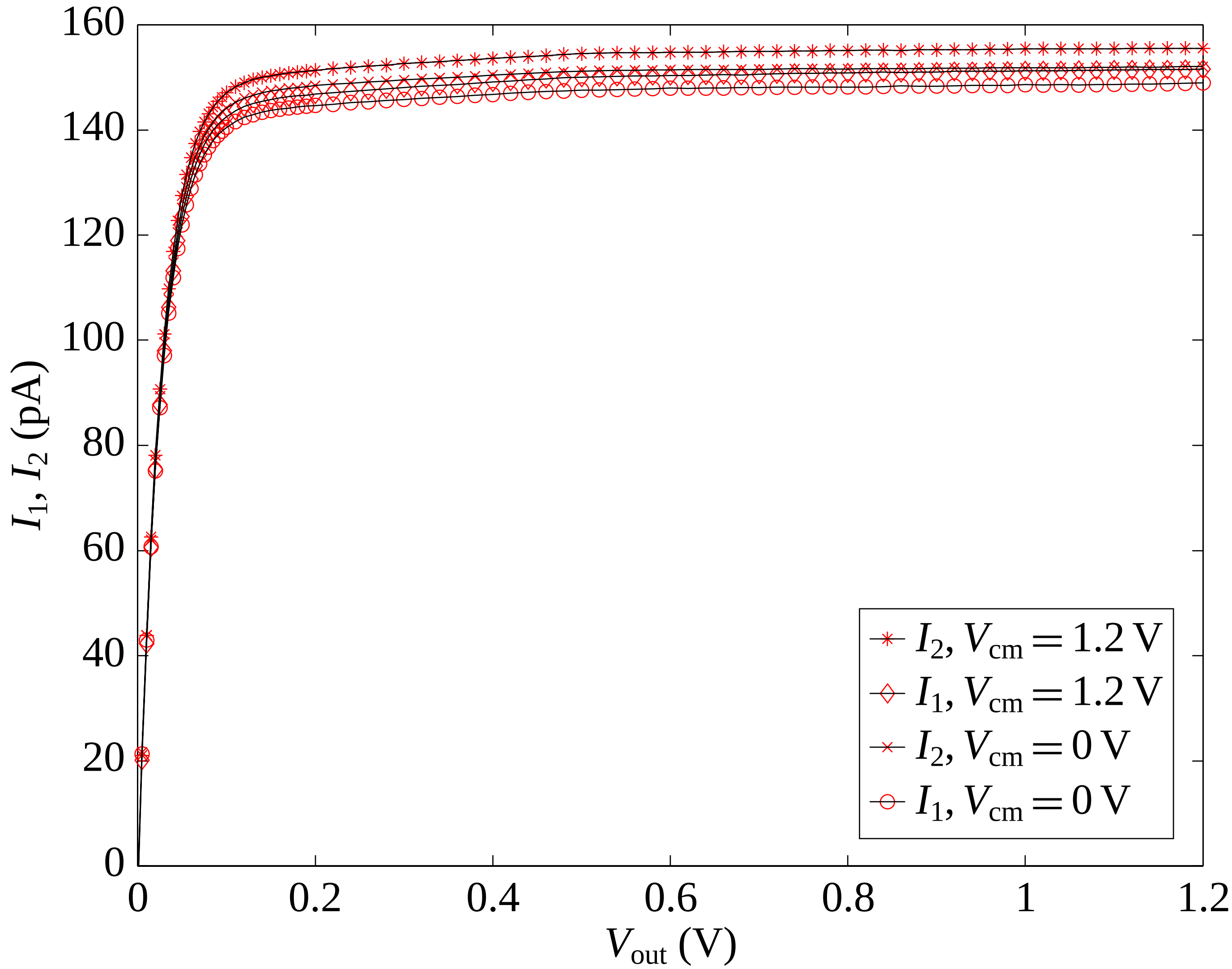
Output Currents vs. V_{dm} ($I_b = 31.6\,\mu A$)



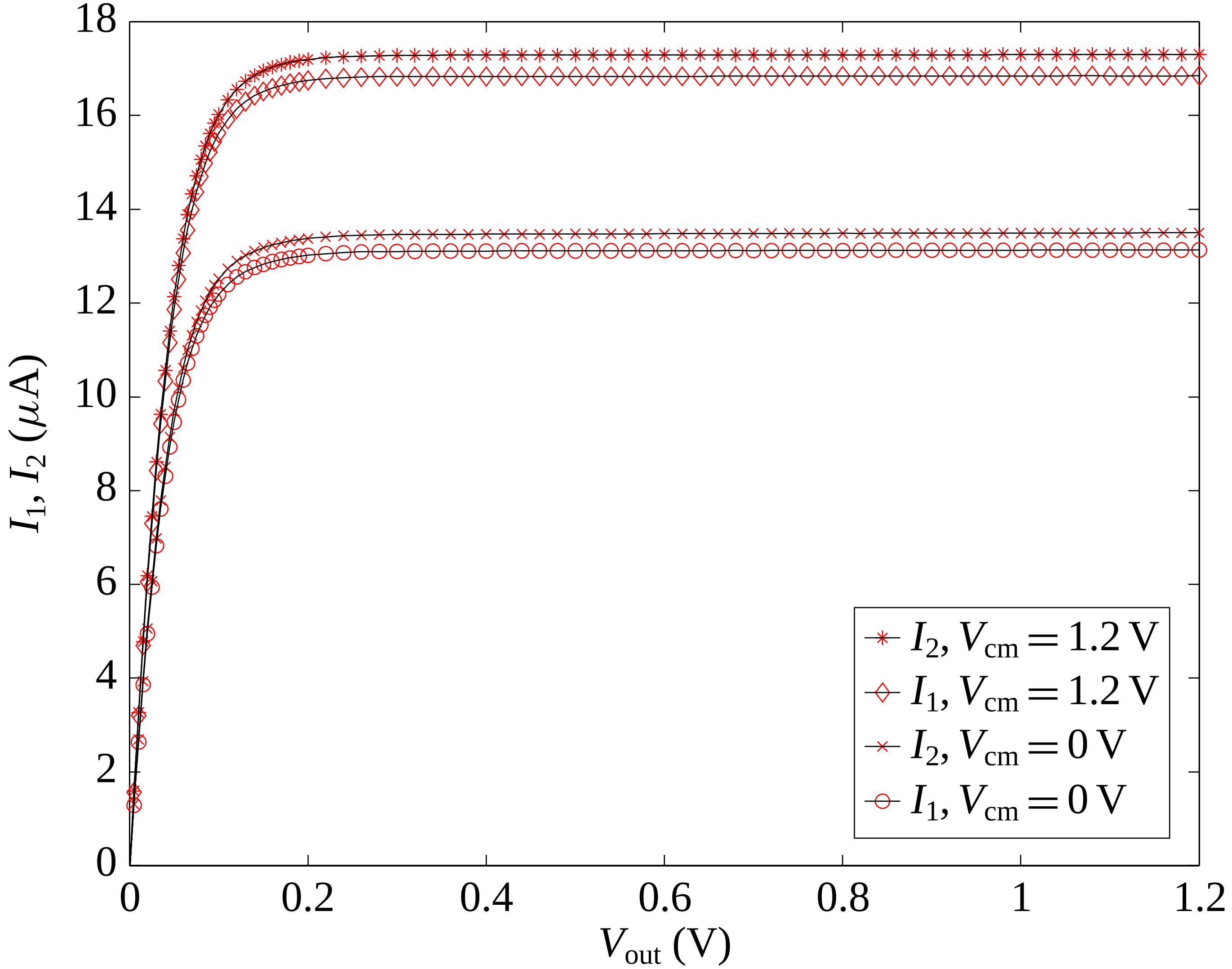
Transconducance Gain vs. V_{cm}



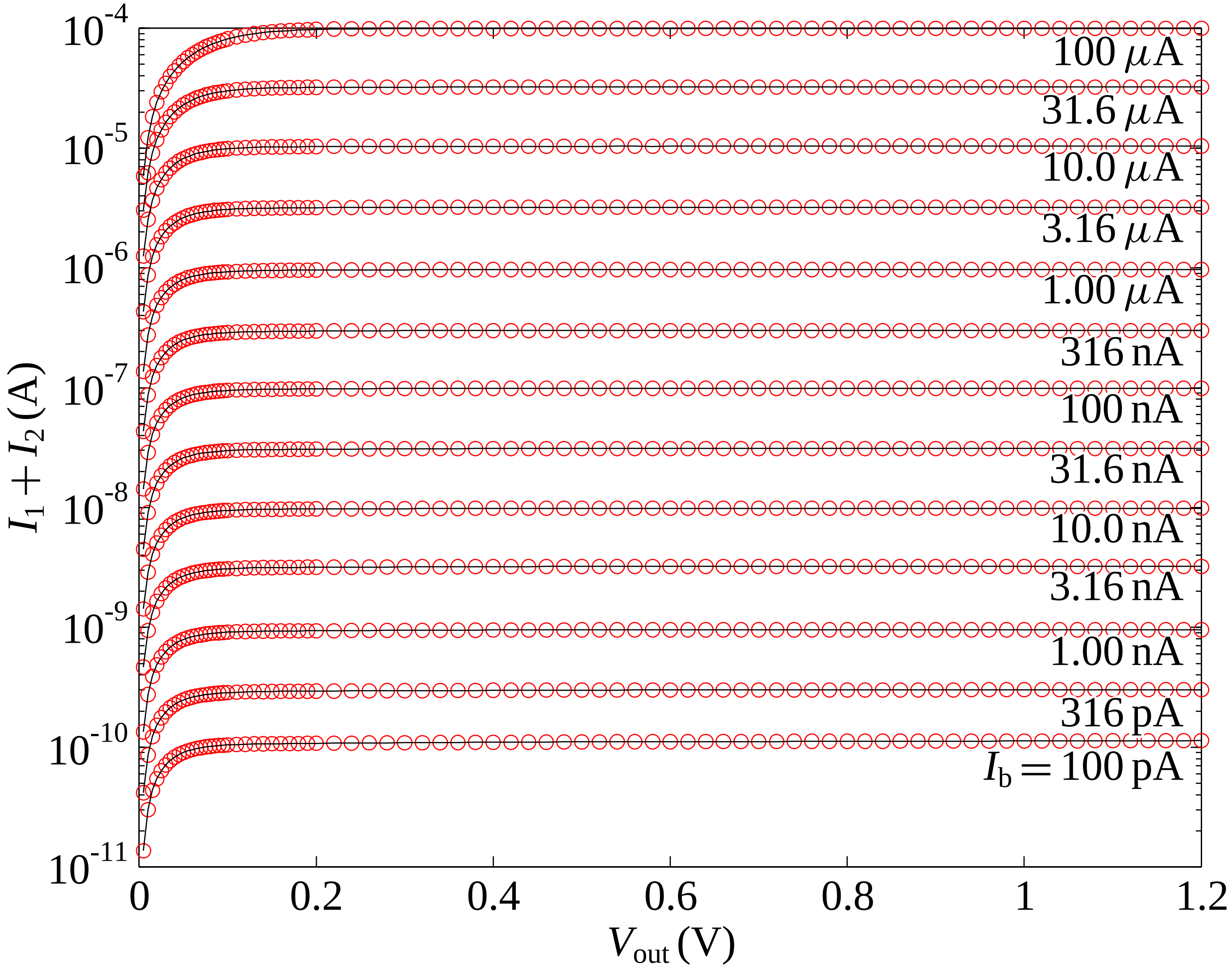
Output Currents vs. V_{out} ($I_b = 300\,\text{pA}$)



Output Currents vs. V_{out} ($I_b = 31.6\,\mu A$)



Common-Mode Output Current vs. V_{out}



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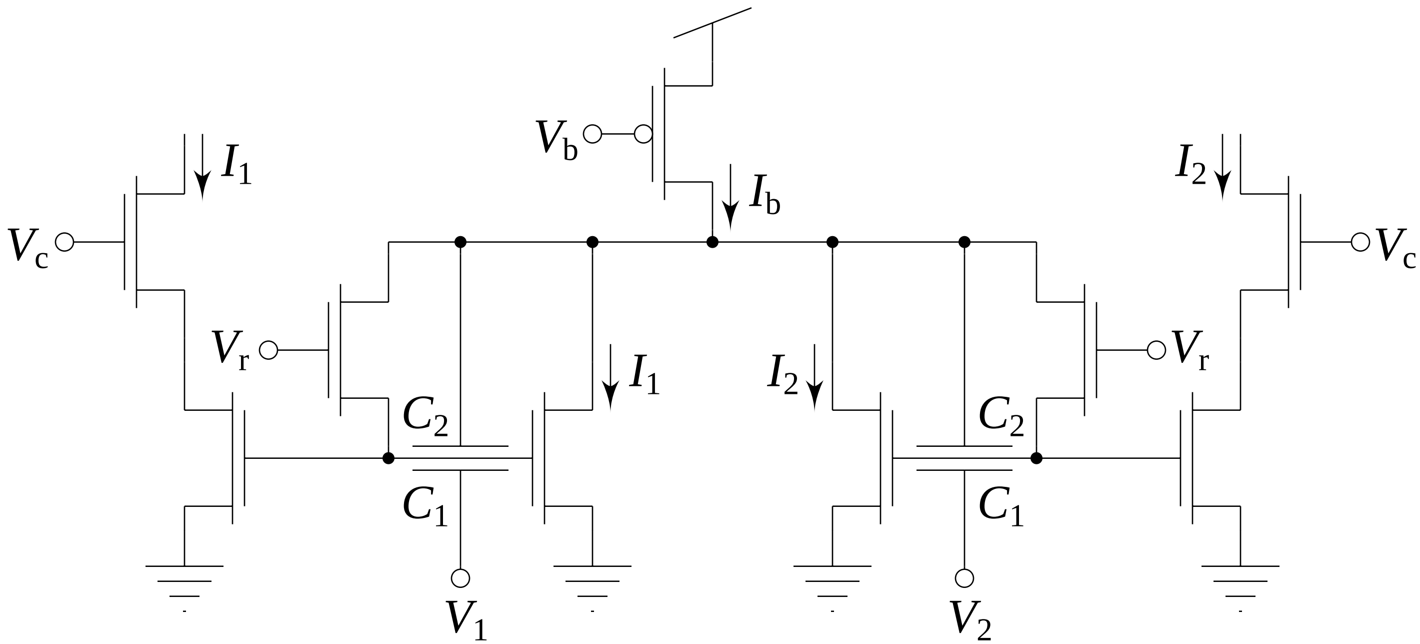
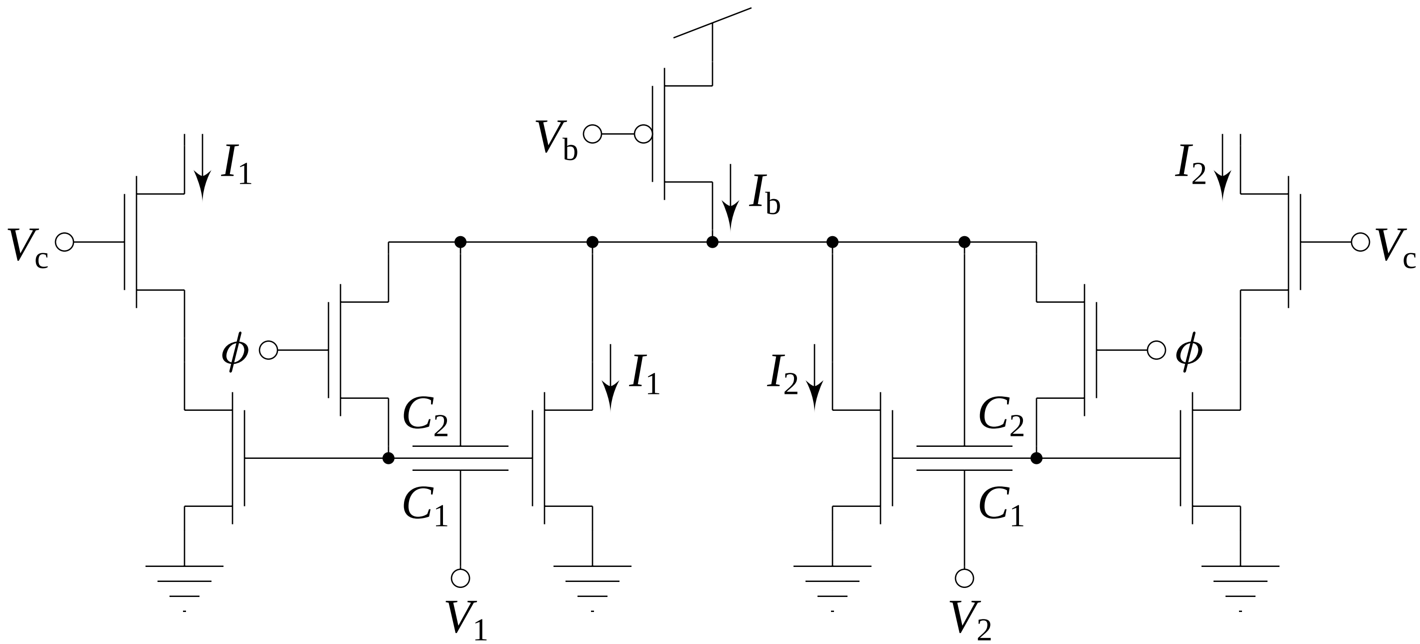
Variations on a Theme...



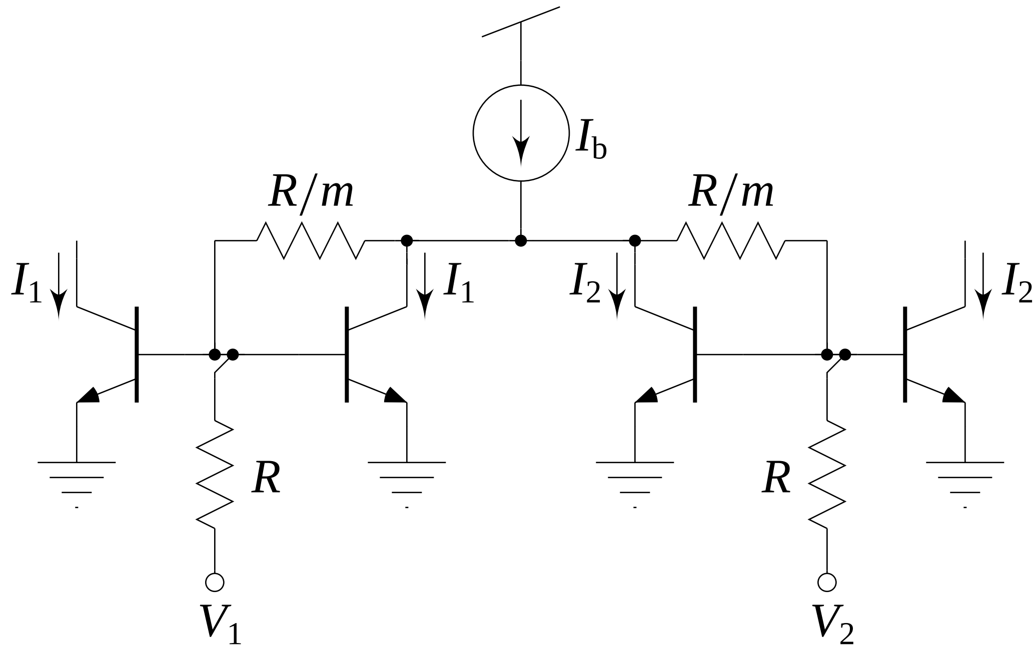
- Add resistive feedback to the floating gates in parallel with C_2 controlled by V_r.
- Resistive path introduces a first-order low-frequency roll-off whose corner frequency is set by C_T and V_r.
- At DC, the circuit is a pair of current mirrors sharing I_b equally. Above the corner, it acts as the FG circuit.

Variations on a Theme...



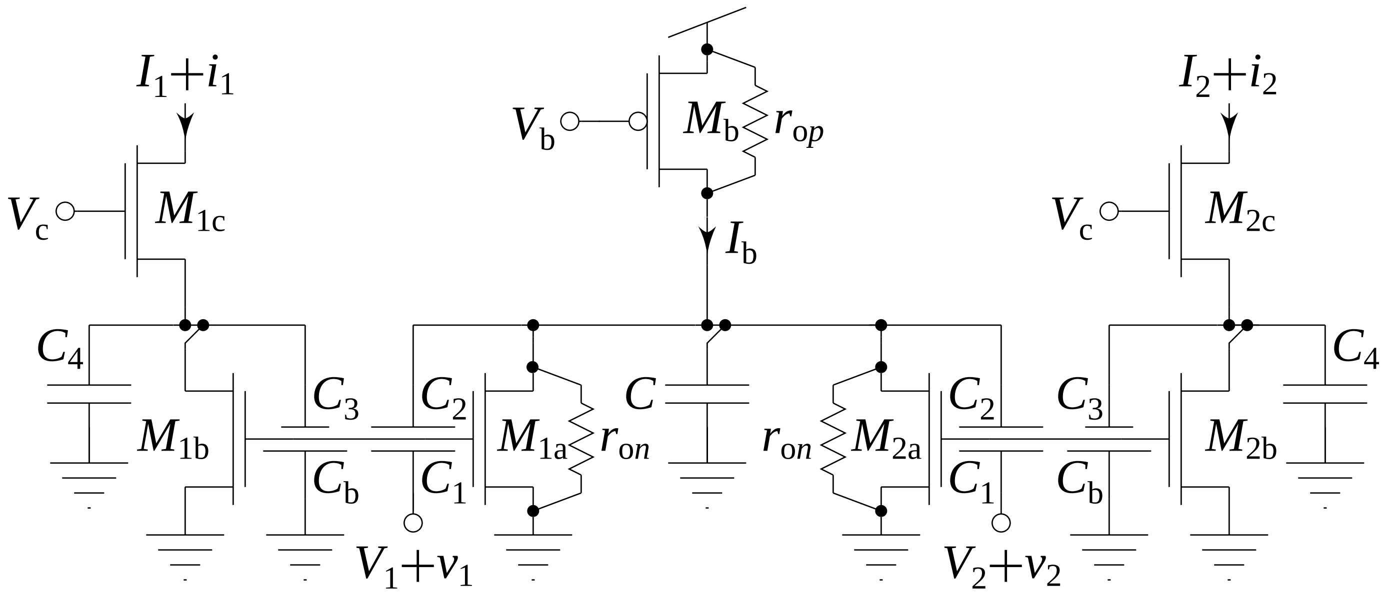
- Use feedback transistors as switches gated by a clock signal, ϕ.
- When ϕ is high, the circuit rebalances itself. When ϕ is low, the circuit acts just like the FG circuit.
- Injected charge is rejected as a common-mode signal if it matches on both sides.

Variations on a Theme...



- Rail-to-rail input common-mode range, wide output voltage swing.
- Acts very much like an emitter-degenerated bipolar differential pair.
- Input resistance primarily determined by *R* because base nodes are basically clamped by shunt feedback.

Incremental High-Frequency Analysis

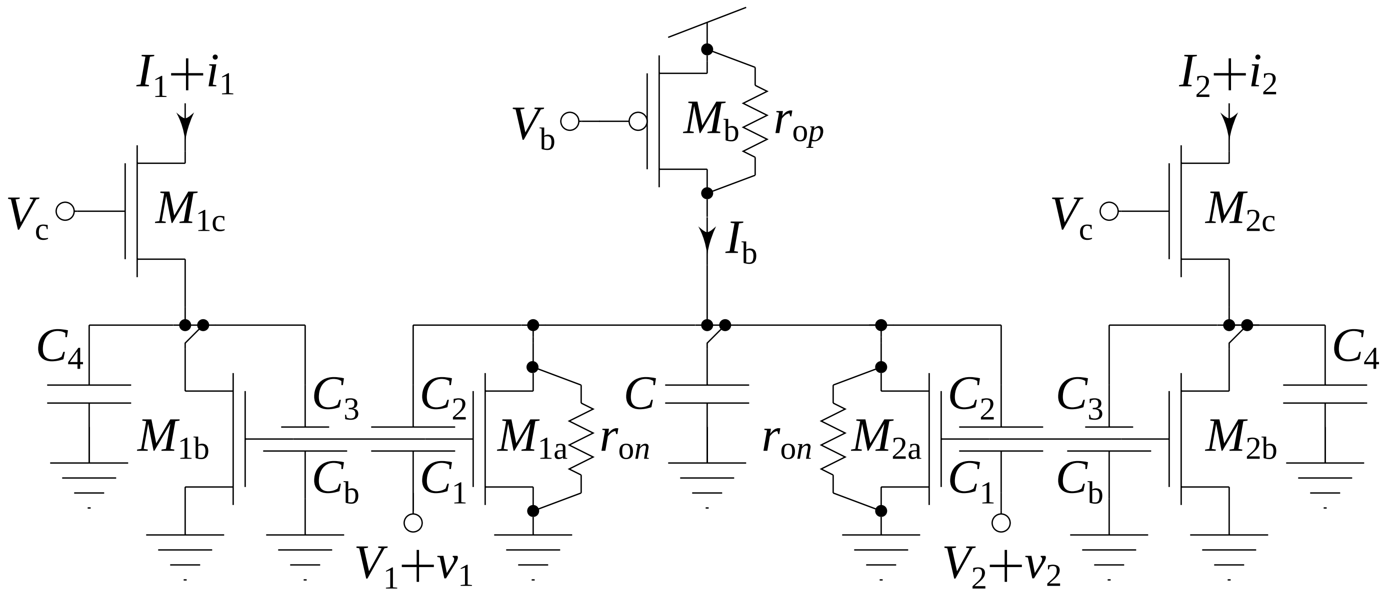


- Given that $g_m\left(r_{on}\|2r_{op}\right)\gg 1$ and $C_3 \ll C_2$, we can show that

$$i_{dm} \equiv i_1 - i_2 = g_m \frac{C_1}{C_T} \frac{1 - sC_3/g_m}{1 + s(C_3 + C_4)/g_s} v_{dm}$$

where $C_T \equiv C_1 + C_2 + C_3 + C_b$.

Incremental High-Frequency Analysis

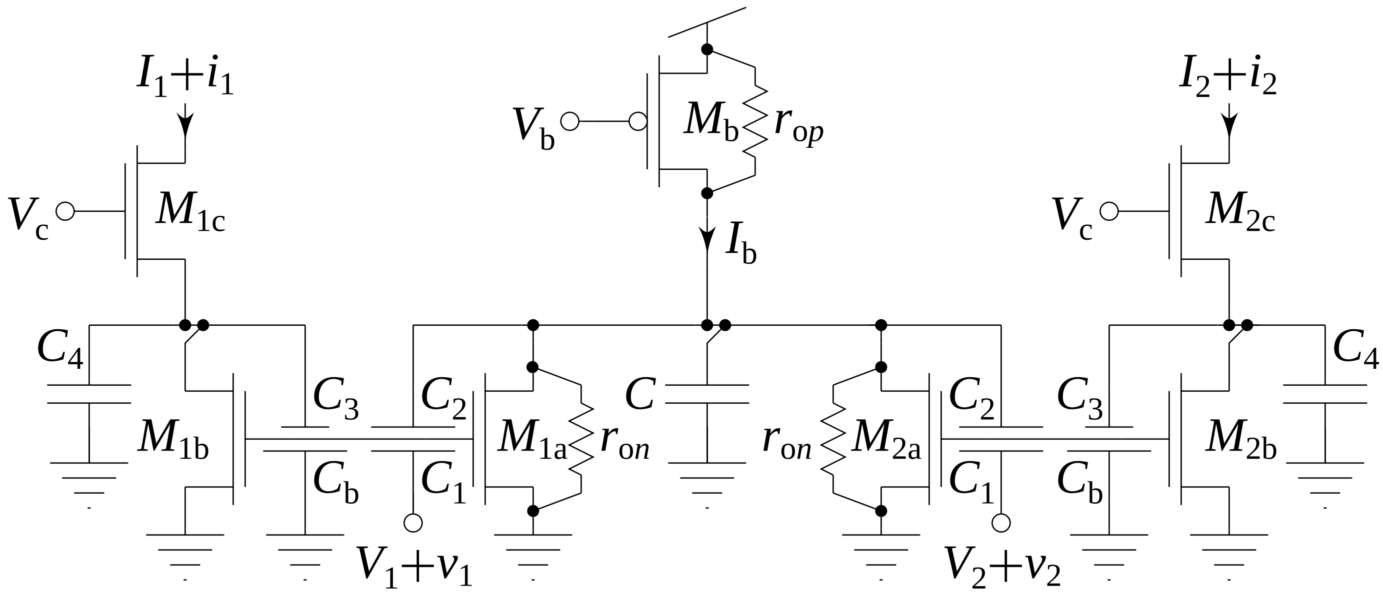


...and that

$$i_{cm} \equiv \frac{i_1 + i_2}{2}$$

$$= \frac{C_1/C_2}{r_{on}\|2r_{op}} \frac{(1 - sC_3/g_m)\left(1 + s\left(r_{on}\|2r_{op}\right)(C_2 + C/2)\right)}{(1 + s(C_3 + C_4)/g_s)\left(1 + s\left(C_2\|(C_1 + C_3 + C_b)\right)/(g_m C_2/C_T)\right)} v_{cm}$$

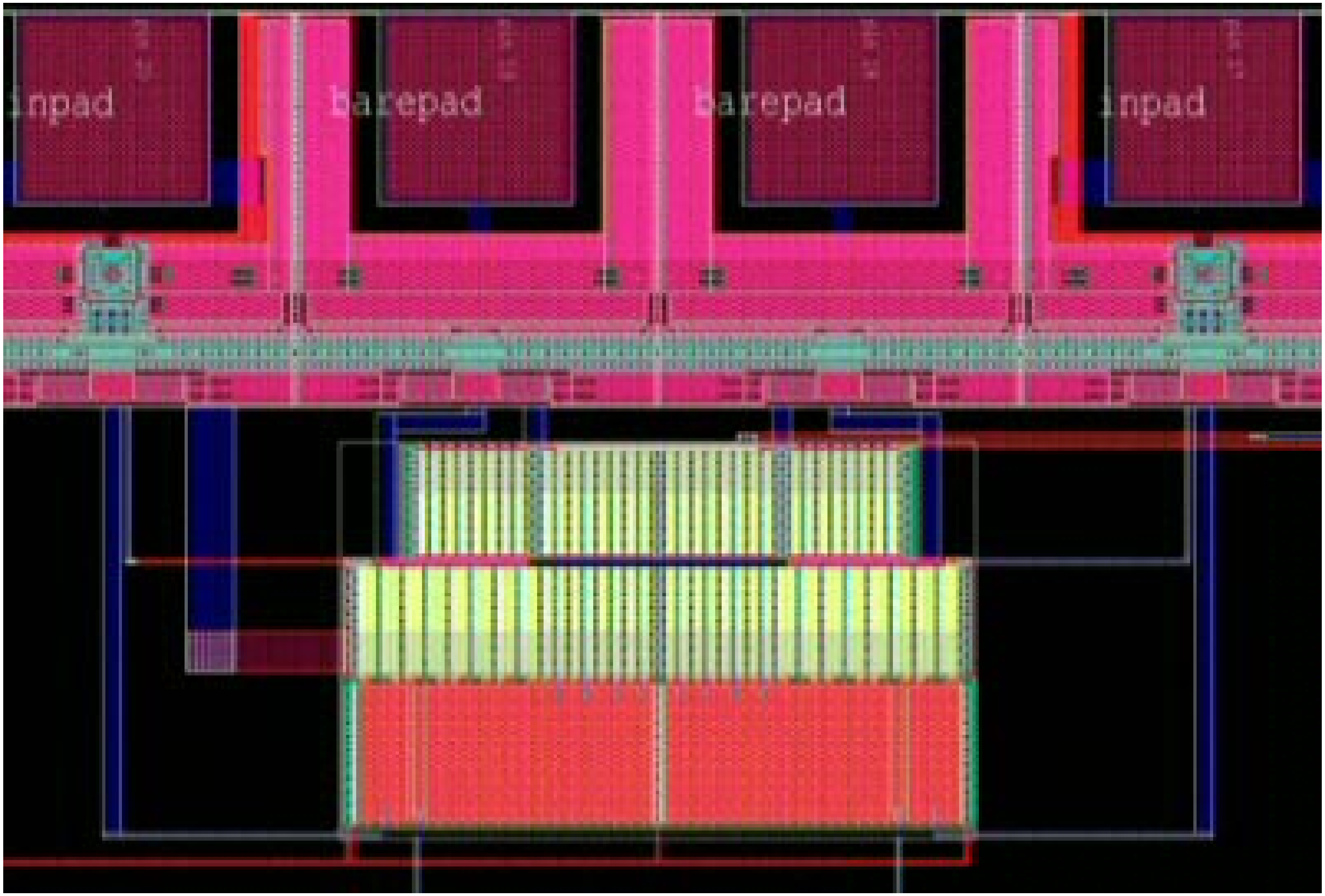
Incremental High-Frequency Analysis



...and so

$$\text{CMRR} \equiv \frac{i_{dm}/v_{dm}}{i_{cm}/v_{cm}} = g_m\left(r_{on}\|2r_{op}\right)\frac{C_2}{C_T}\frac{\left(1+s\left(C_2\|(C_1+C_3+C_b)\right)/(g_m C_2/C_T)\right)}{\left(1+s\left(r_{on}\|2r_{op}\right)(C_2+C/2)\right)}$$

Folded FGMOS Differential Pair Layout



Chip Photomicrograph