A Low-Voltage MOS Cascode Current Mirror for All Current Levels

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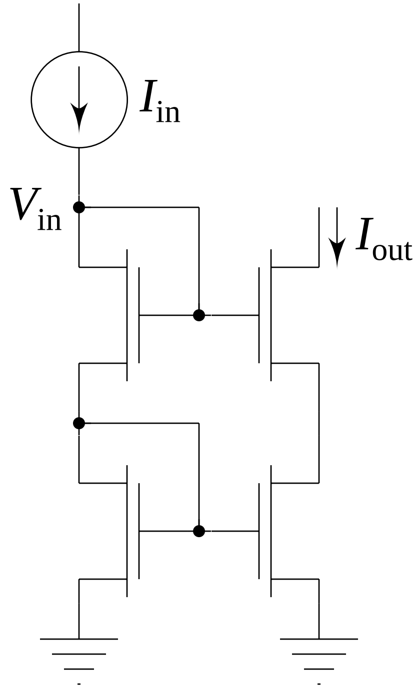
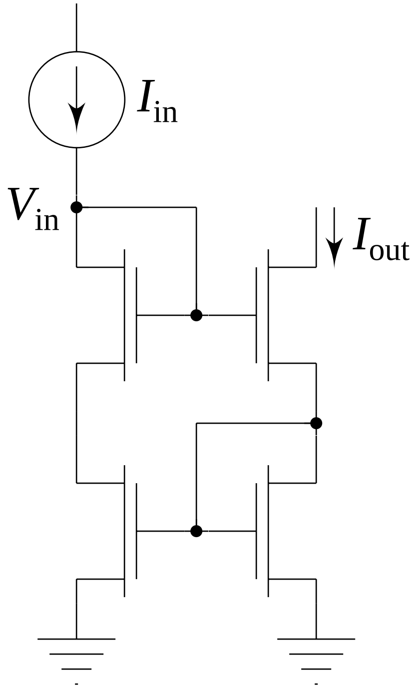
Cascode Mirrors of Yore With Low Systematic Transfer Errors

- Each of these mirrors is self biasing, has a high output impedance, and provides a low systematic transfer error.
- Each requires an input voltage of two diode drops.
- Each has an output compliance voltage of a diode drop plus a saturation voltage.
- Neither is suitable for use with a low power supply voltage.



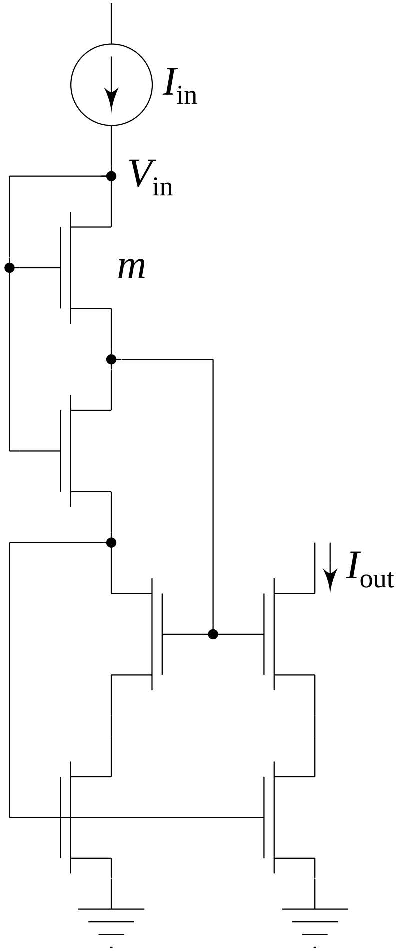
Stacked



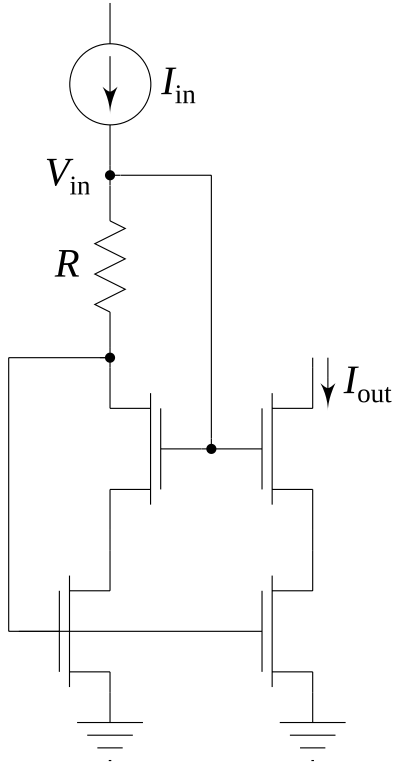
Super Wilson

Wide-Swing Cascode Mirrors With Low Systematic Transfer Error

- Each of these mirrors is self biasing, has a high output impedance, and provides a low systematic transfer error.
- Each has an output compliance voltage of two saturation voltages.
- The Sooch mirror requires an input voltage of two diode drops, which makes it unsuitable for low-voltage applications.
- The Brooks-Rybicki mirror requires an input voltage of a diode drop plus a saturation voltage, but requires a different value of R for every I_{in}.



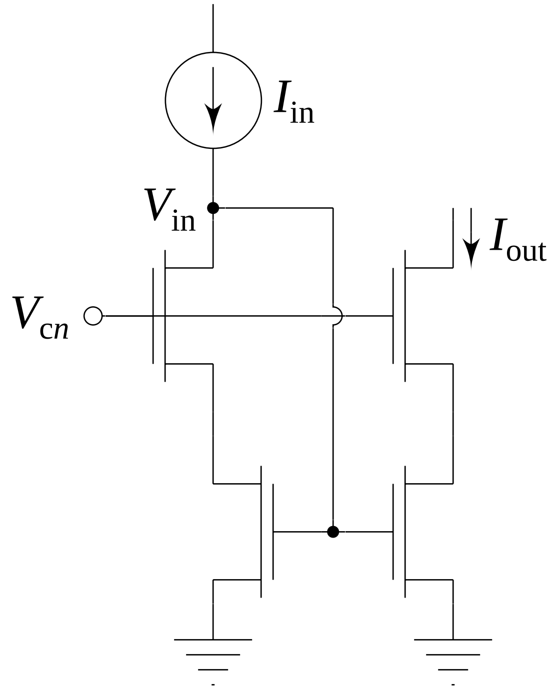
Sooch



Brooks & Rybicki

Wide-Swing Cascode Mirrors With Low Systematic Transfer Error

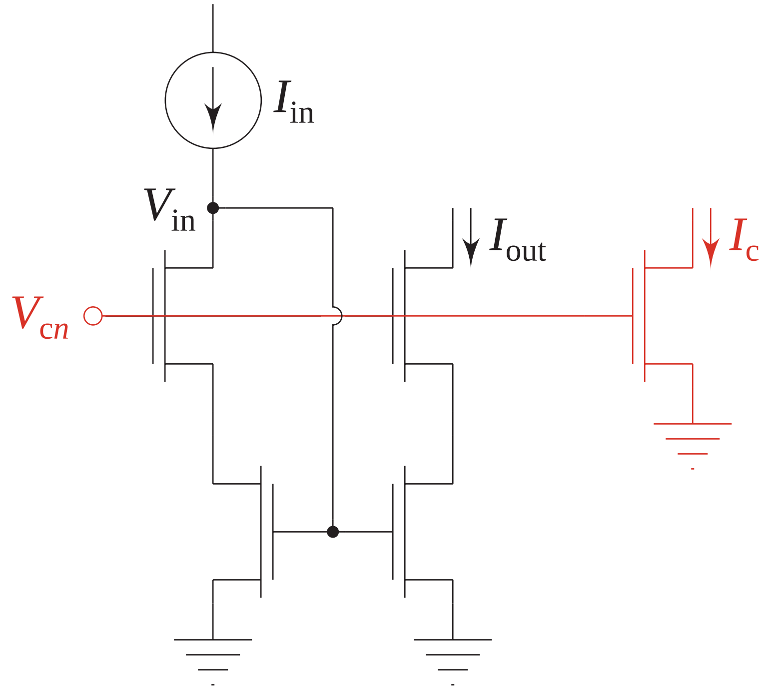
- To facilitate low-voltage operation, we can remove the cascode bias-voltage generation from the input branch.
- The output compliance voltage remains two saturation voltages.
- The input voltage becomes a diode drop, comparable to that of a simple mirror.



Babanezhad & Gregorian

Wide-Swing Cascode Mirrors With Low Systematic Transfer Error

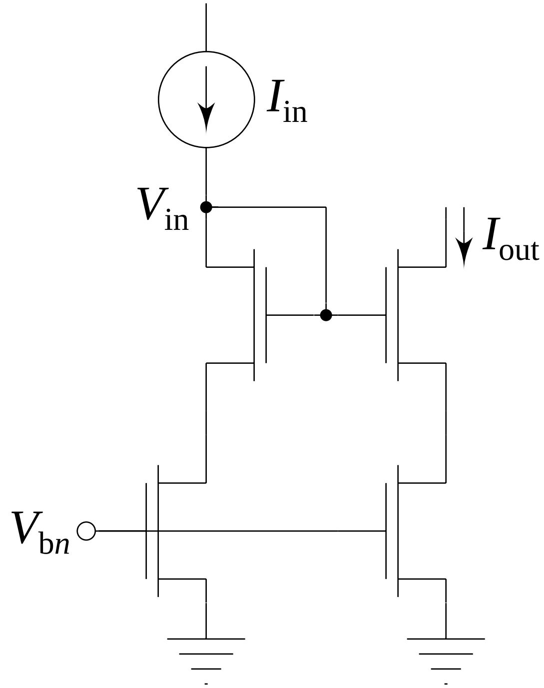
- To facilitate low-voltage operation, we can remove the cascode bias-voltage generation from the input branch.
- The output compliance voltage remains two saturation voltages.
- The input voltage becomes a diode drop, comparable to that of a simple mirror.
- I_{in} is limited to I_{c} and the optimal value of V_{cn} depends on I_{in}, which sometimes requires us to generate V_{cn} adaptively.



Babanezhad & Gregorian

Wide-Swing Cascode Mirrors With Low Systematic Transfer Error

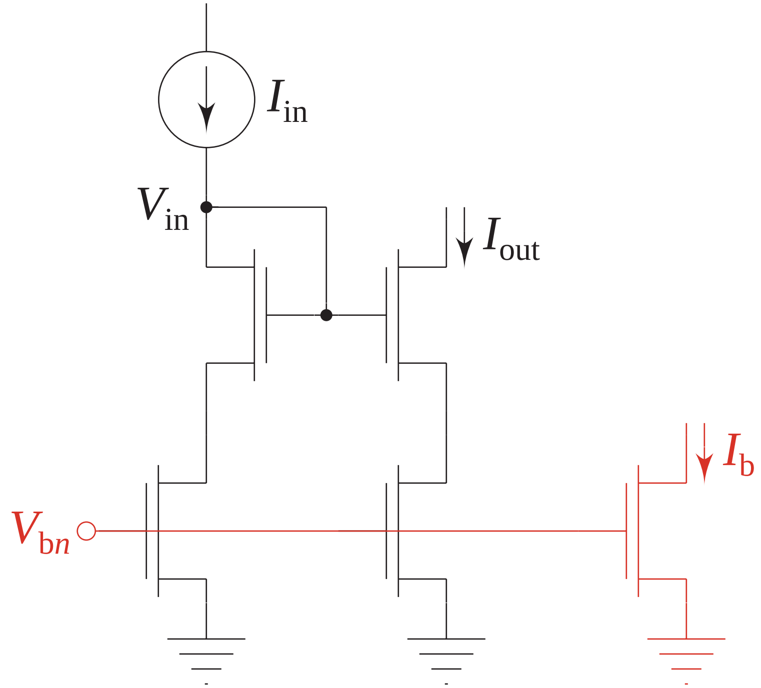
- Mulder *et al.* recently proposed a wide-swing cascode mirror comprising a simple mirror with source degeneration via ohmic MOS transistors.
- The output compliance voltage remains two saturation voltages.
- The input voltage is a diode drop plus a saturation voltage.



Mulder *et al.*

Wide-Swing Cascode Mirrors With Low Systematic Transfer Error

- Mulder *et al.* recently proposed a wide-swing cascode mirror comprising a simple mirror with source degeneration via ohmic MOS transistors.
- The output compliance voltage remains two saturation voltages.
- The input voltage is a diode drop plus a saturation voltage.
- I_{in} is limited to I_b and the optimal value of V_{bn} depends critically on I_{in}, which mandates that we generate V_{bn} adaptively.



Mulder *et al.*

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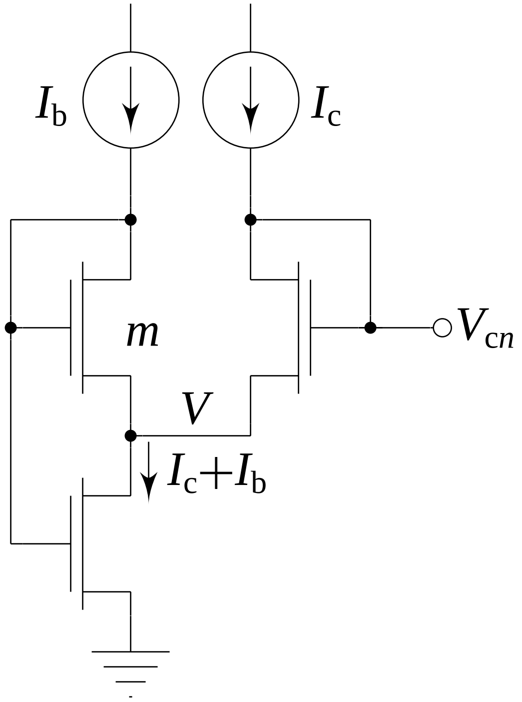
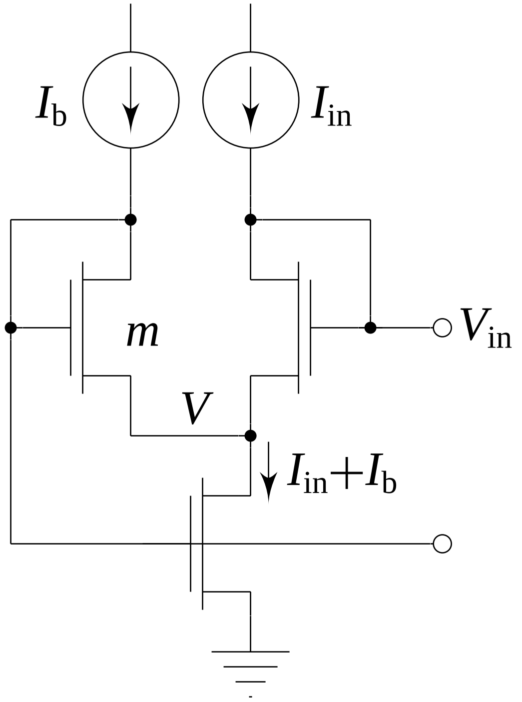
Development of a New Low-Voltage Cascode Current Mirror

- We recently presented a low-voltage cascode bias circuit that generates a V_{cn} appropriate for a unit-width transistor with a channel current of about I_c.
- The degree to which the bottom transistor is saturated depends on m and I_c/I_b—the larger these values, the closer V is to V_{DSsat}.
- V_{cn} is about a diode drop plus a saturation voltage.



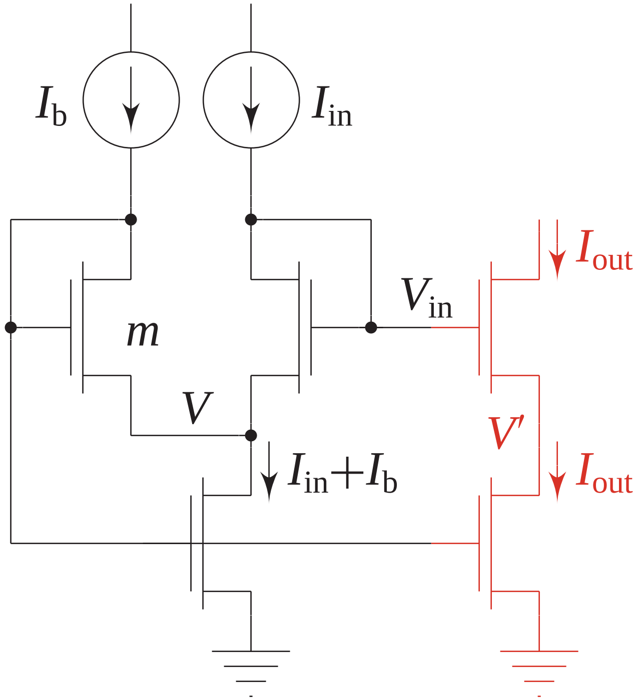
Development of a New Low-Voltage Cascode Current Mirror

- Suppose we take this circuit and make I_c the input current.



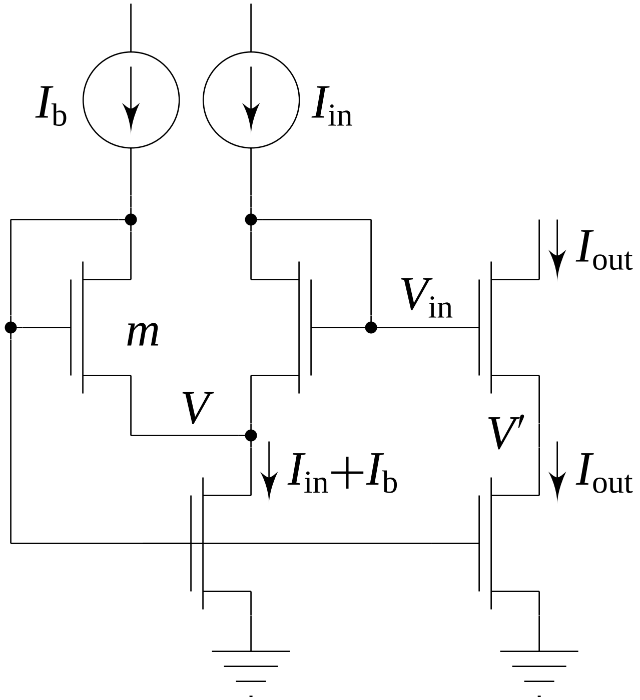
Development of a New Low-Voltage Cascode Current Mirror

- Suppose we take this circuit and make I_c the input current.
- Then, we produce an output current by adding two transistors, as shown.



Development of a New Low-Voltage Cascode Current Mirror

- Suppose we take this circuit and make I_c the input current.
- Then, we produce an output current by adding two transistors, as shown.
- In this mirror, V' will be slightly lower than V, giving rise to a systematic transfer errror. In fact, it is easy to see that $I_{in} < I_{out} < I_{in} + I_b$. If $I_{in} \gg I_b$, this systematic error is negligible.



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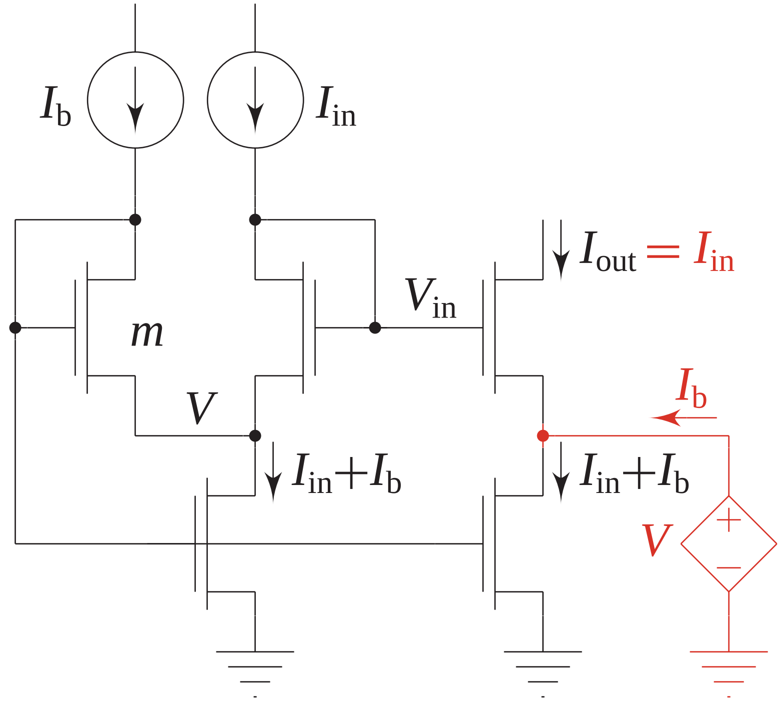
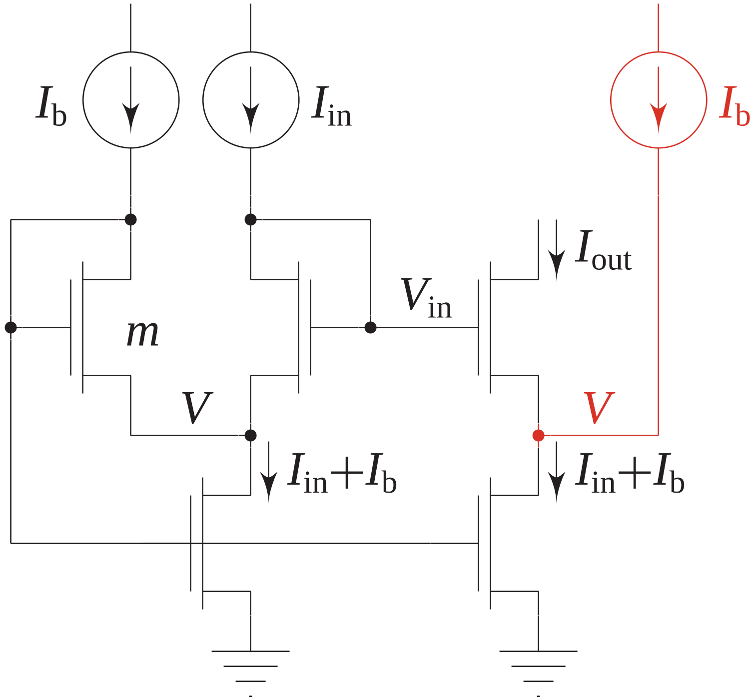
Development of a New Low-Voltage Cascode Current Mirror

- If we make V' equal to V, we could eliminate the systematic gain error, but we would effectively disable the cascode.



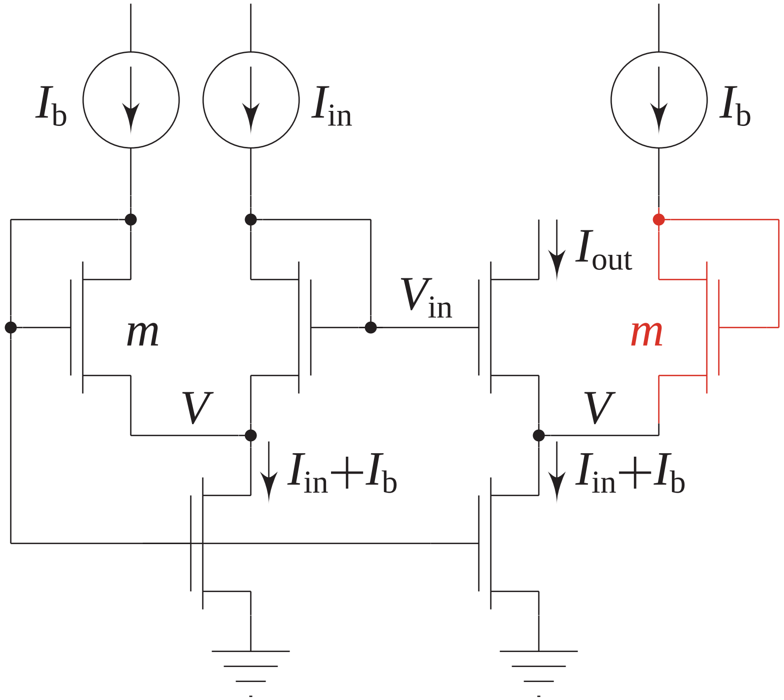
Development of a New Low-Voltage Cascode Current Mirror

- If we make V' equal to V, we could eliminate the systematic gain error, but we would effectively disable the cascode.
- Instead, we can inject another copy of I_b into node V', as shown.



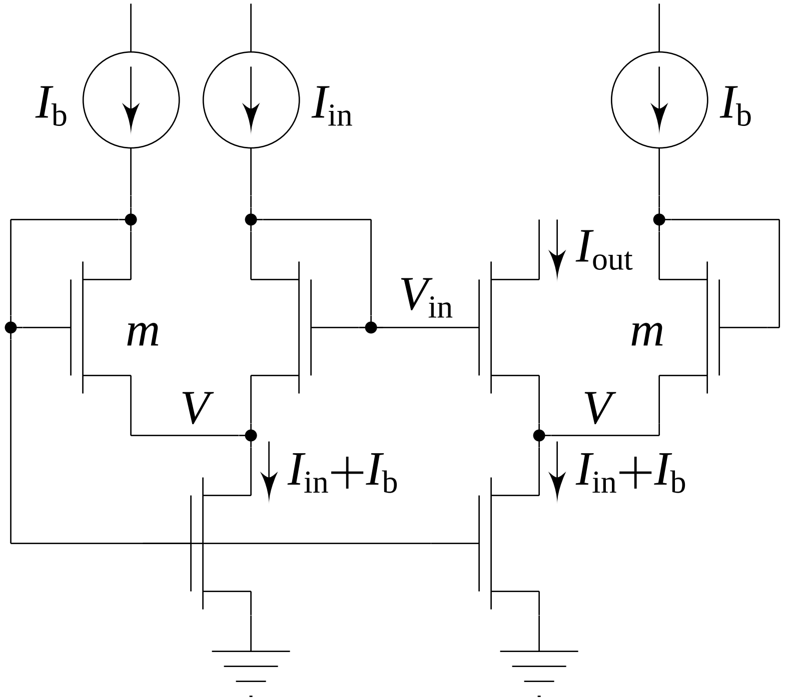
Development of a New Low-Voltage Cascode Current Mirror

- If we make V' equal to V, we could eliminate the systematic gain error, but we would effectively disable the cascode.
- Instead, we can inject another copy of I_b into node V', as shown.
- If I_b is generated by a saturated pMOS transistor, we can improve the circuit further by adding a diode-connected transistor of width m, as shown.

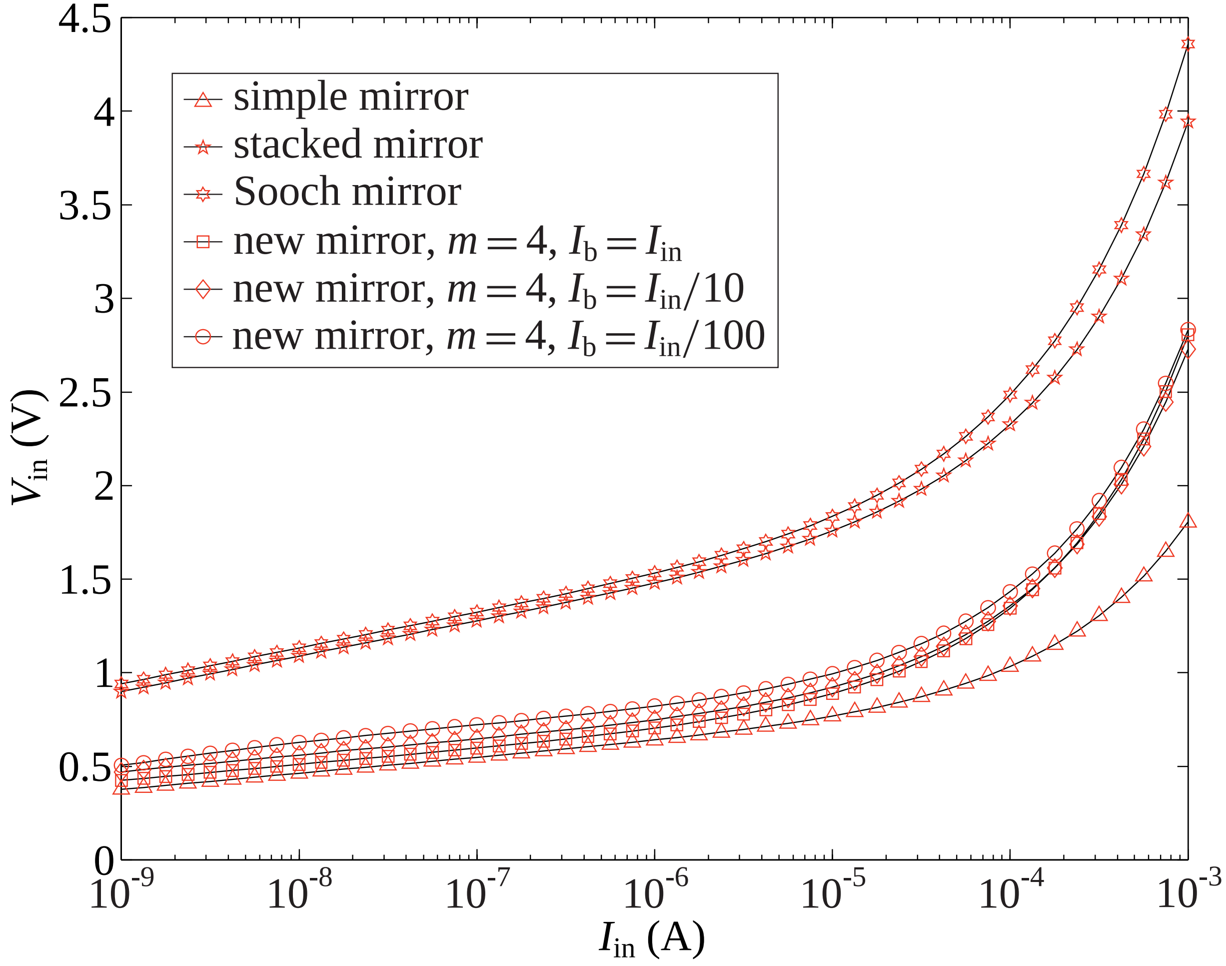


Development of a New Low-Voltage Cascode Current Mirror

- The resulting mirror has a low systematic transfer error and a high output impedance.
- The output compliance voltage of this mirror is two saturation voltages.
- The input voltage of this mirror is a diode drop plus a saturation voltage.
- The bias current, I_b, does not represent an upper limit on I_{in} and does not need to track I_{in} adaptively.



Experimental Results: Input Characteristics



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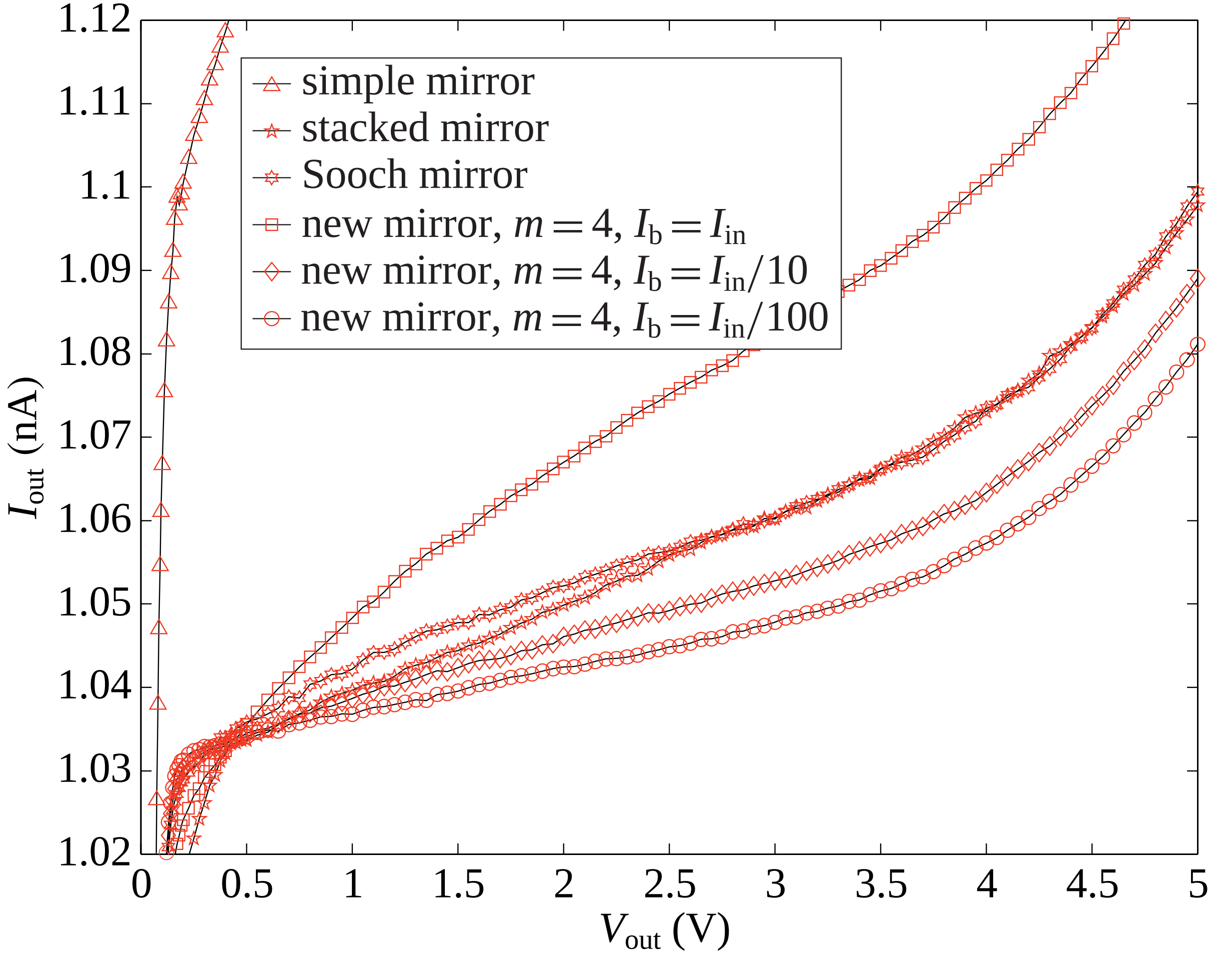
Experimental Results: Output Characteristics $I_{\text{in}} = 1.00\,\text{nA}$



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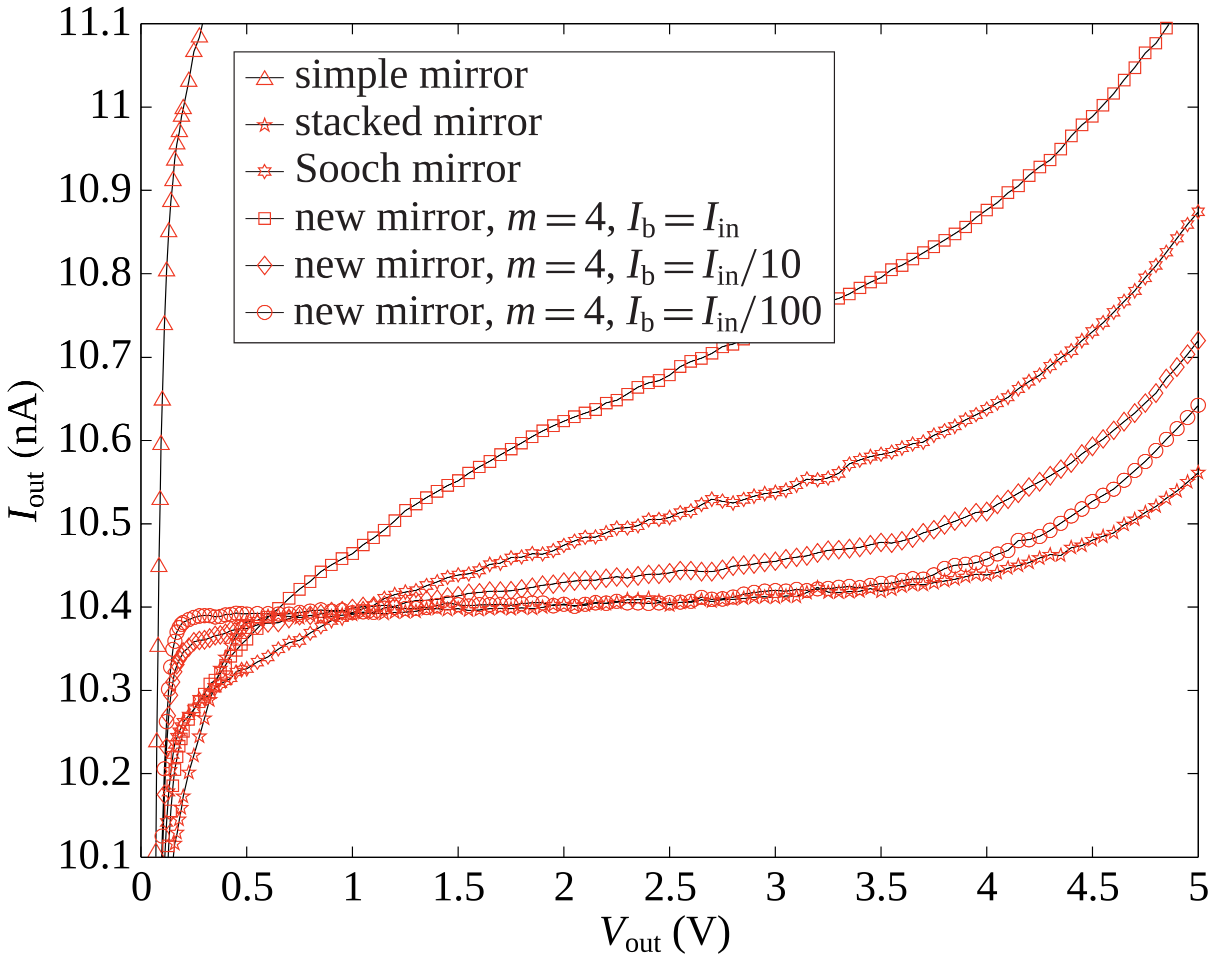
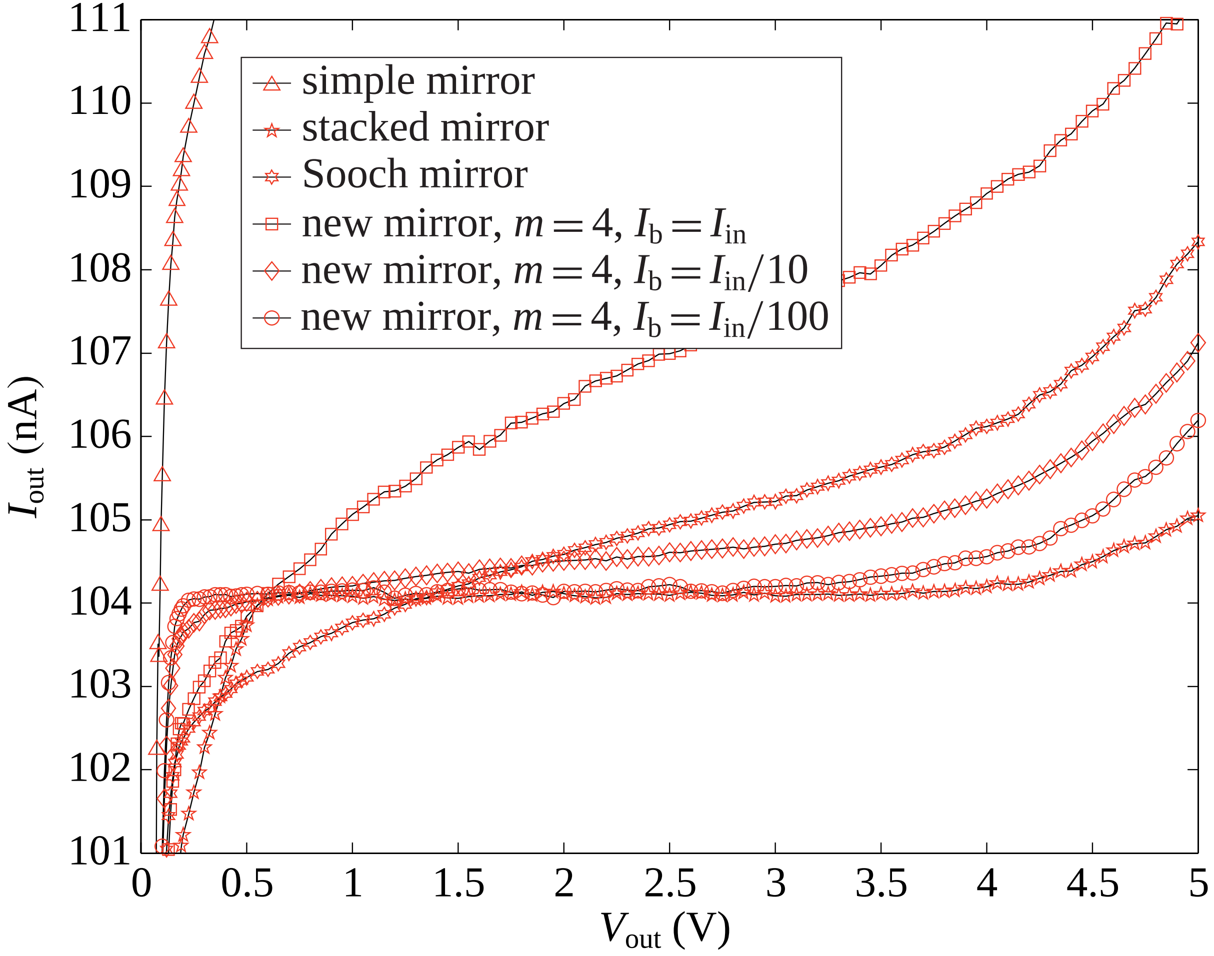
Experimental Results: Output Characteristics $I_{in} = 10.0\,\text{nA}$



Experimental Results: Output Characteristics $I_{in} = 100.$ nA



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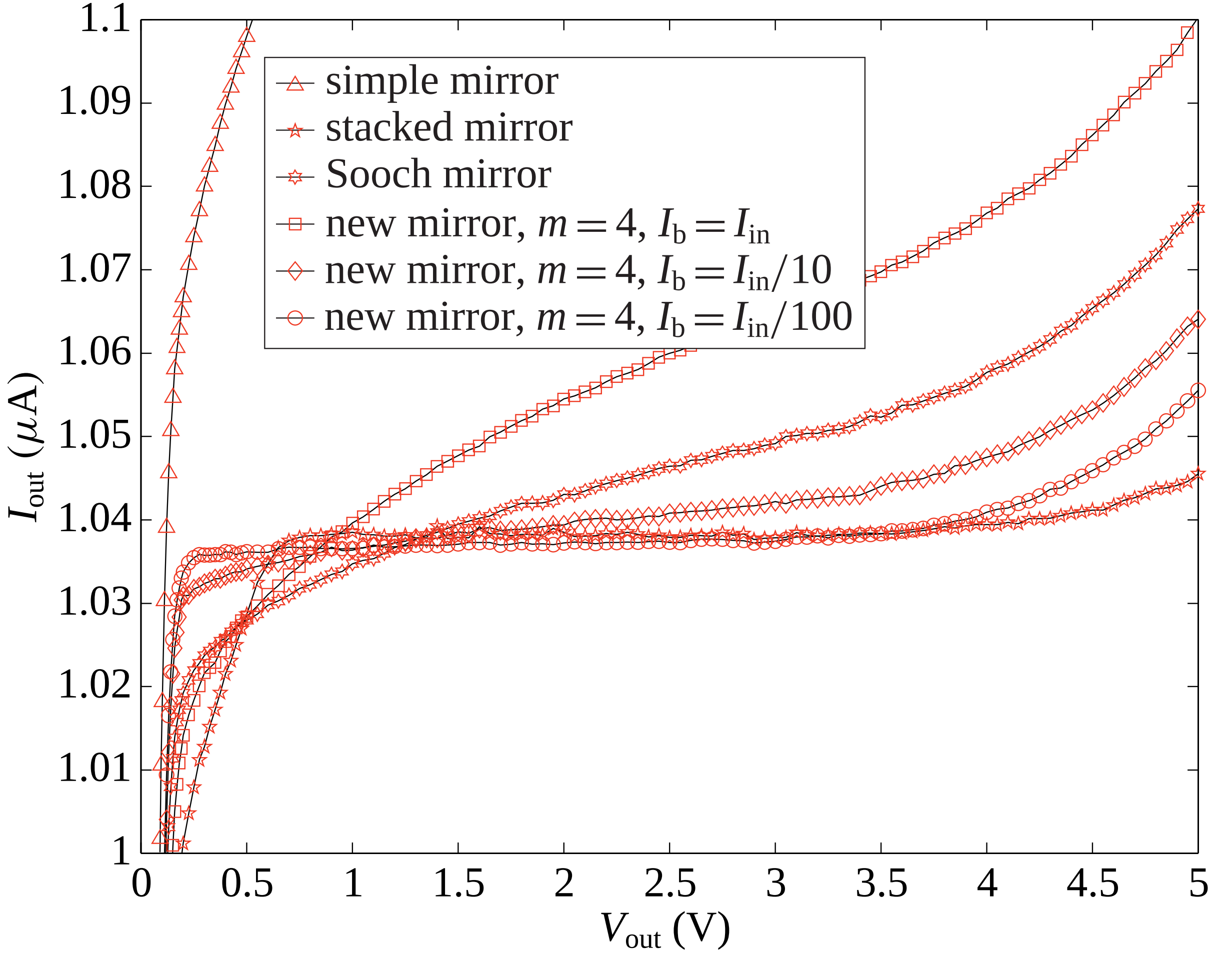
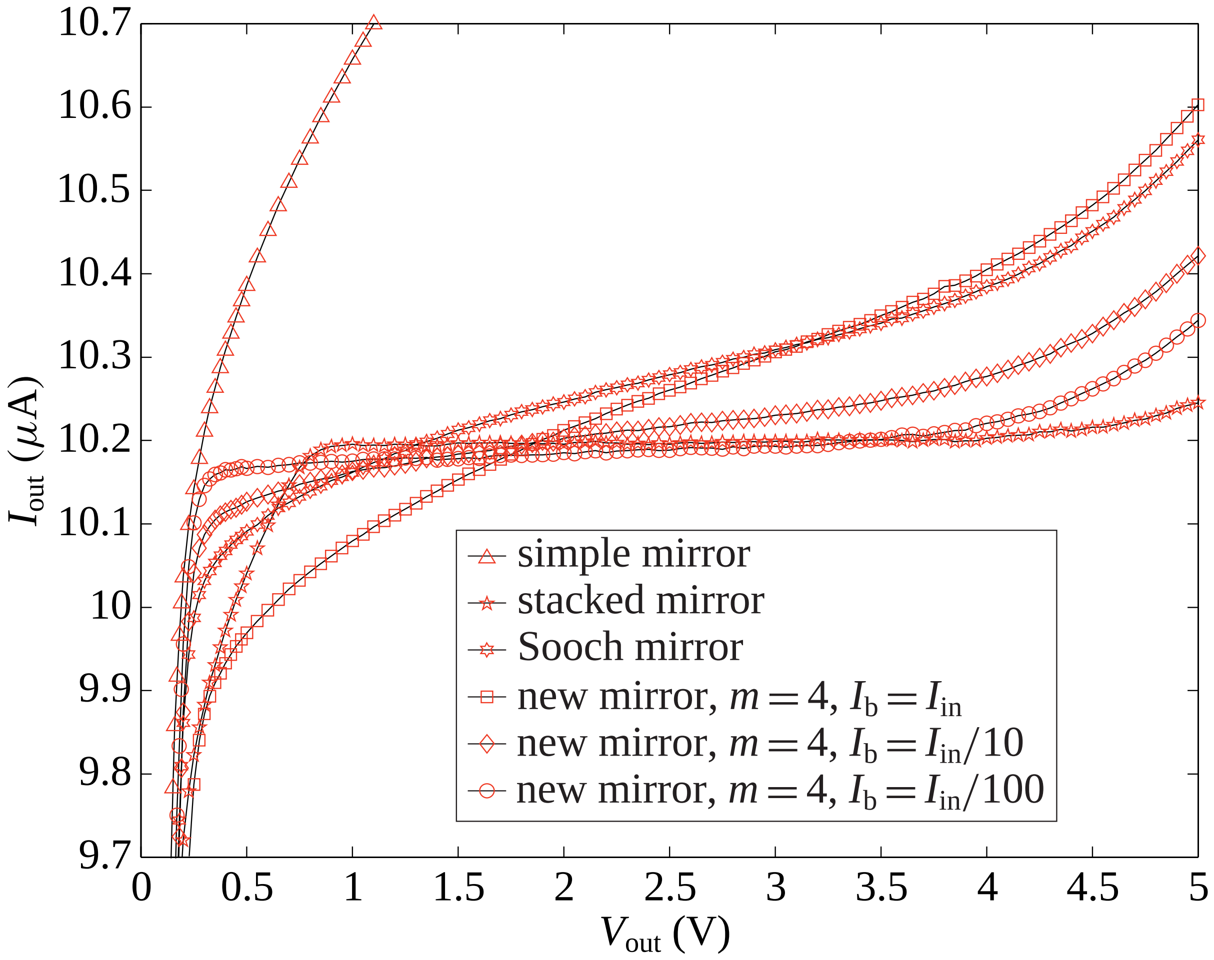
Experimental Results: Output Characteristics $I_{in} = 1.00\,\mu A$



Experimental Results: Output Characteristics $I_{\text{in}} = 10.0\,\mu\text{A}$



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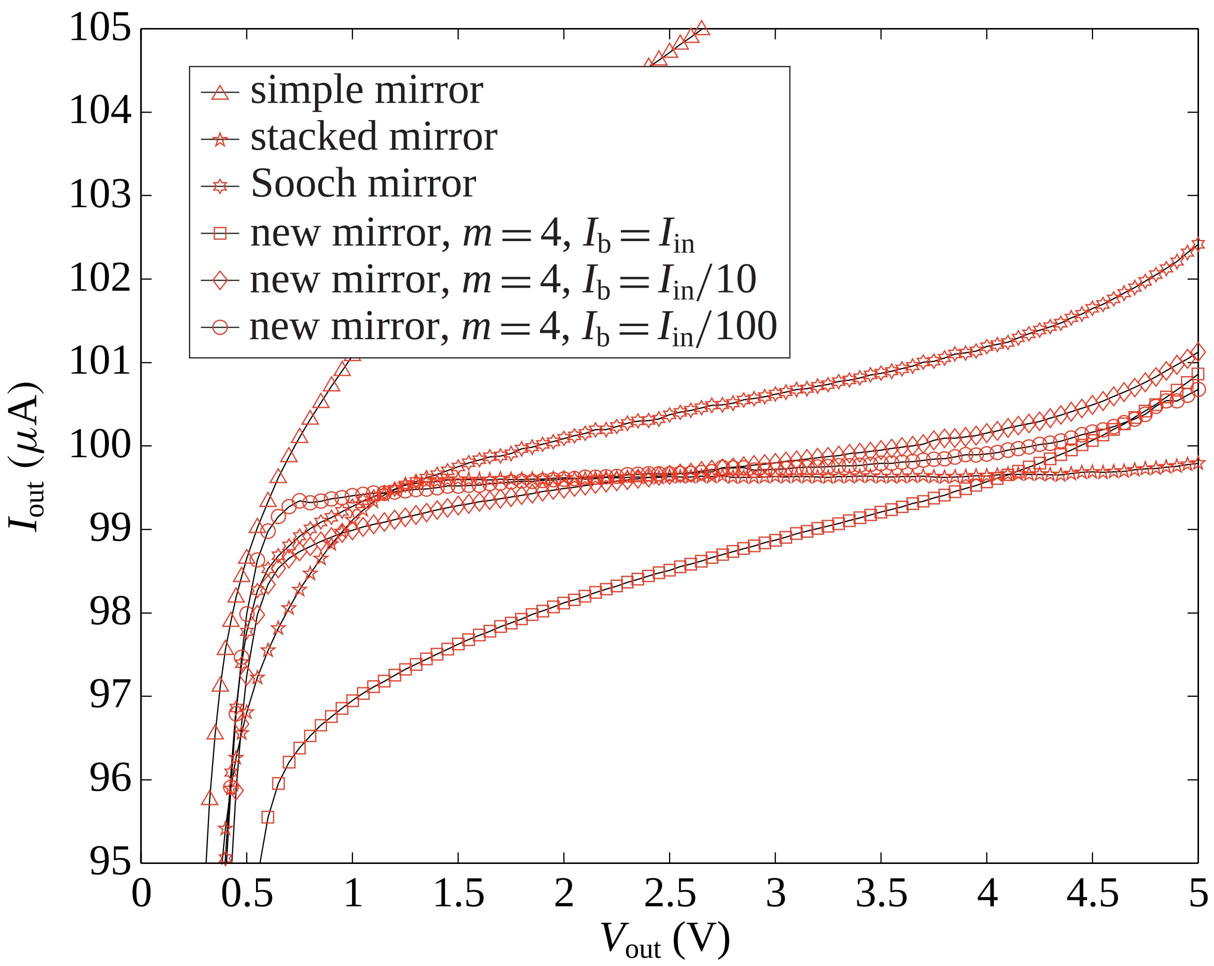

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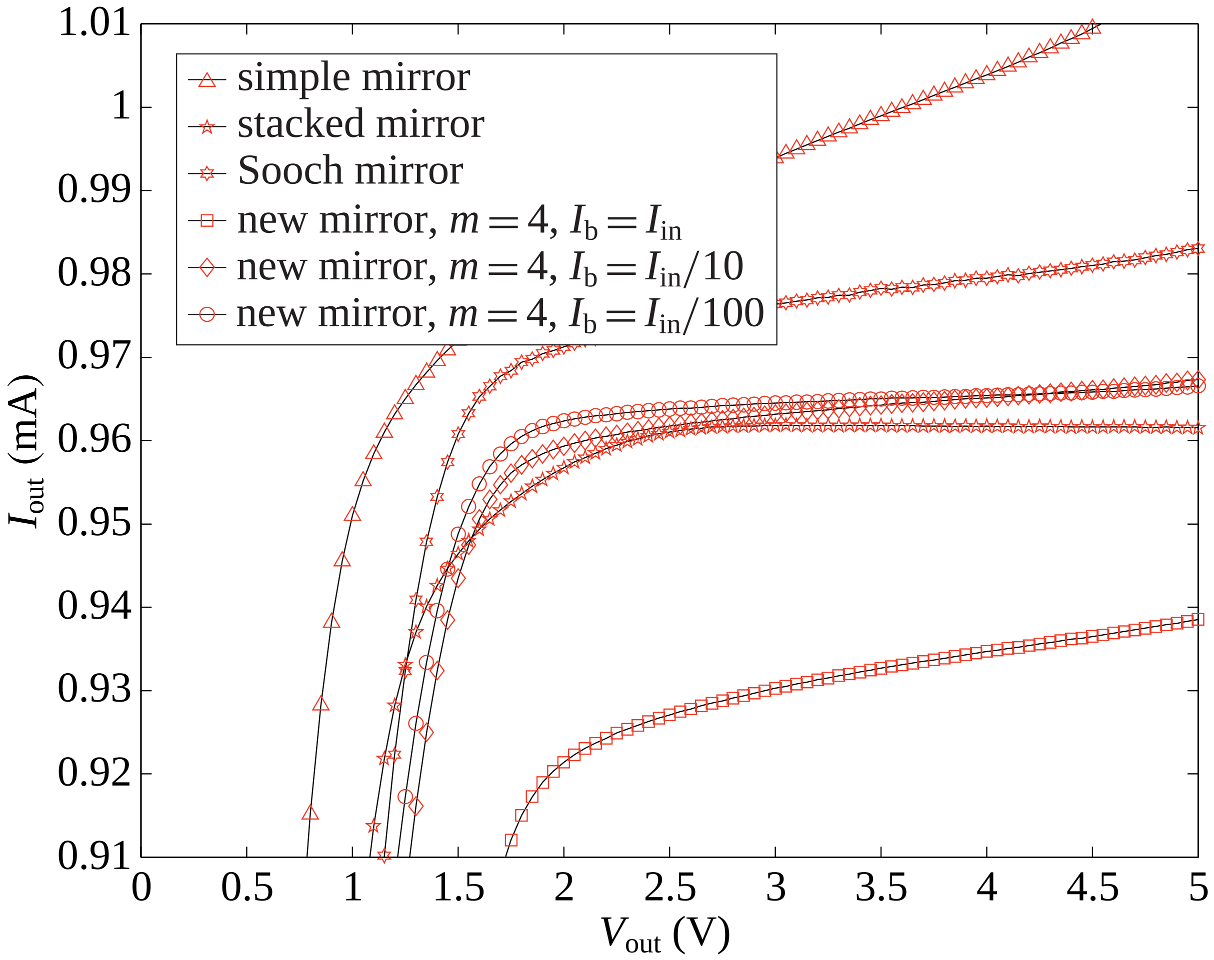

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