A Simple Way to Extend the Common-Mode Input-Voltage Range of the MOS Differential Pair

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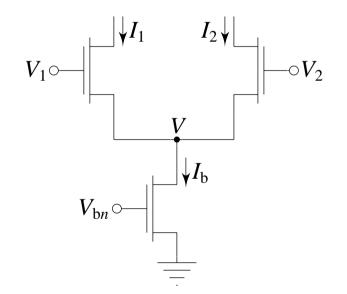
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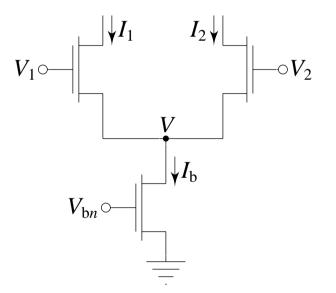
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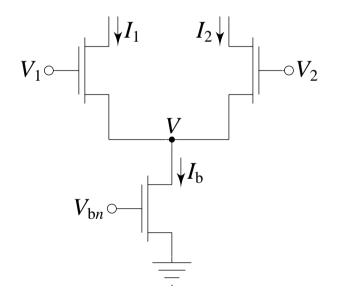
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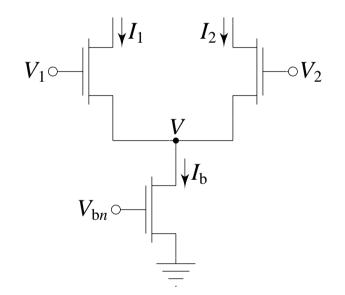
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- This venerable cirucit starts to have headroom problems as the power supply voltage shrinks.
- The *n*MOS diff pair has a lower limit on $V_{\rm cm}$ of about a diode drop plus a saturation voltage.

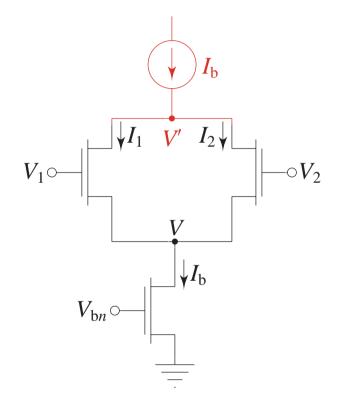






• Suppose that we sum I_1 and I_2 and compare the sum to I_b at the drains, as shown.

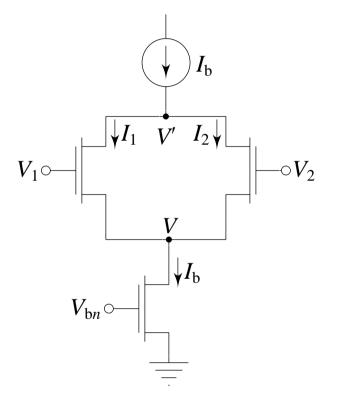
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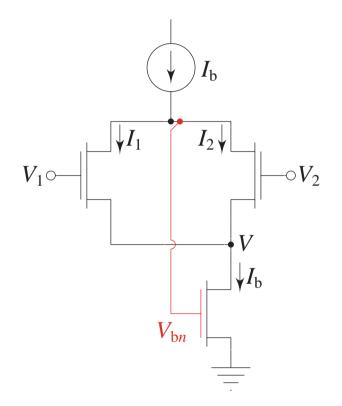
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- Next, suppose that we connect V' to V_{bn} , as shown, thereby creating a negative feedback loop that adjusts V_{bn} so that $I_1 + I_2 = I_b$, even if $V \le V_{DSsat}$.

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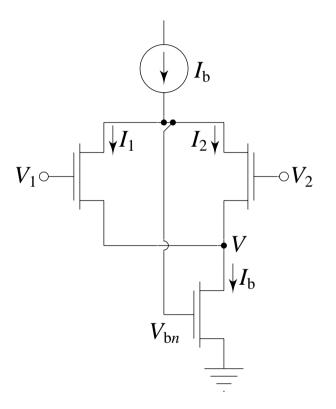




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- We call this circuit the *flipped differential pair* after Ramírez-Angulo *et al*.

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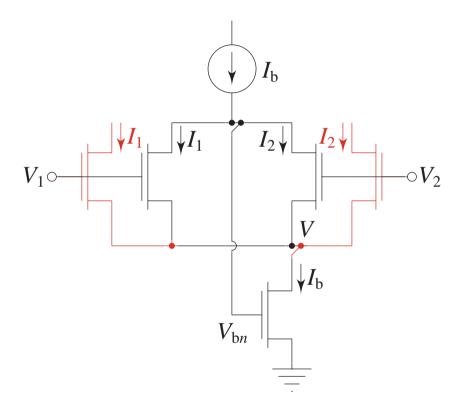




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• We can generate output currents by adding another pair of transistors to the circuit, as shown.

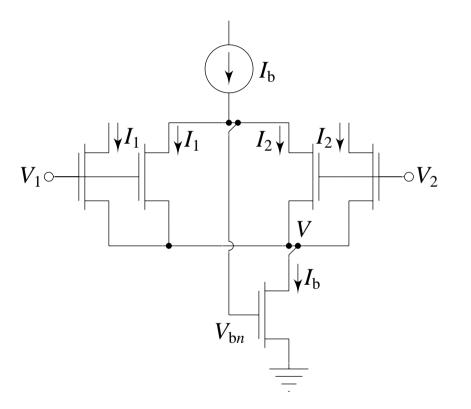
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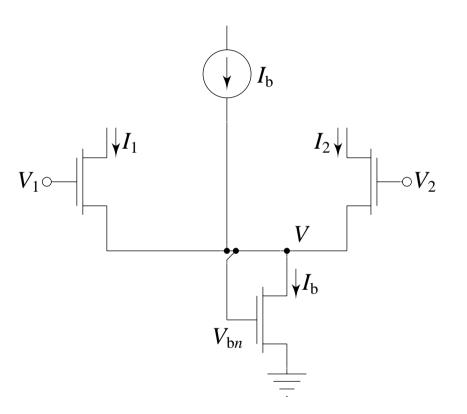
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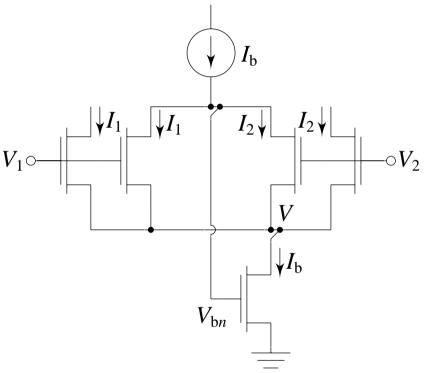






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- As V_{cm} increases, V hits V_{bn} , driving the central pair out of saturation. Beyond this point, the circuit behaves as that shown.
- Nonetheless, this diff pair is useful when $V_{\rm DD}$ is less than about two diode drops.

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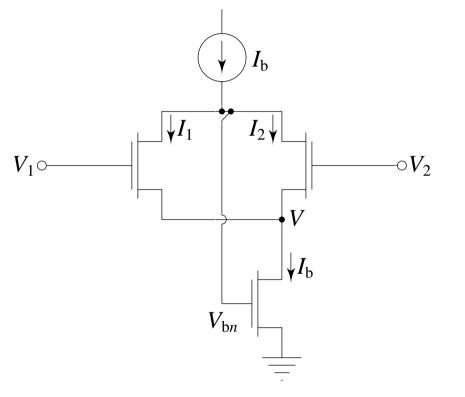




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• If this upper limit on $V_{\rm cm}$ is undesirable, we can use the flipped diff pair core to bias a normal diff pair adaptively, as shown.

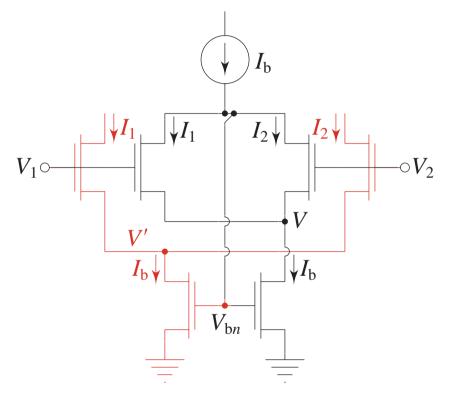
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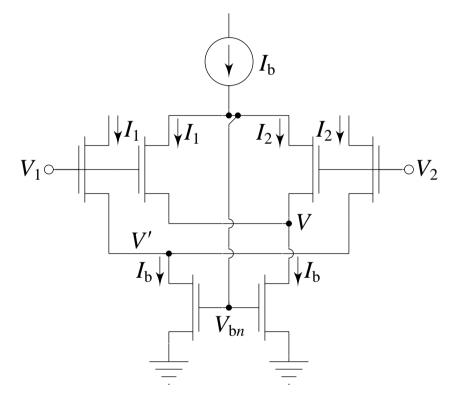
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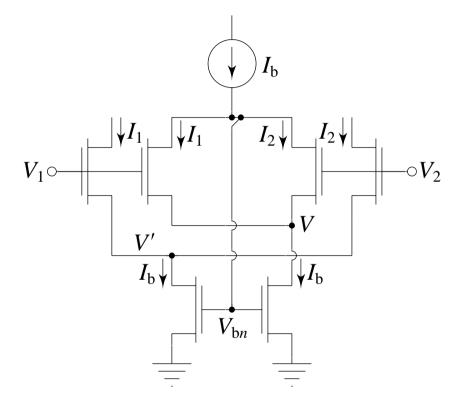
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- For high V_{cm} , the flipped diff pair behaves effectively as a diode connected transistor, and the normal diff pair behaves as ususal.
- For low V_{cm} , the central pair is saturated, V = V', and V_{bn} adjusts itself to keep $I_1 + I_2 = I_b$, even if $V = V' \le V_{DSsat}$.

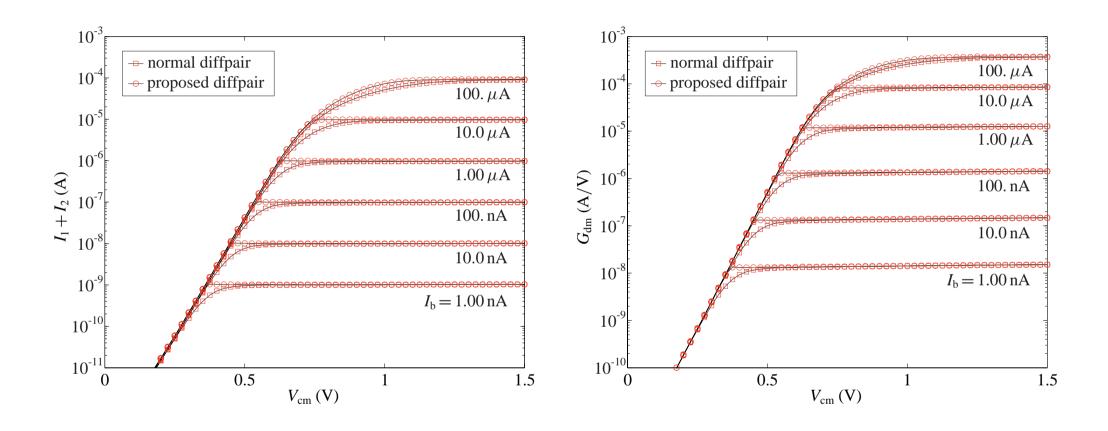
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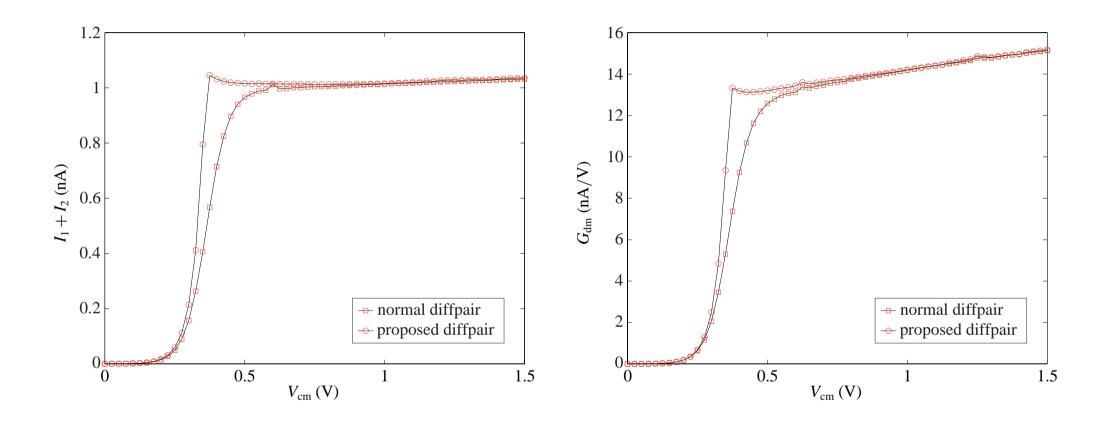
Experimental Common-Mode Characteristics







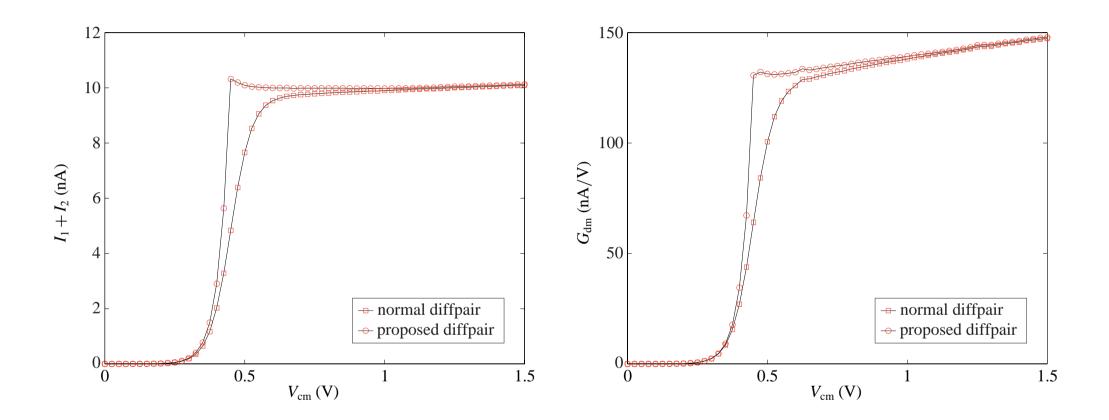
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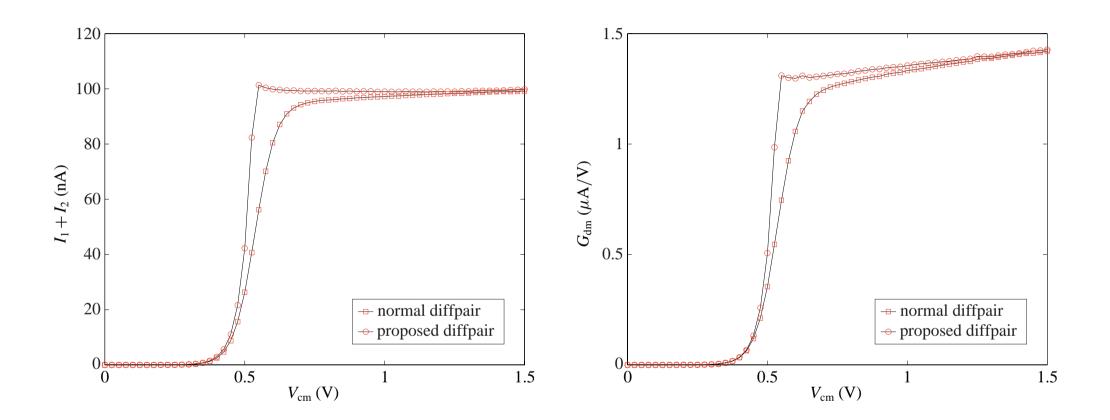
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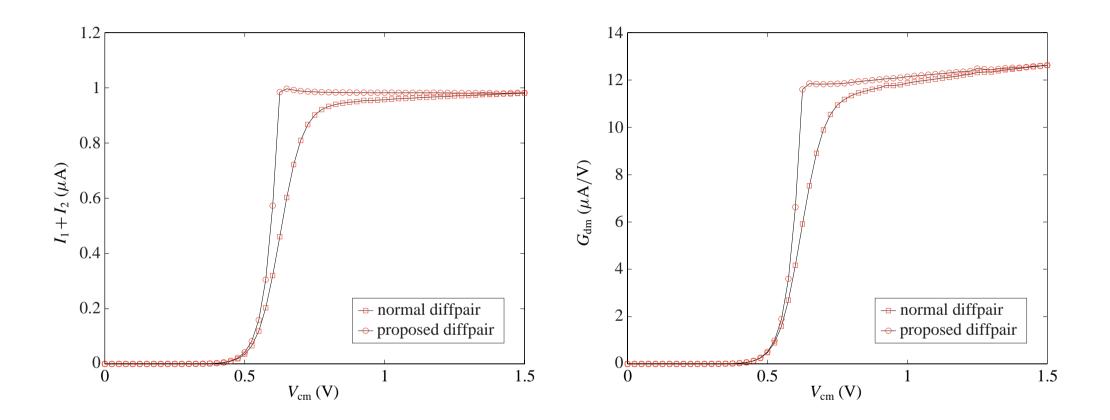
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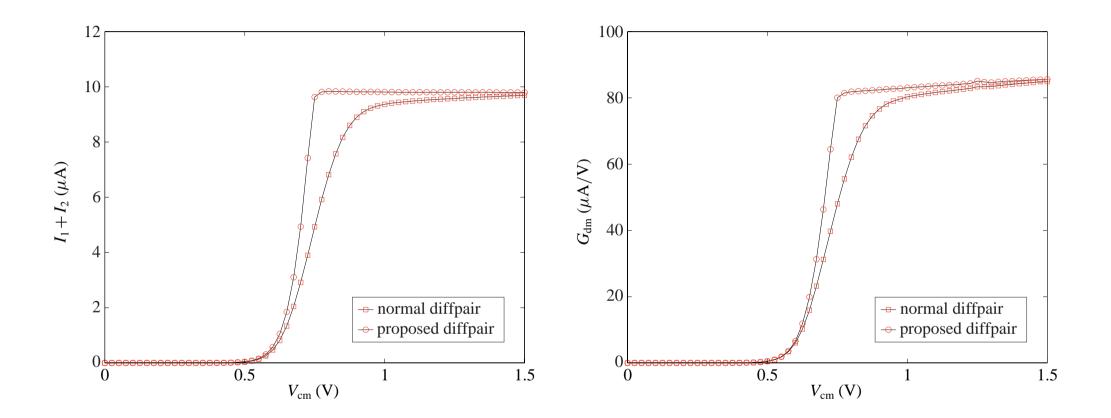
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