A Low-Voltage MOS Cascode Bias Circuit for All Current Levels

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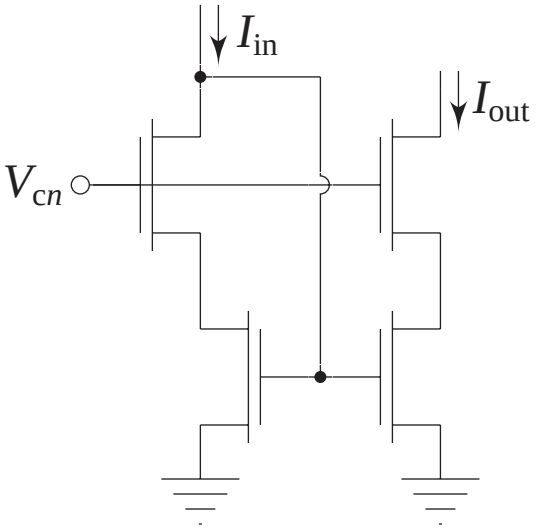
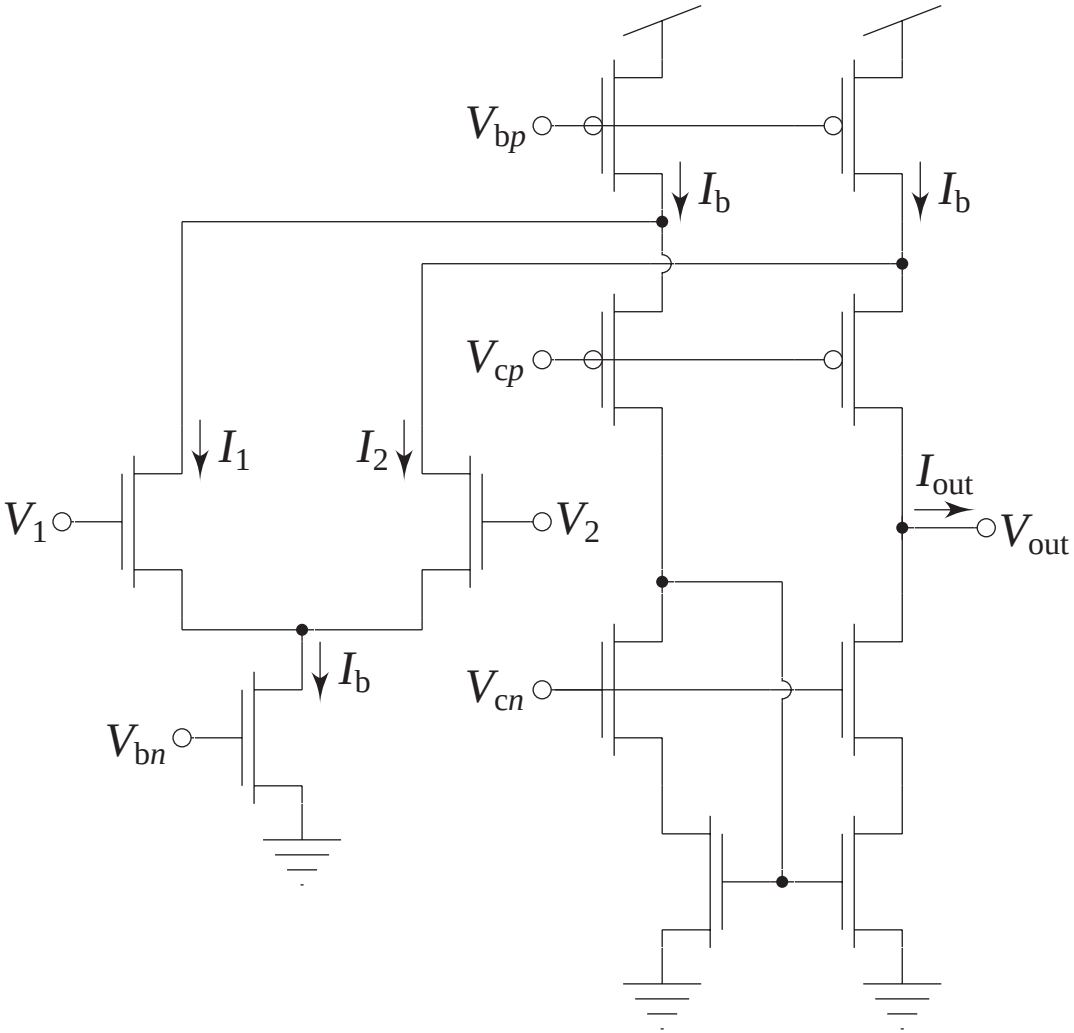
Low-Voltage Cascodes





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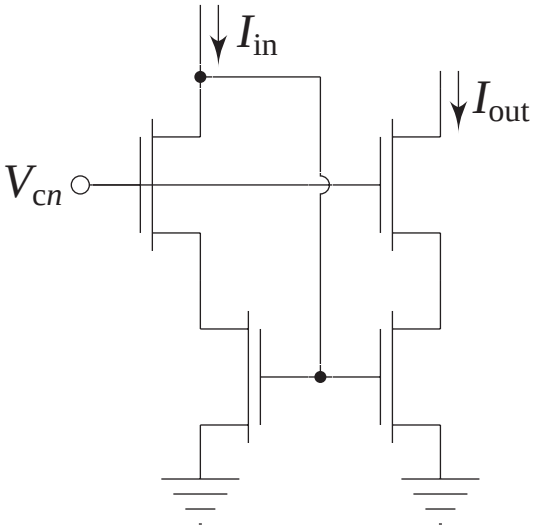

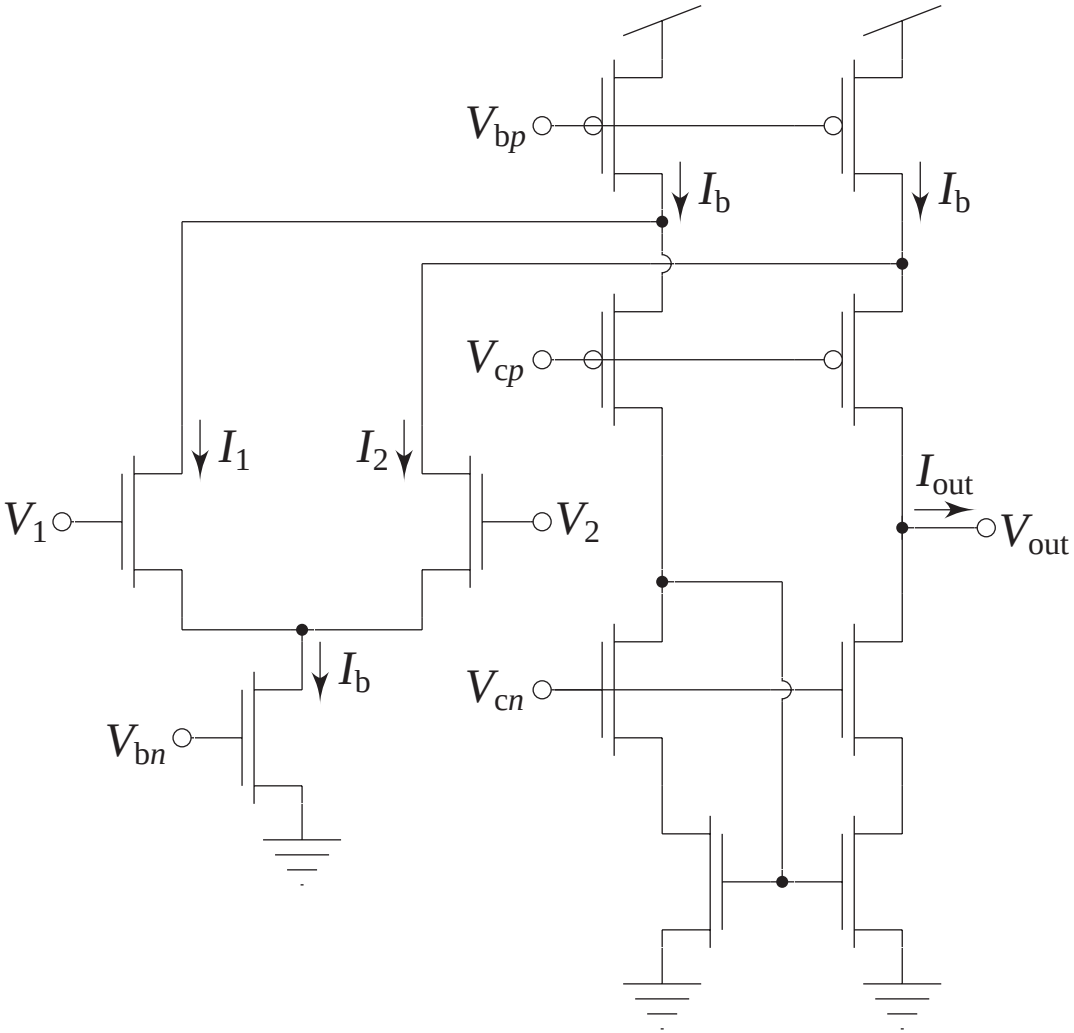

- Cascodes are alive and well, but we must bias them properly for low-voltage operation.
- How can we generate V_{cn} and V_{cp} without consuming too much headroom?

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Simple EKV MOS Transistor Model

- We model the channel current of an *n*MOS transistor as the difference between a *forward* current and a *reverse* current,

$$I = I_{\mathrm{F}} - I_{\mathrm{R}},$$

whose values are given by

$$I_{\mathrm{F(R)}} = \frac{W}{L} I_{\mathrm{s}} \log^2 \left(1 + e^{\left(\kappa (V_{\mathrm{G}} - V_{\mathrm{T0}}) - V_{\mathrm{S(D)}}\right)/2U_{\mathrm{T}}}\right),$$

where

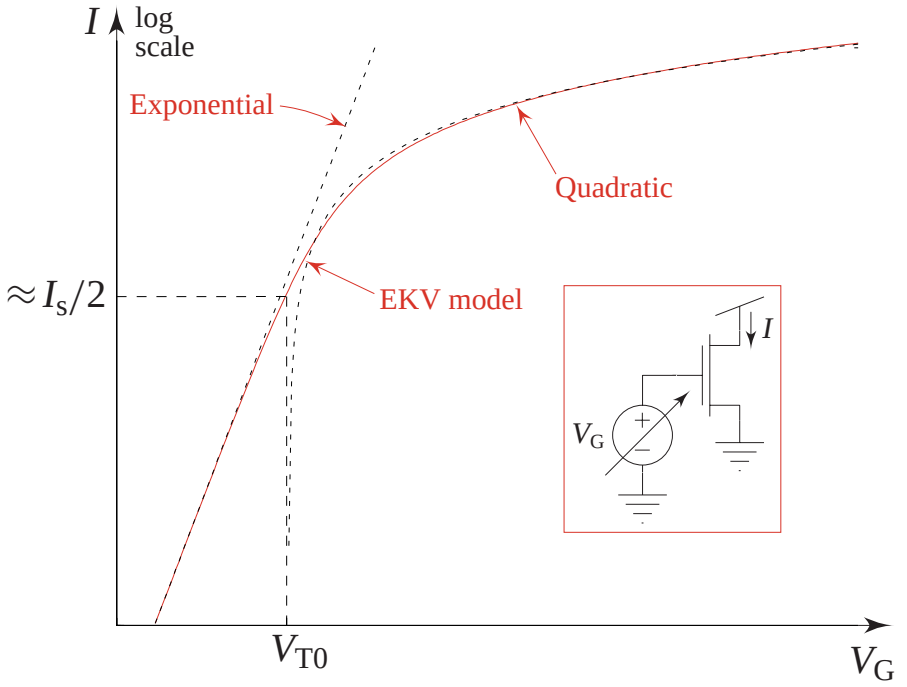
$$U_{\mathrm{T}} \equiv \frac{kT}{q}, \quad I_{\mathrm{s}} \equiv \frac{2\mu C_{\mathrm{ox}} U_{\mathrm{T}}^2}{\kappa}, \quad \text{and} \quad \kappa \equiv \frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}} + C_{\mathrm{dep}}}.$$

- Note that $\kappa \equiv 1/n$ and that I_{s} is approximately twice the threshold current of a square transistor.

Simple EKV MOS Transistor Model

- The model covers all regions of MOS transistor operation and is continuous and smooth.
- The expression reduces asymptotically to an exponential in weak inversion and a quadratic in strong inversion, given by

$$I_{F(R)} \approx \begin{cases} \dfrac{W}{L} I_s e^{(\kappa(V_G - V_{T0}) - V_{S(D)})/U_T}, \\ \qquad V_G < V_{T0} + \dfrac{V_{S(D)}}{\kappa} \\ \dfrac{W}{L} \cdot \dfrac{\mu C_{ox}}{2\kappa} \left(\kappa\,(V_G - V_{T0}) - V_{S(D)}\right)^2, \\ \qquad V_G > V_{T0} + \dfrac{V_{S(D)}}{\kappa} \end{cases}$$



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- If $I_F \approx I_R$, then I depends on both V_S and V_D in a symmetric manner, which corresponds qualitatively to the *ohmic* region of operation.

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- We define the onset of saturation operationally in terms of an arbitrary parameter, $A \gg 1$: We say that an MOS transistor is saturated if and only if $I_F / I_R \geq A$.

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- We define the onset of saturation operationally in terms of an arbitrary parameter, $A \gg 1$: We say that an MOS transistor is saturated if and only if $I_F/I_R \geq A$.
- To find an explicit expression for V_{DSsat}, we write that

$$A = \frac{I_F}{I_R} = \frac{\log^2\left(1 + e^{(\kappa(V_G - V_{T0}) - V_S)/2U_T}\right)}{\log^2\left(1 + e^{(\kappa(V_G - V_{T0}) - V_S - V_{DSsat})/2U_T}\right)}.$$

Simple EKV MOS Transistor Model

- Solving for V_{DSsat}, we find that

$$
\begin{aligned}
V_{\mathrm{DSsat}} &= \kappa\,(V_{\mathrm{G}} - V_{\mathrm{T0}}) - V_{\mathrm{S}} - 2U_{\mathrm{T}} \log\left(\left(1 + e^{(\kappa(V_{\mathrm{G}} - V_{\mathrm{T0}}) - V_{\mathrm{S}})/2U_{\mathrm{T}}}\right)^{1/\sqrt{A}} - 1\right) \\
&= 2U_{\mathrm{T}} \log\left(\frac{e^{\sqrt{I_{\mathrm{F}}/(W/L)I_{\mathrm{s}}}} - 1}{e^{\sqrt{I_{\mathrm{F}}/A(W/L)I_{\mathrm{s}}}} - 1}\right) \\
&\approx \begin{cases} U_{\mathrm{T}} \log A, & V_{\mathrm{G}} < V_{\mathrm{T0}} + \dfrac{V_{\mathrm{S}}}{\kappa} \\ \left(1 - \dfrac{1}{\sqrt{A}}\right)(\kappa\,(V_{\mathrm{G}} - V_{\mathrm{T0}}) - V_{\mathrm{S}}), & V_{\mathrm{G}} > V_{\mathrm{T0}} + \dfrac{V_{\mathrm{S}}}{\kappa}. \end{cases}
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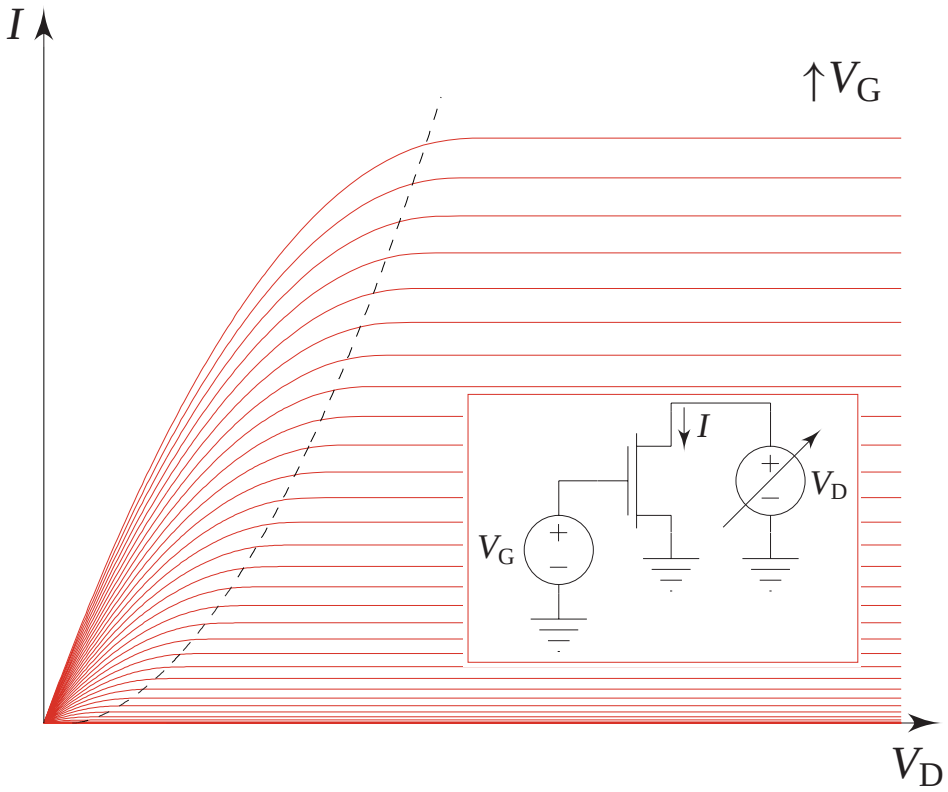

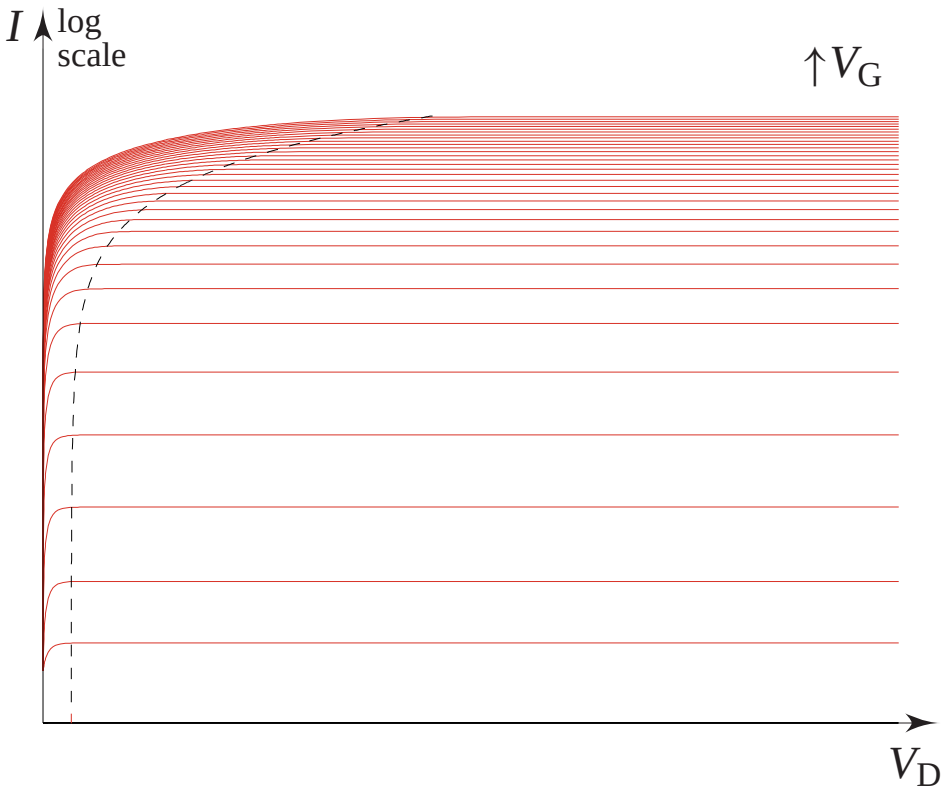

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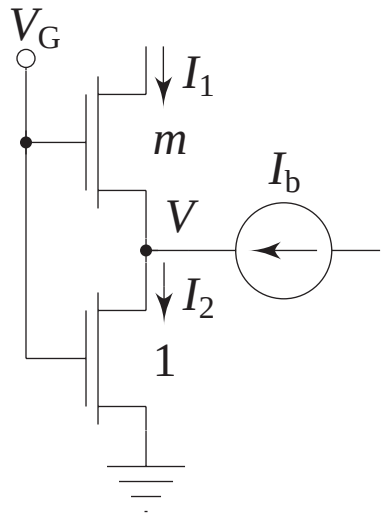
Low-Voltage Cascode Bias Circuit

- Assume M_1 saturated, M_2 either ohmic or saturated:

$$I_1 \approx I_{F1} \quad \text{and} \quad I_2 = I_{F2} - I_{R2}.$$



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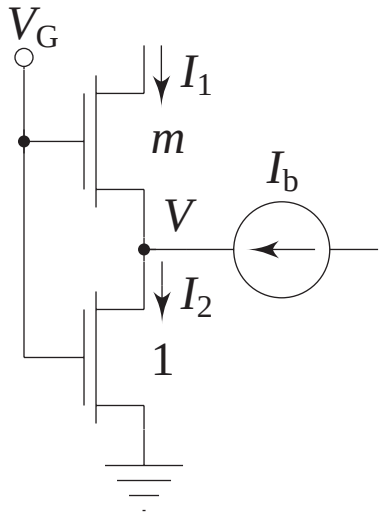
- V is source of M_1 and drain of M_2, so we have

$$I_{F1} = m I_{R2} \quad \Longrightarrow \quad I_{R2} = \frac{I_{F1}}{m} \approx \frac{I_1}{m}.$$



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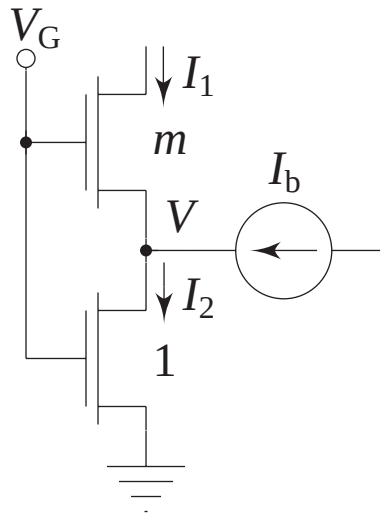

- Solving for I_{F2}/I_{R2}, we get

$$\frac{I_{F2}}{I_{R2}} = 1 + \frac{I_2}{I_{R2}} = 1 + m\frac{I_2}{I_1} = 1 + m\left(1 + \frac{I_b}{I_1}\right).$$

Low-Voltage Cascode Bias Circuit

- Setting I_1 equal to I_b/n, we get

$$\frac{I_{F2}}{I_{R2}} = 1 + m\left(1 + n\frac{I_b}{I_b}\right) = 1 + m\,(1+n)\,,$$

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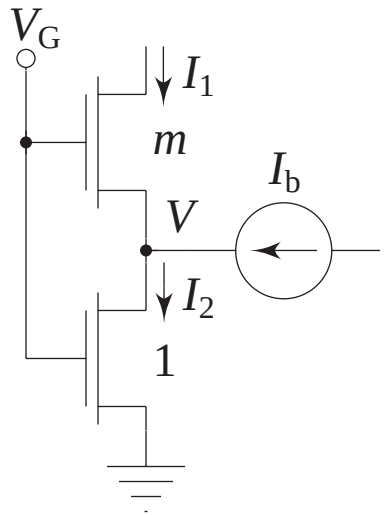

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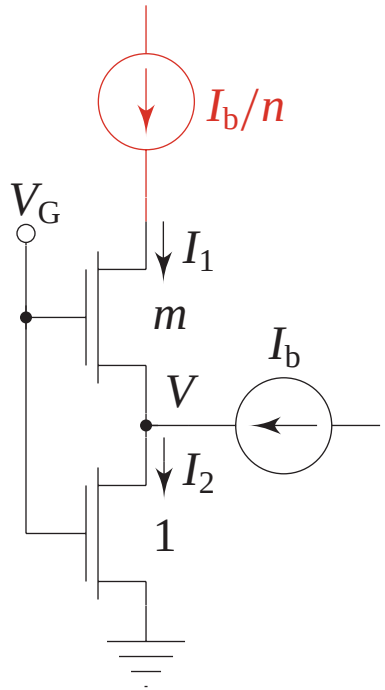

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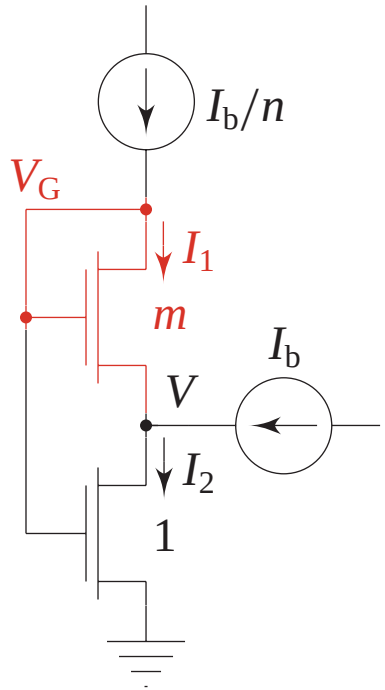

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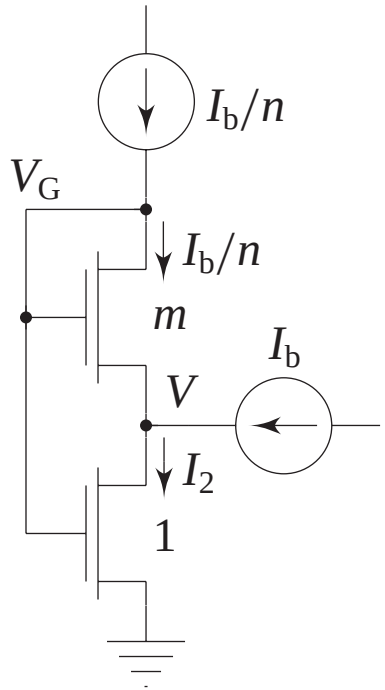

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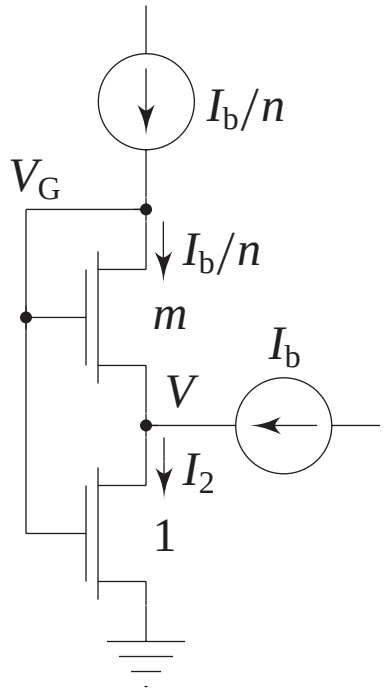

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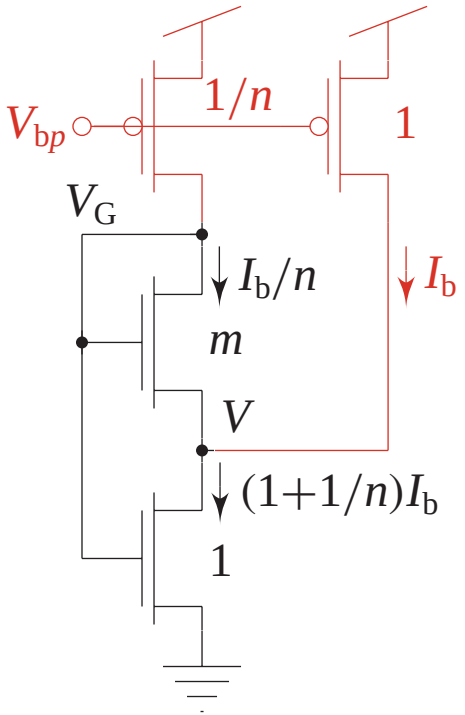

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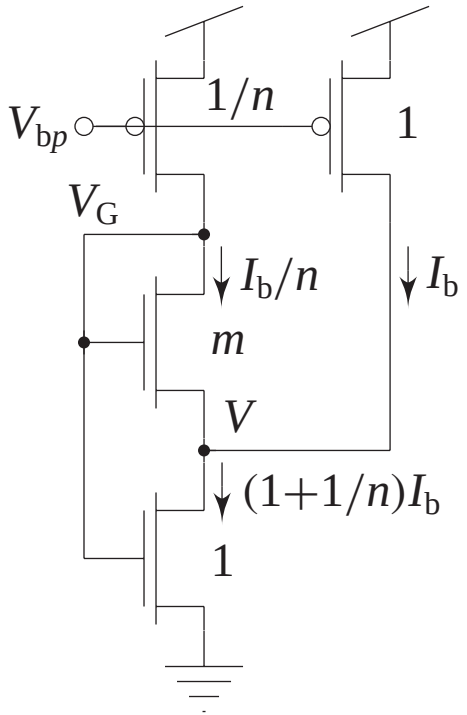

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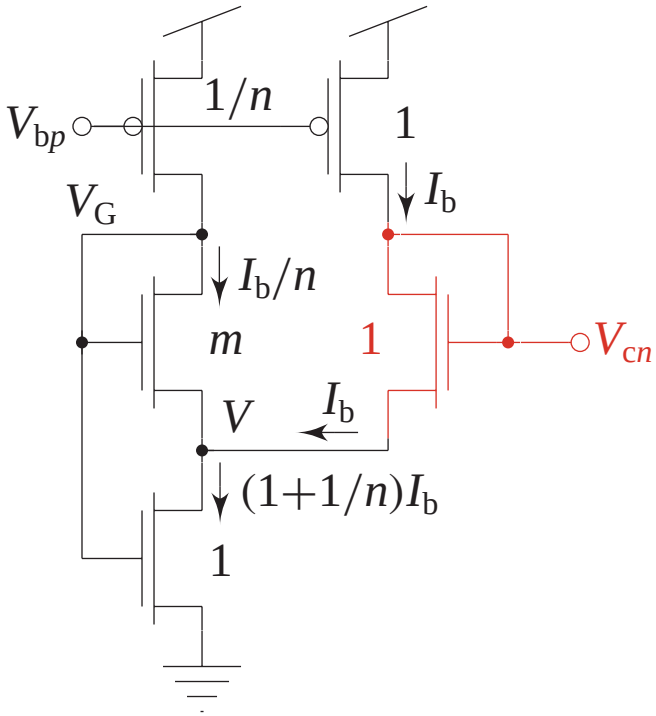

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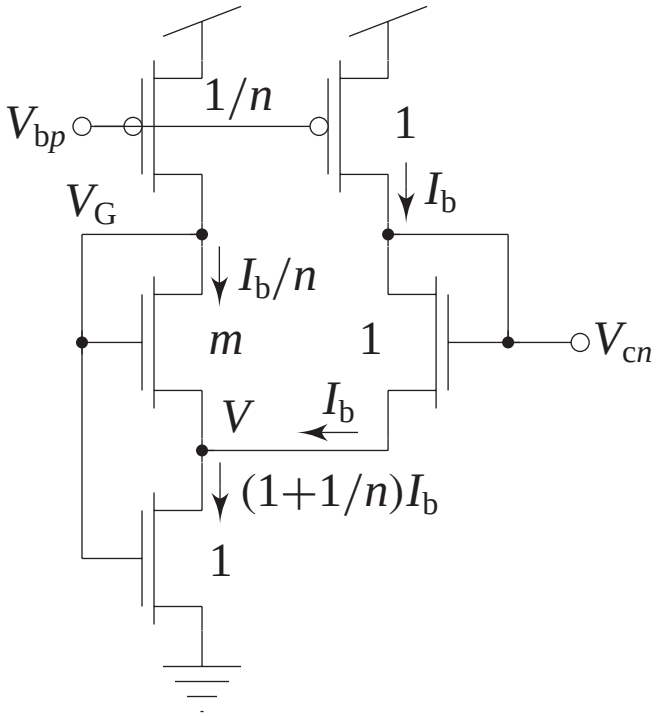

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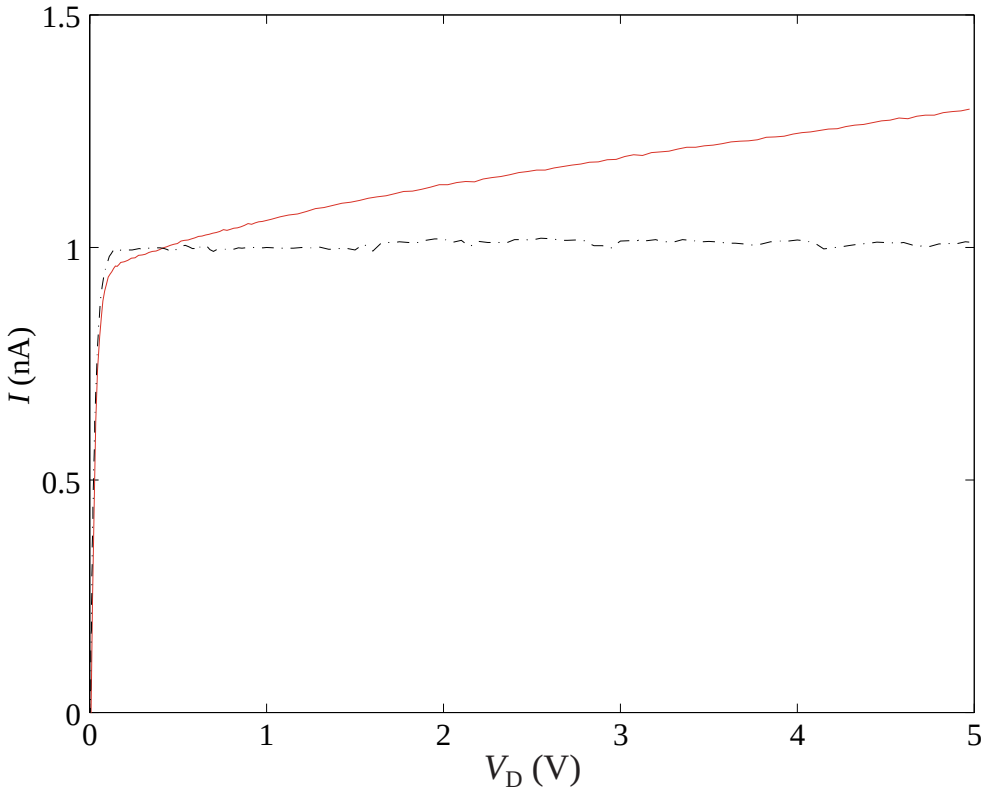

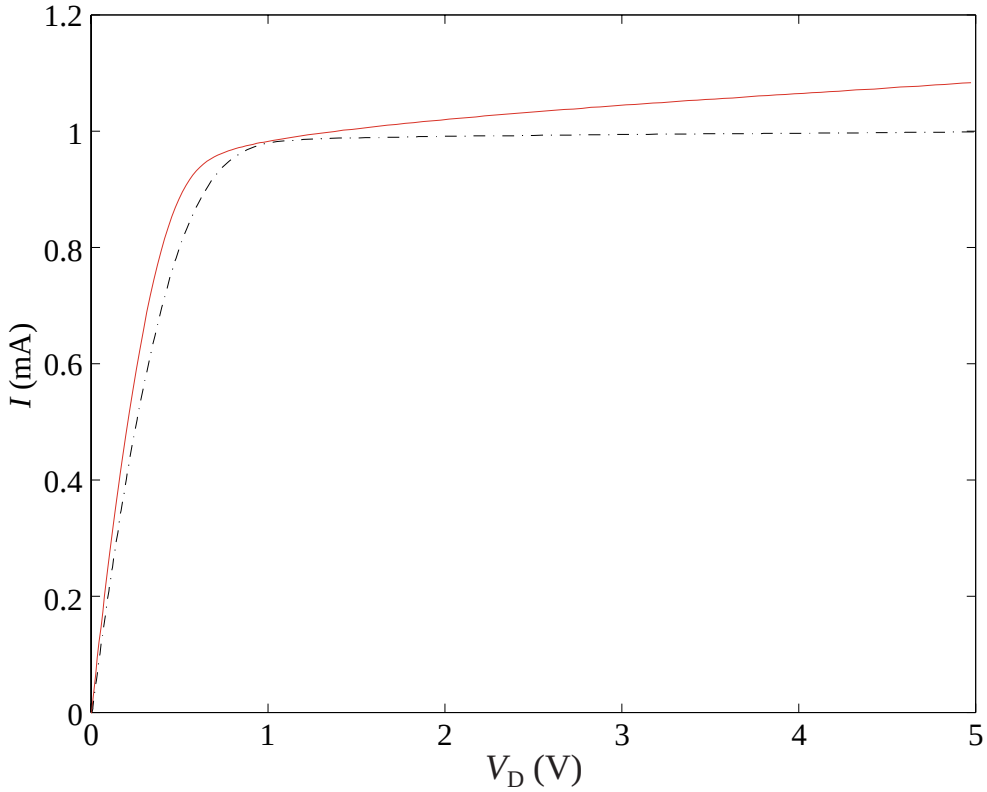

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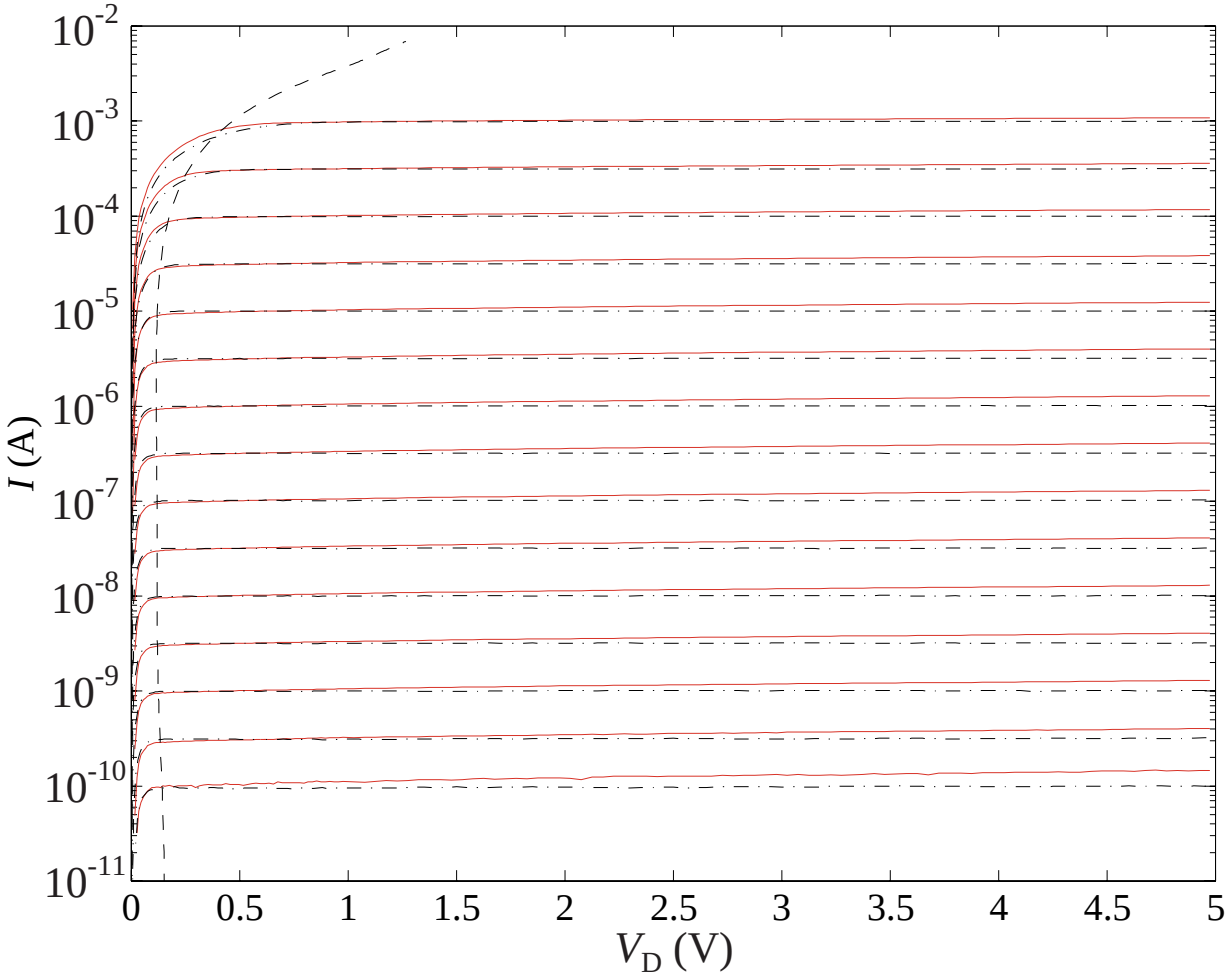

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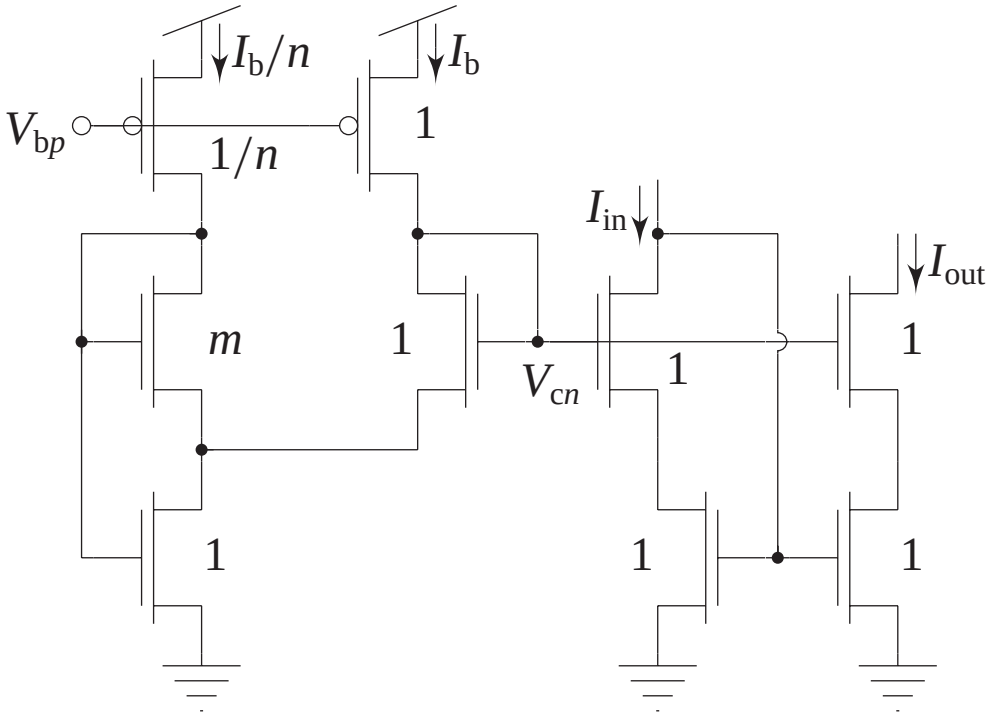
Layout Considerations for a Low-Voltage Cascode Current Mirror

- To get accurate ratios, we implement the *n*MOS of width *m* as a parallel connection of *m* unit transistors.



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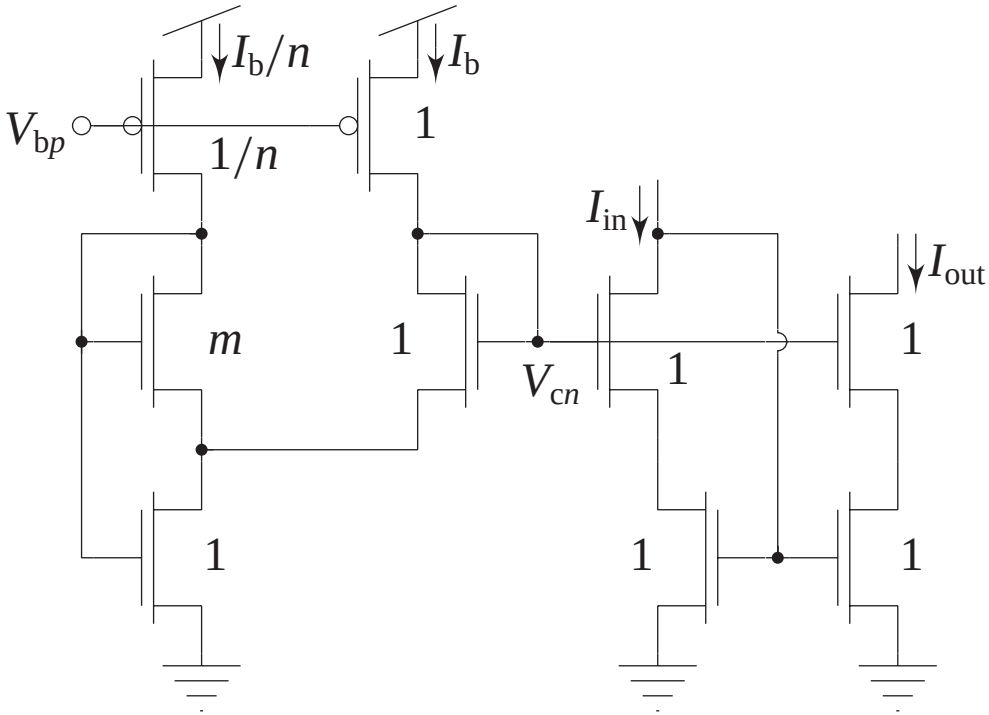

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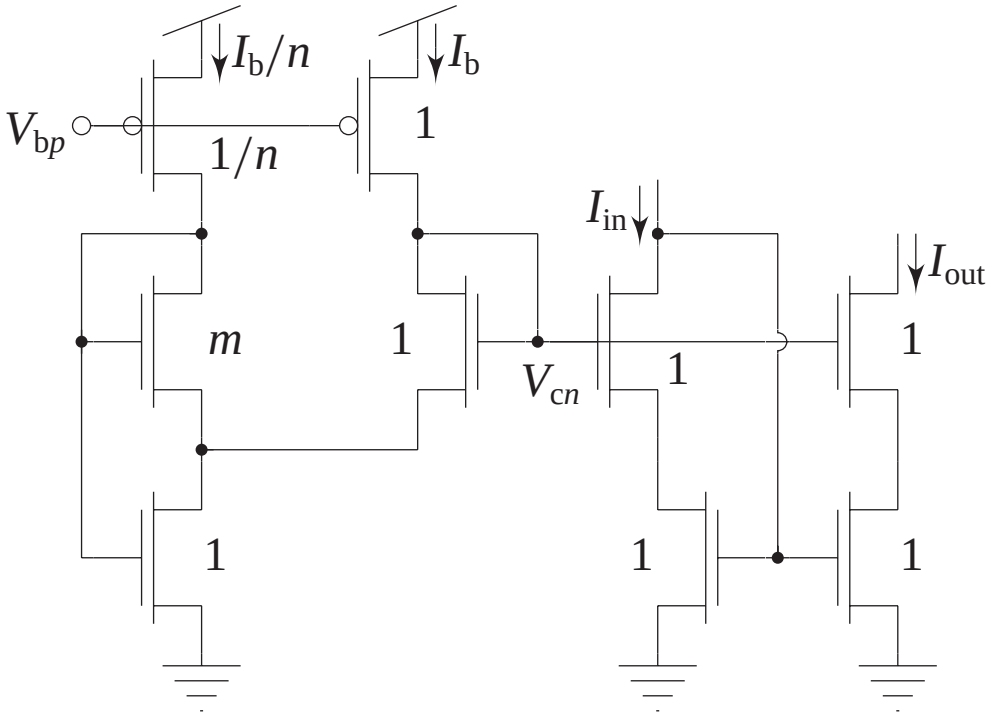

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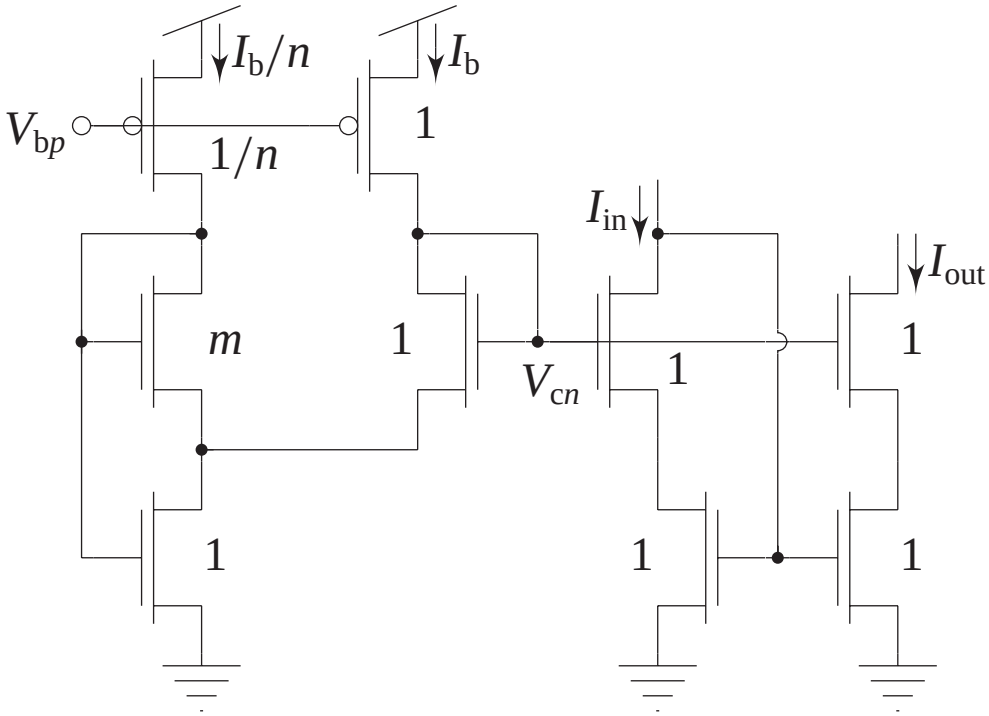
- If we choose *m* to be even, we can optimally share source/drain regions of the *n*MOS transistors in the bias circuit.
- If we choose $n = m + 1$, we have as many *p*MOS strips as *n*MOS strips.



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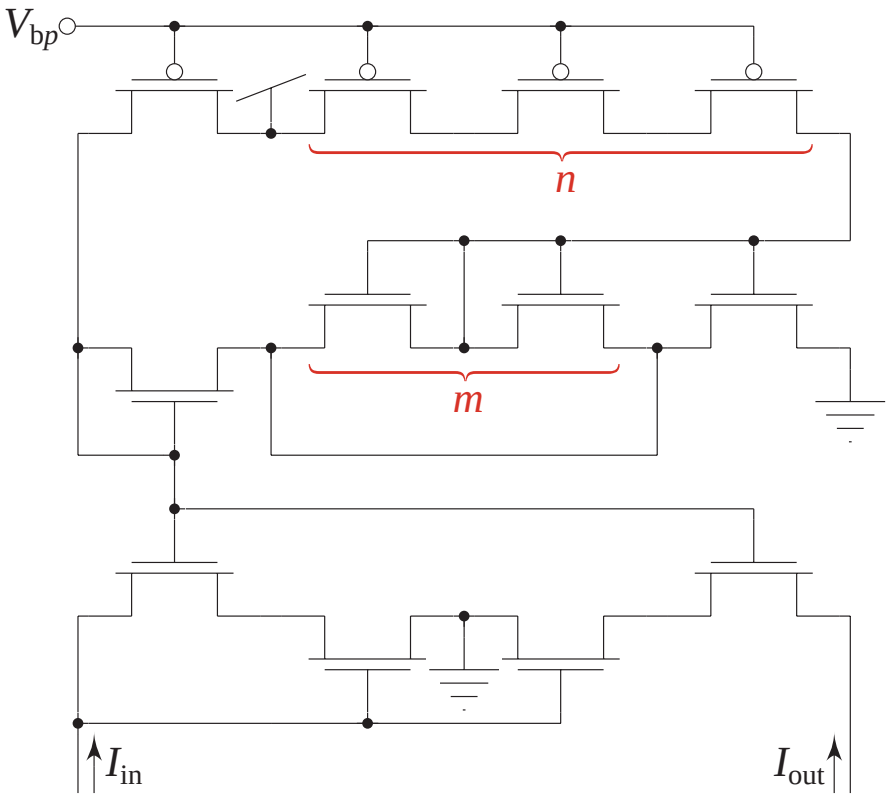

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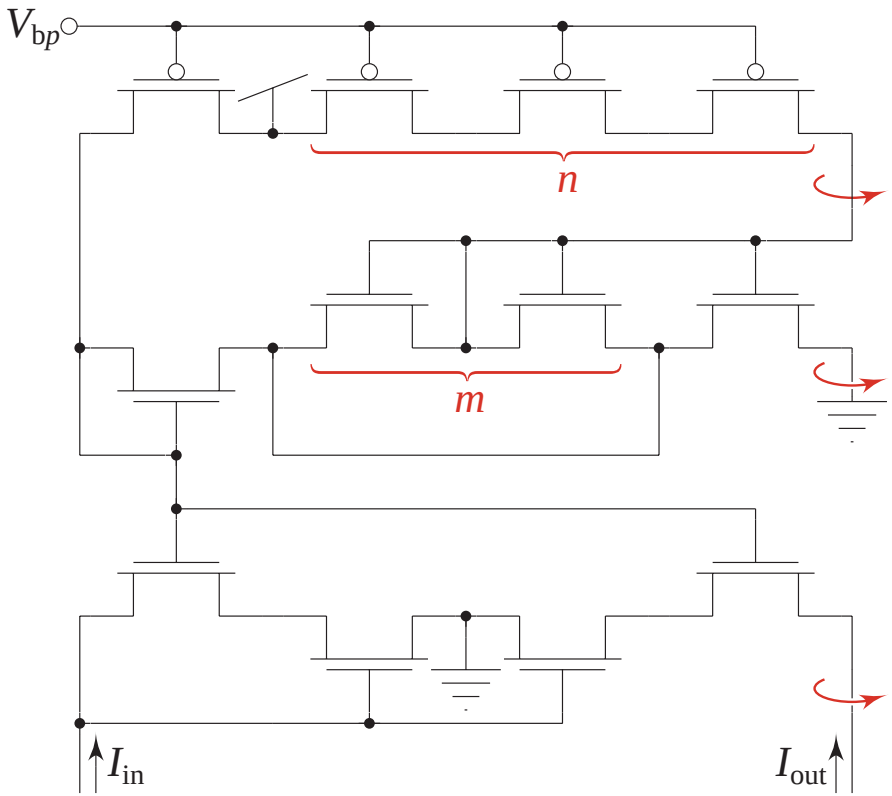

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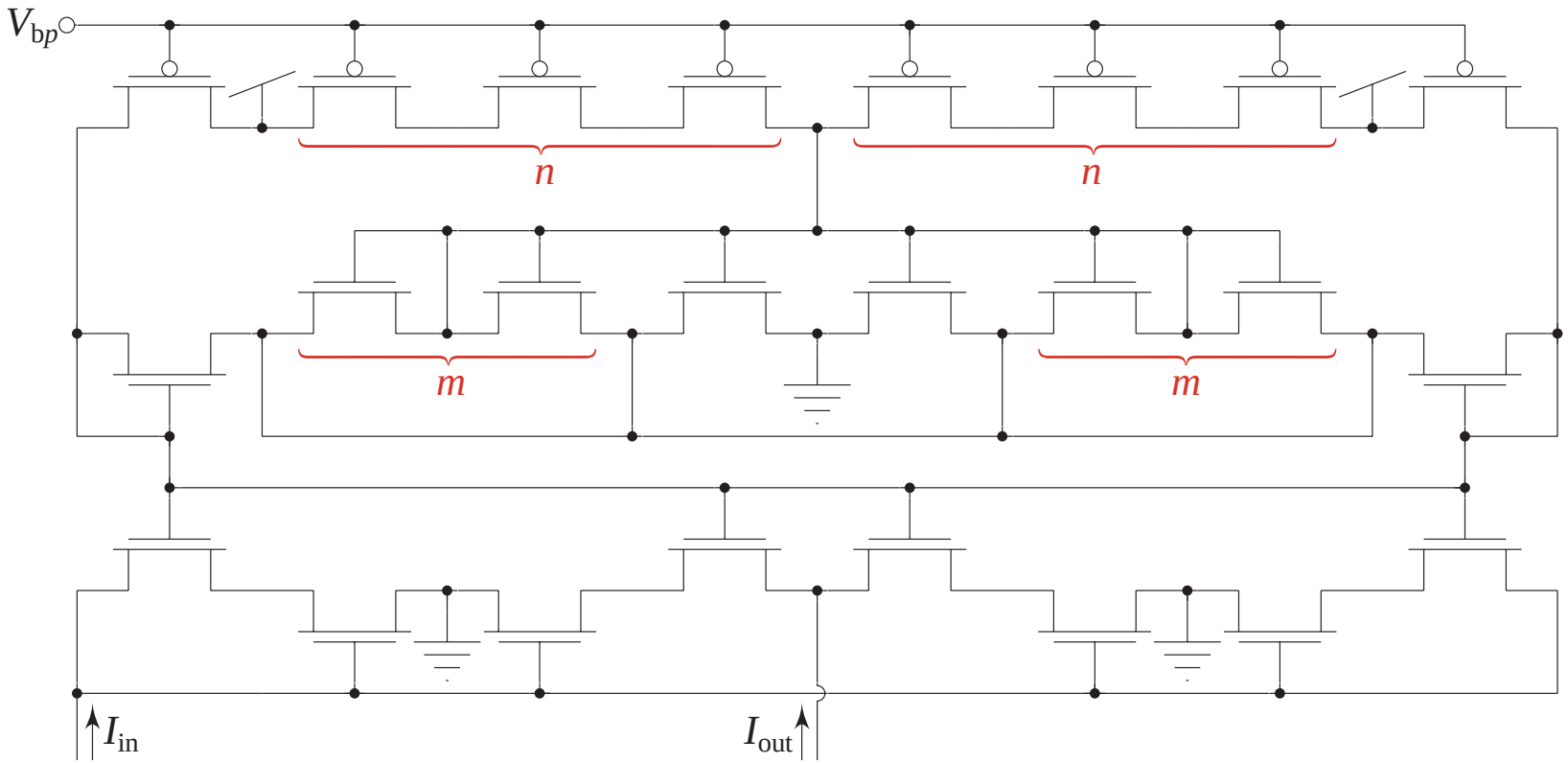

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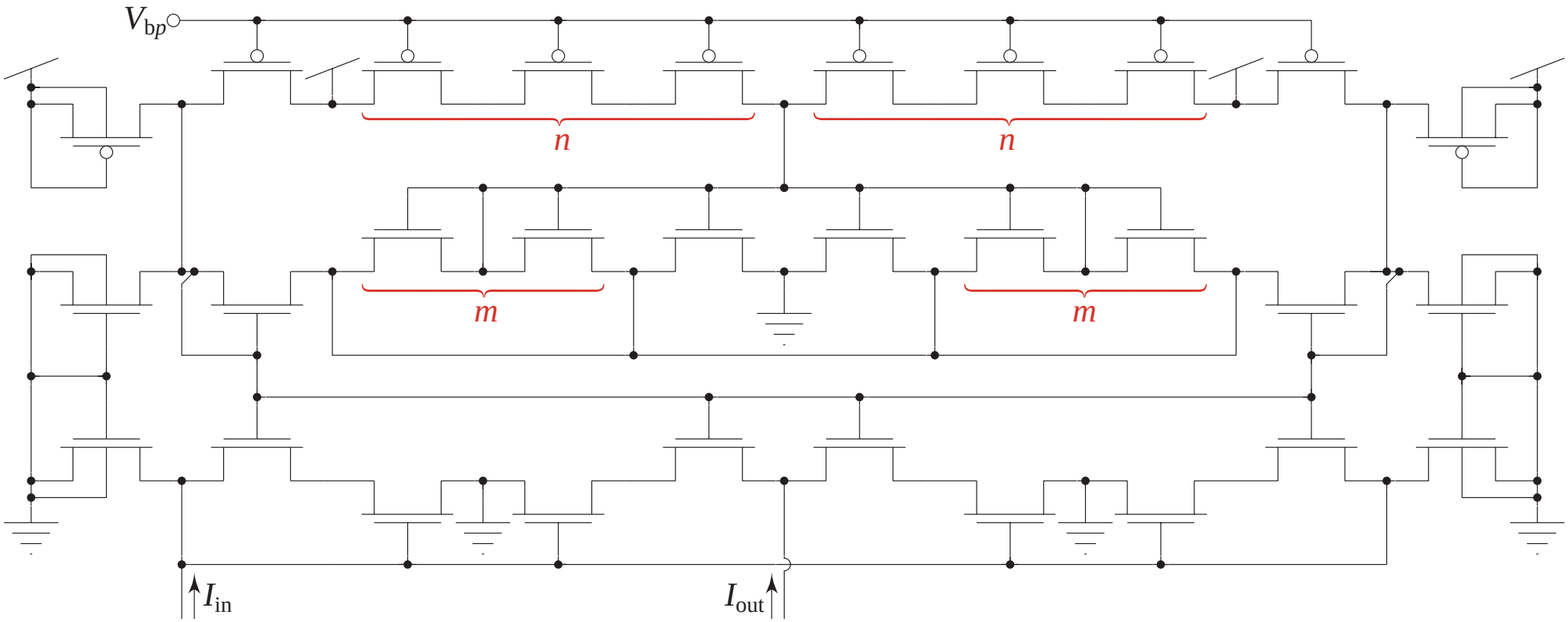

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