

Low-Voltage Circuits in Floating-Gate and Double-Gate CMOS

Bradley A. Minch

Mixed Analog-Digital VLSI Circuits and Systems Lab

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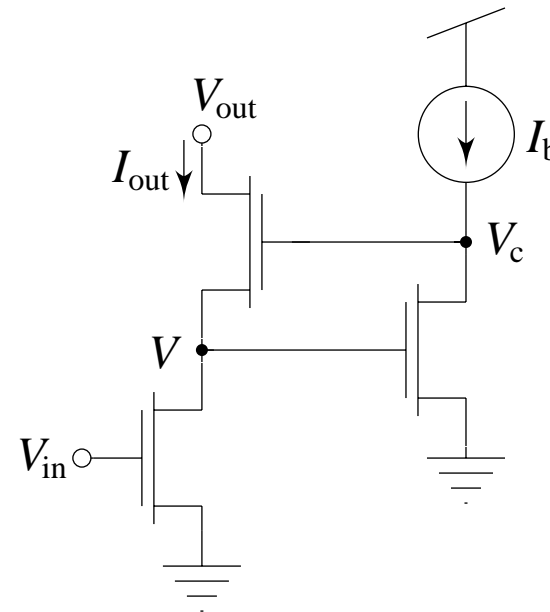


Mixed Analog-Digital VLSI Circuits and Systems Lab

- **Research focus:** Low-voltage/low-power analog and mixed-signal circuit design
- **Current M.S./Ph.D. students:**
Abhishek Kammula, Eric McDonald, Kofi Odame, Sheng-Yu Peng
- **Former M.S./Ph.D. students:**
Karan Mathur, Mark Neidengard, Yuan Yang
- **Current projects:**
 - High-level synthesis of translinear and log-domain circuits and systems
 - Floating-gate MOS (FGMOS) circuit design
 - Double-gate MOS (DGMOS) modelling and circuit design
 - Chemical sensing with chemoreceptive neuron MOS (CvMOS) transistors

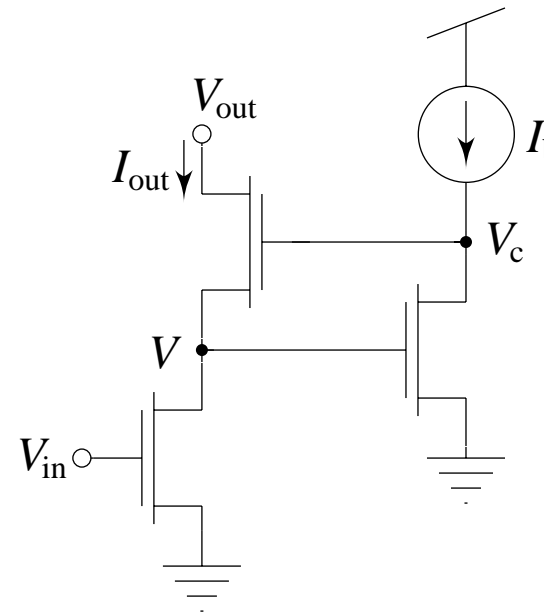
In Search of Low-Voltage Topologies: **Regulated Cascode**

- Säckinger's regulated cascode circuit has a very high incremental R_{out} .



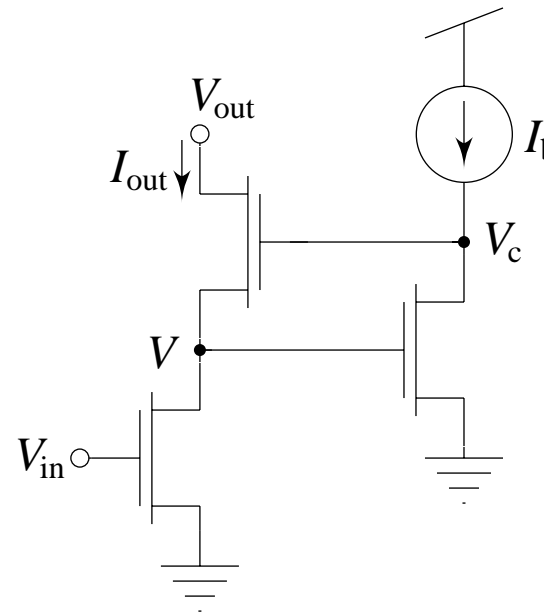
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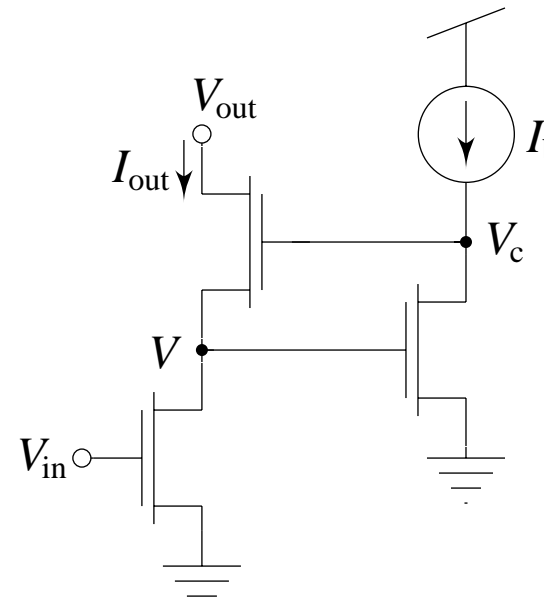
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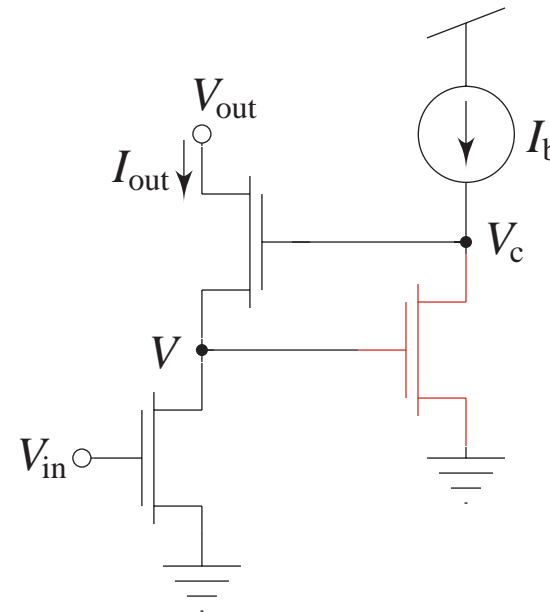
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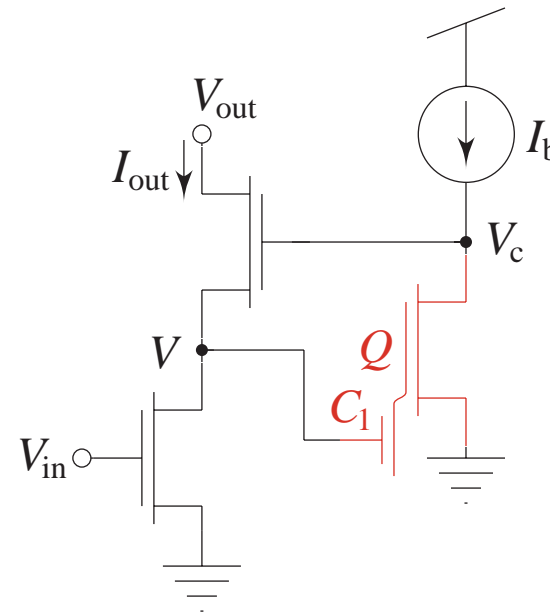
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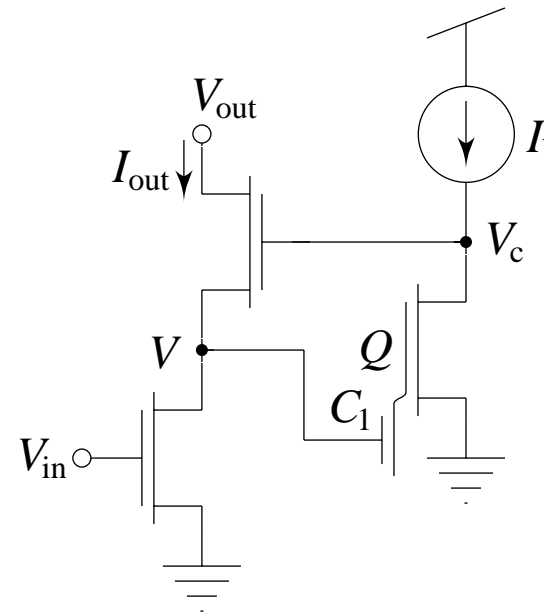
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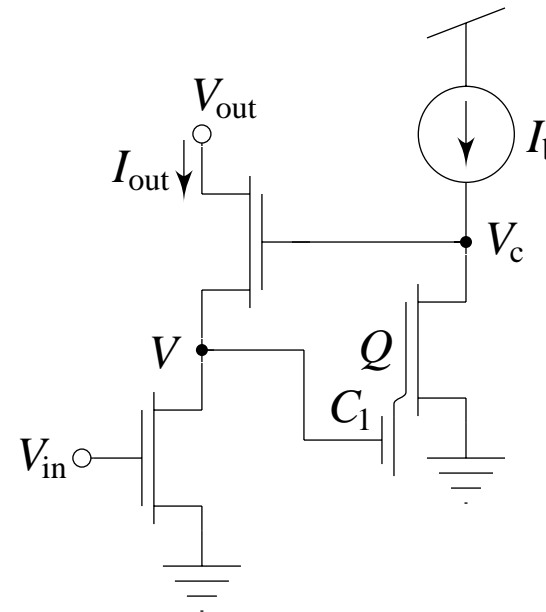
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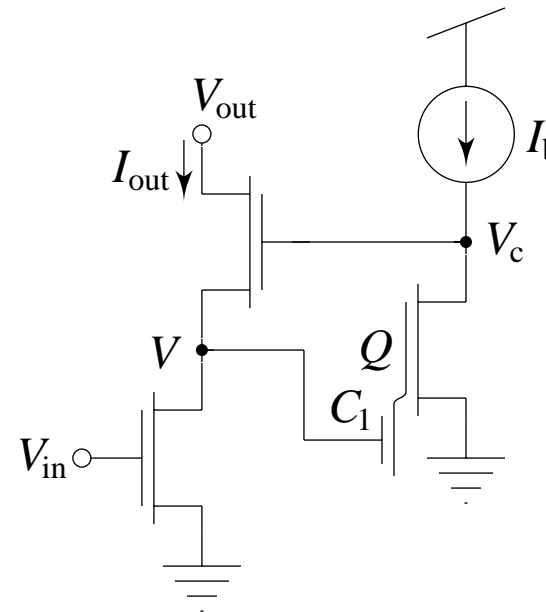
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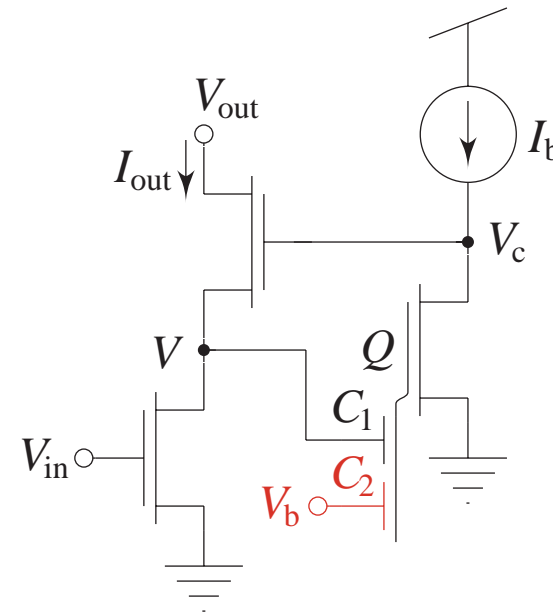
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- Not robust to drift in Q , or changes in I_b or temperature.



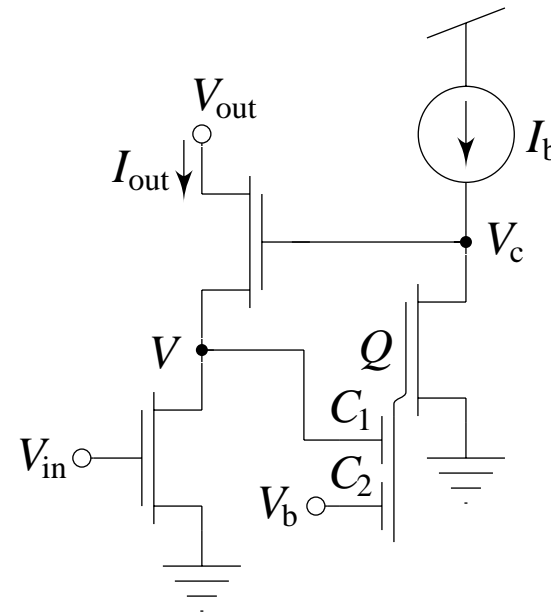
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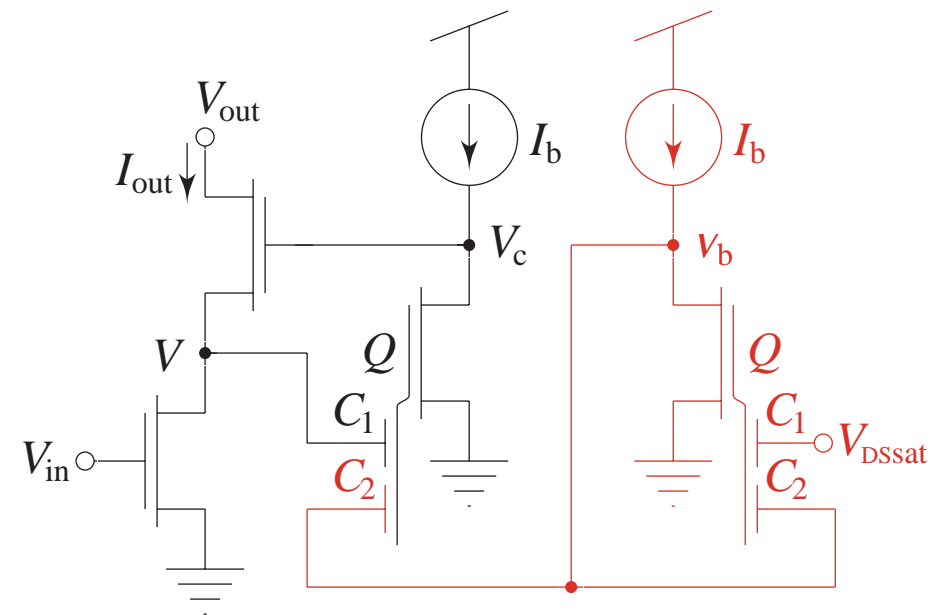
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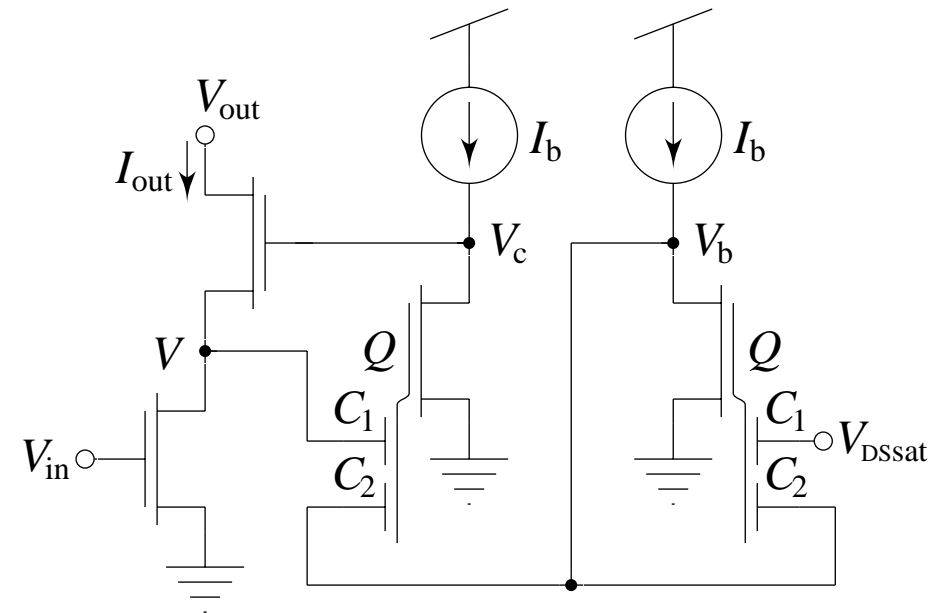
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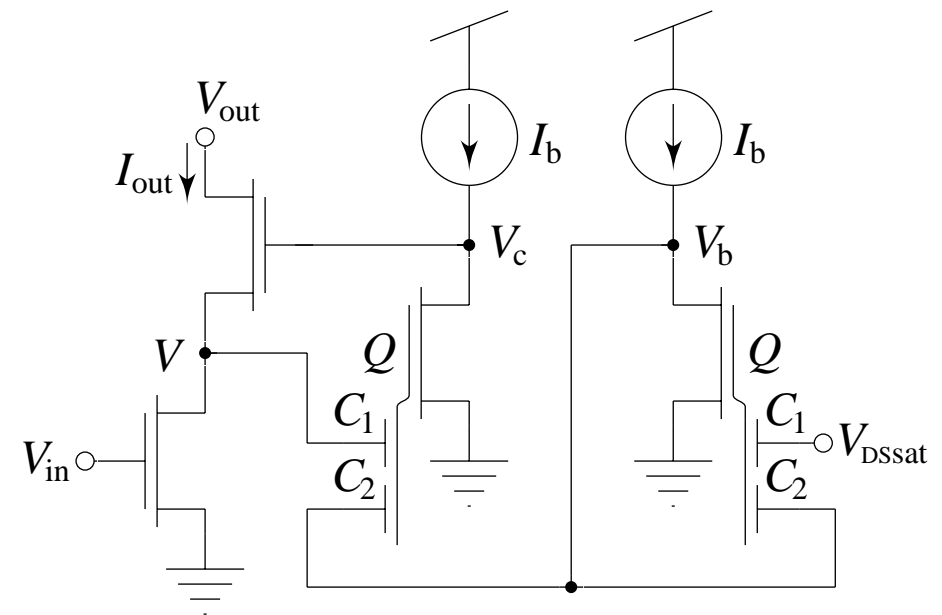
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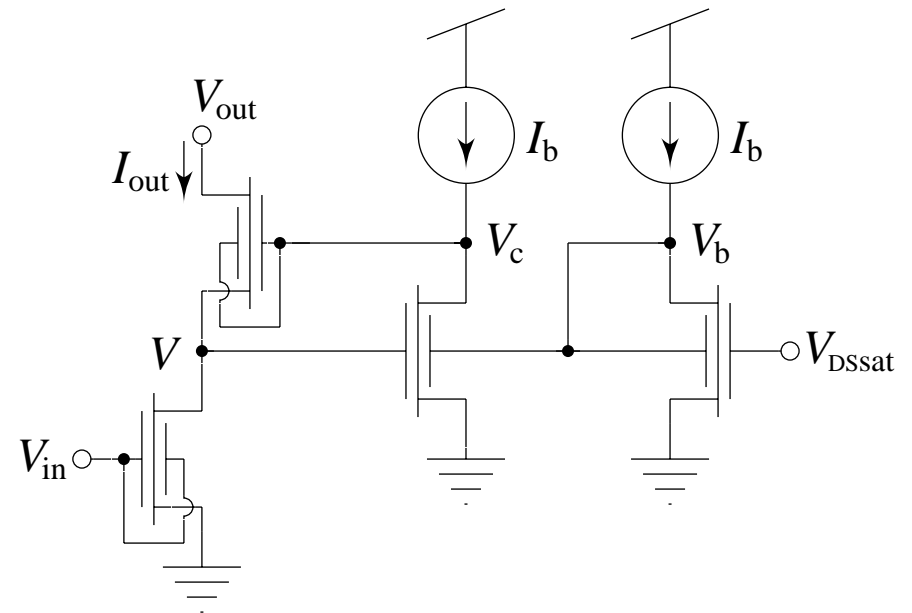
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- One V_b generator can be shared by multiple regulated cascodes.



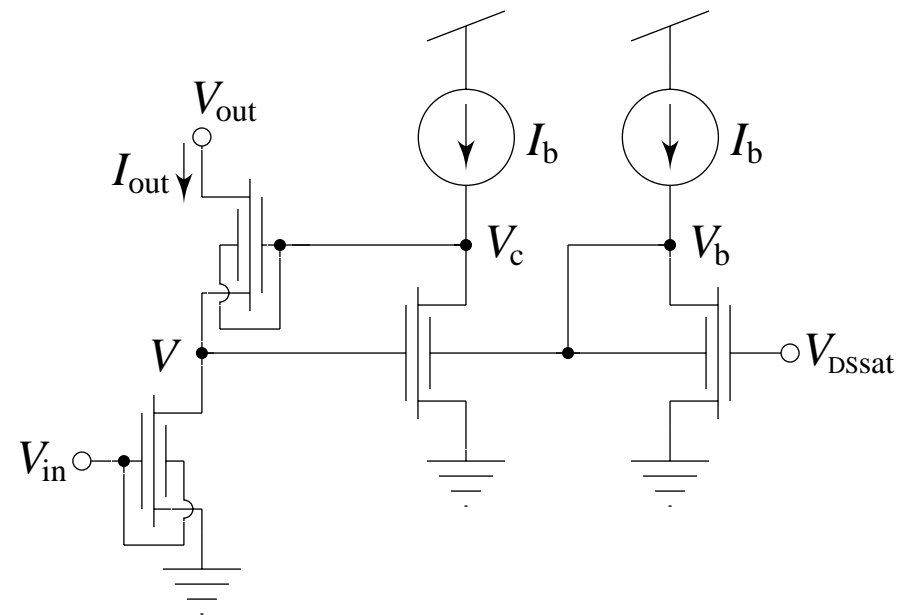
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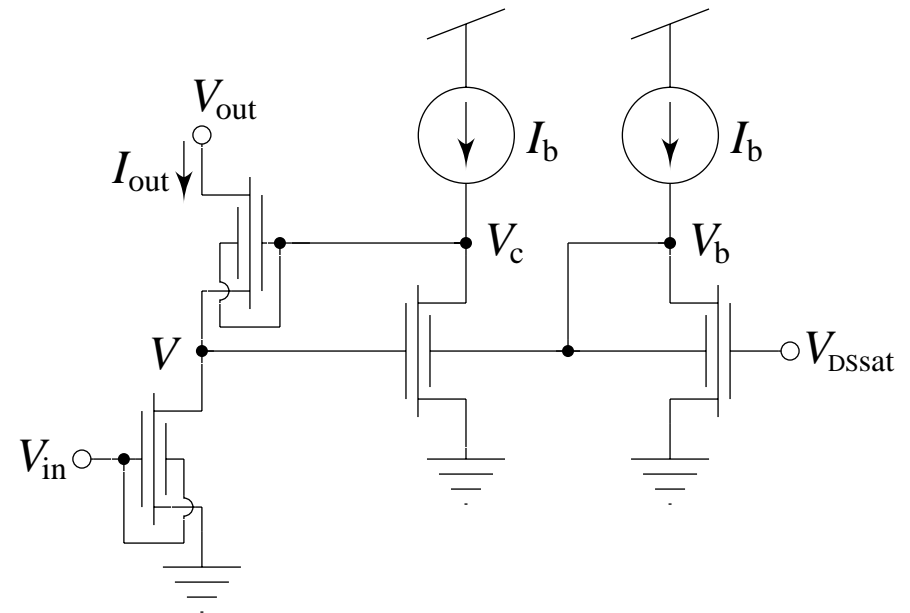
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- Requires independent access to front and back gates.
- Requires that the front and back gate voltages affect the channel current in a (qualitatively) symmetric manner.
- Desirable for the threshold voltages of the front and back gates to both be positive.

