CORNELL
UNIVERSITY
School of Electrical and Computer Engineering

Mixed Analog-Digital VLSI Circuits & Systems Laboratory

Our research presently revolves around two major themes:

- Devising new circuit techniques to facilitate the development of low-power/low-voltage analog and mixed-signal systems.
- Developing structured synthesis methodologies that will shorten the design time for complex analog and mixed-signal systems.

Low-Voltage Topologies for Analog and Mixed-Signal Circuits in Nanoscale CMOS

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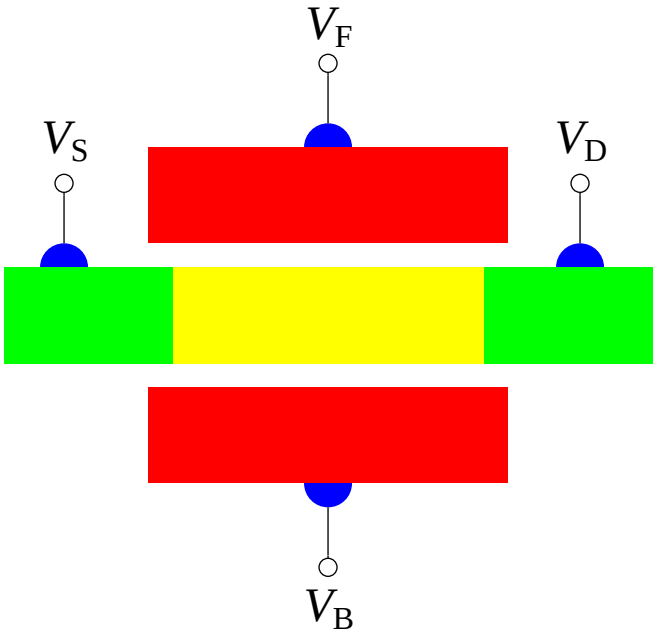
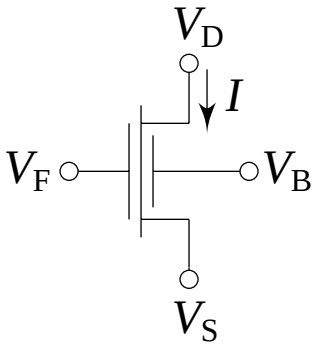
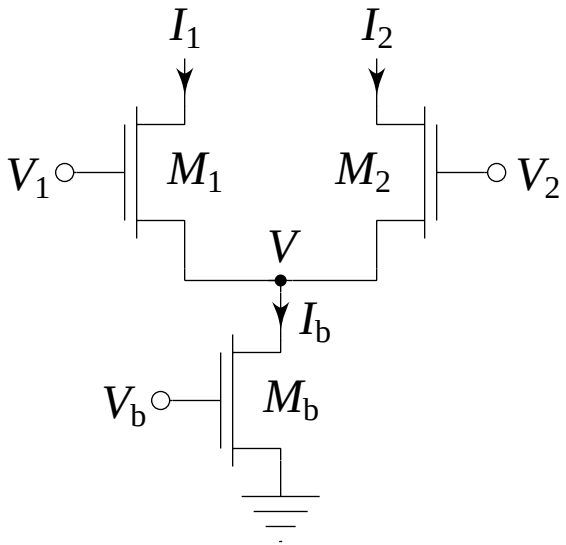
The Double-Gate MOS Transistor

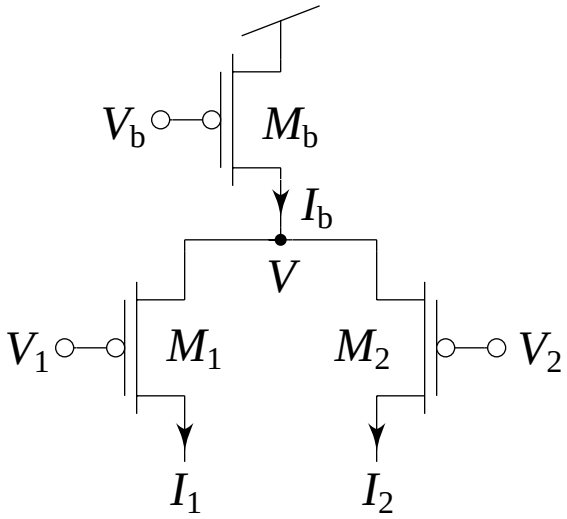




- The double-gate MOS transistor is perhaps the most promising device structure for scaling L down to 20 nm.
- Similar to fully-depleted SOI structure, but back gate provides better control over the potential in the silicon body, reducing short-channel effects.
- In principle, we can use V_F and V_B independently for signal or biasing inputs $\Rightarrow$ new topologies possible!

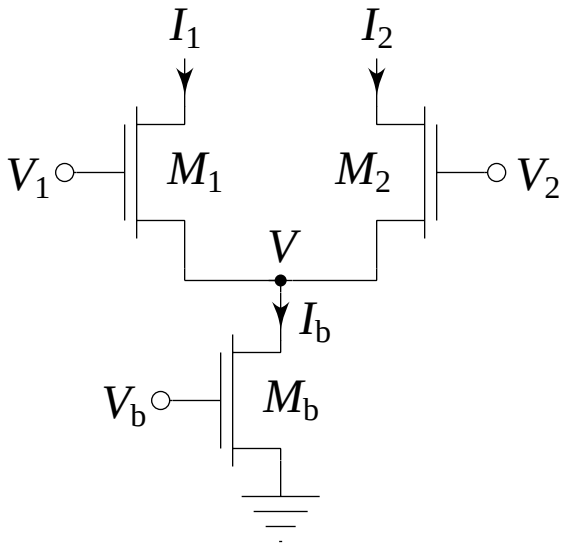
Conventional MOS Differential Pairs

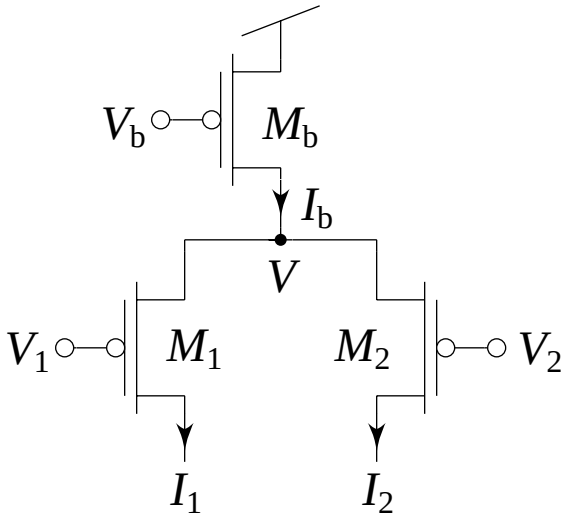




- The differential pair is widely used as an input stage for operational amplifiers, comparators, mixers, and many other circuits.
- This circuit does not function well with a low power-supply voltage, because transistor M_b shuts off if V_1 and V_2 get too close to the appropriate rail.

Conventional MOS Differential Pairs

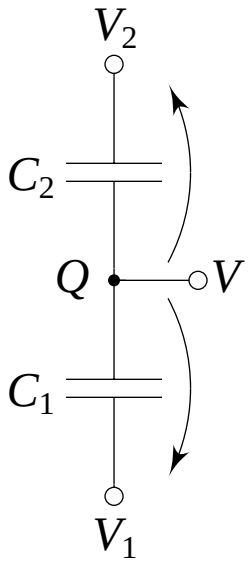




Differential-pair intuition:

- $I_1 = f(g(V_1, -V))$ and $I_2 = f(g(V_2, -V))$, where f is expansive and g is quasilinear.
- V adjusts itself so that $I_1 + I_2 \rightarrow I_b$.

Capacitive Voltage Dividers



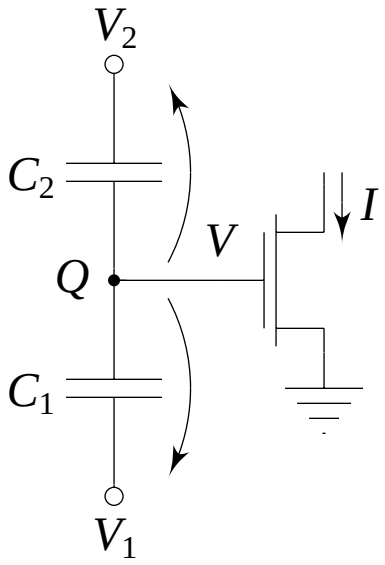
$$-C_1(V_1 - V) - C_2(V_2 - V) = Q$$

$$\Rightarrow (C_1 + C_2)V = C_1V_1 + C_2V_2 + Q$$

$$\Rightarrow \boxed{V = \frac{C_1}{C_1 + C_2}V_1 + \frac{C_2}{C_1 + C_2}V_2 + \frac{Q}{C_1 + C_2}}$$

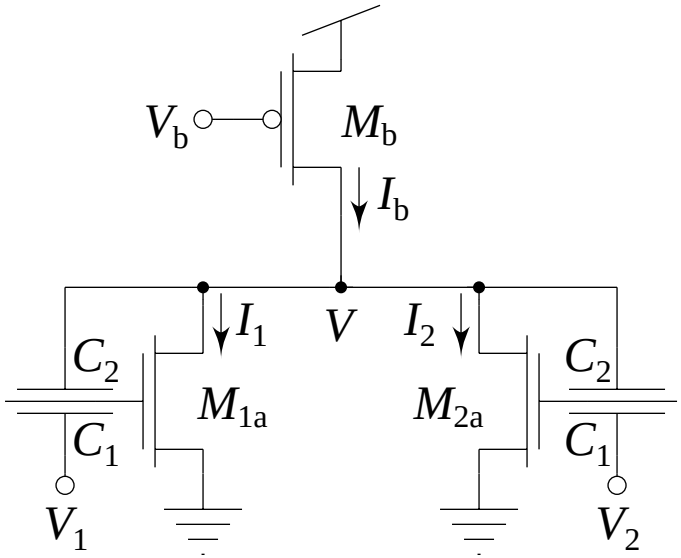
- The voltage on the middle node is a weighted sum of the two input voltages.
- If node V is really floating, then the inputs couple into the floating node all the way down to DC!
- The charge Q linearly offsets the V. The charge can be adjusted either optically or electronically.

Floating-Gate MOS Transitors



- The capacitors C_1 and C_2 are called *control gates*.
- If floating-gate voltage, V, is a weighted sum of the control-gate voltages.
- The floating-gate charge, Q, can be thought of as giving us a programmable threshold voltage.

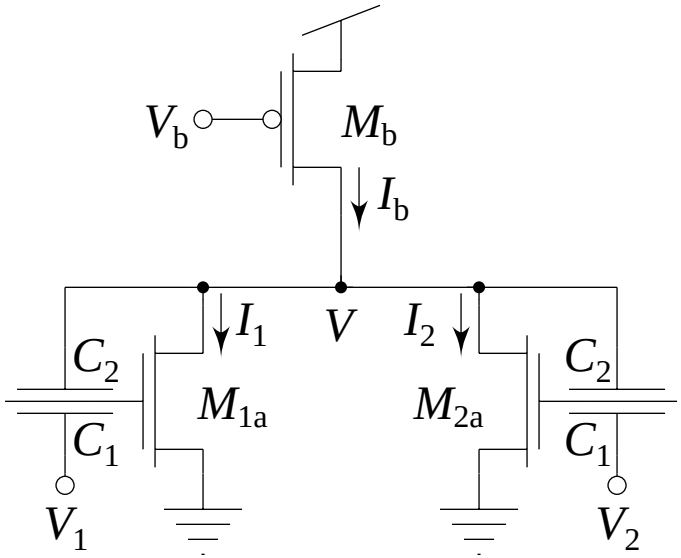
An Inverted Floating-Gate Differential Pair



Differential-pair intuition:

- $I_1 = f(g(V_1, V))$ and $I_2 = f(g(V_2, V))$, where f is expansive and g is quasilinear.
- V adjusts itself so that $I_1 + I_2 \rightarrow I_b$.

An Inverted Floating-Gate Differential Pair



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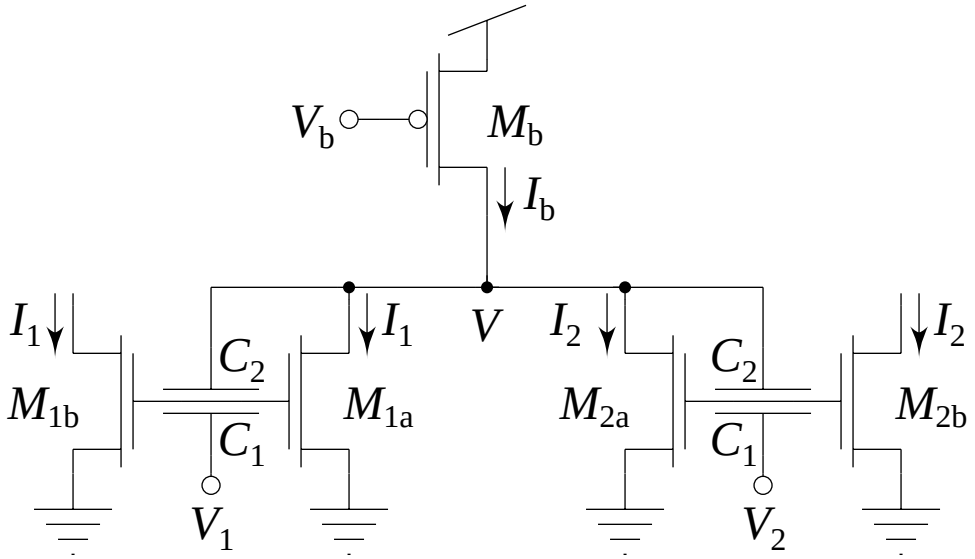
Sign reversal permits us to *invert* V w.r.t. the normal diffpair.

An Inverted Floating-Gate Differential Pair

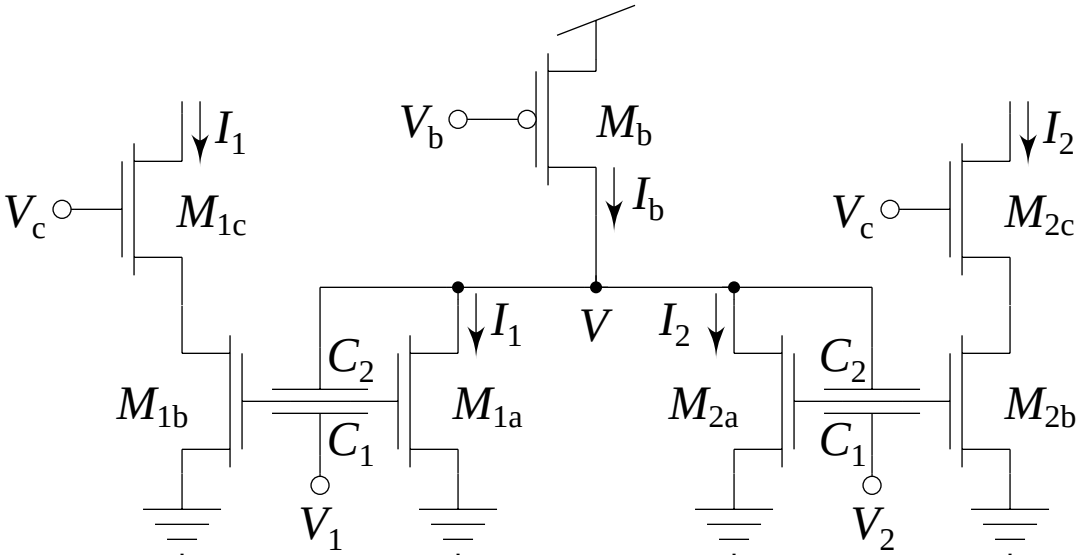


Differential-pair intuition:

- $I_1 = f(g(V_1, V))$ and $I_2 = f(g(V_2, V))$, where f is expansive and g is quasilinear.
- V adjusts itself so that $I_1 + I_2 \rightarrow I_b$.

M_{1b} and M_{2b} provide mirror copies of I_1 and I_2.

An Inverted Floating-Gate Differential Pair

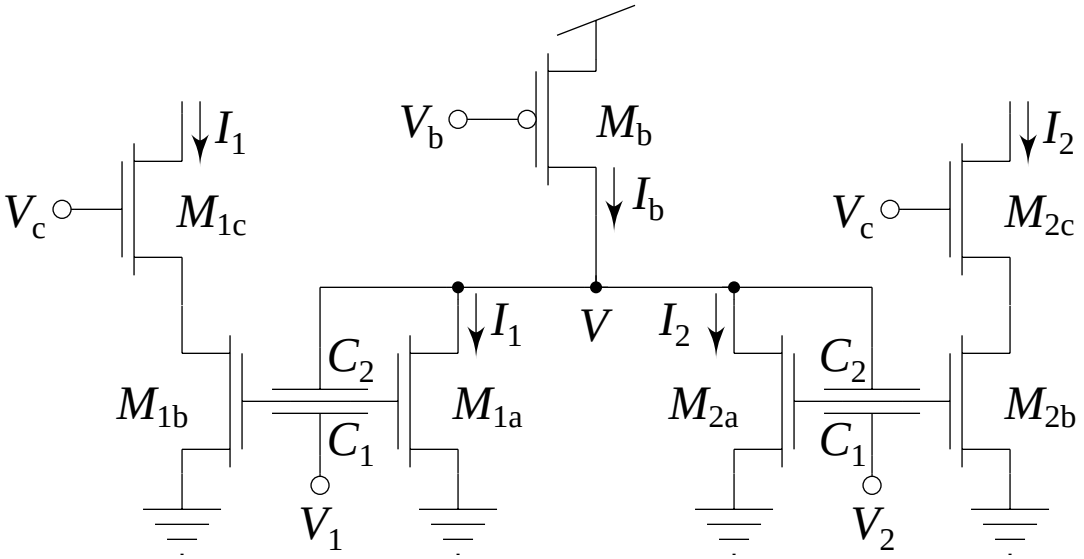


Differential-pair intuition:

- $I_1 = f(g(V_1, V))$ and $I_2 = f(g(V_2, V))$, where f is expansive and g is quasilinear.
- V adjusts itself so that $I_1 + I_2 \rightarrow I_b$.

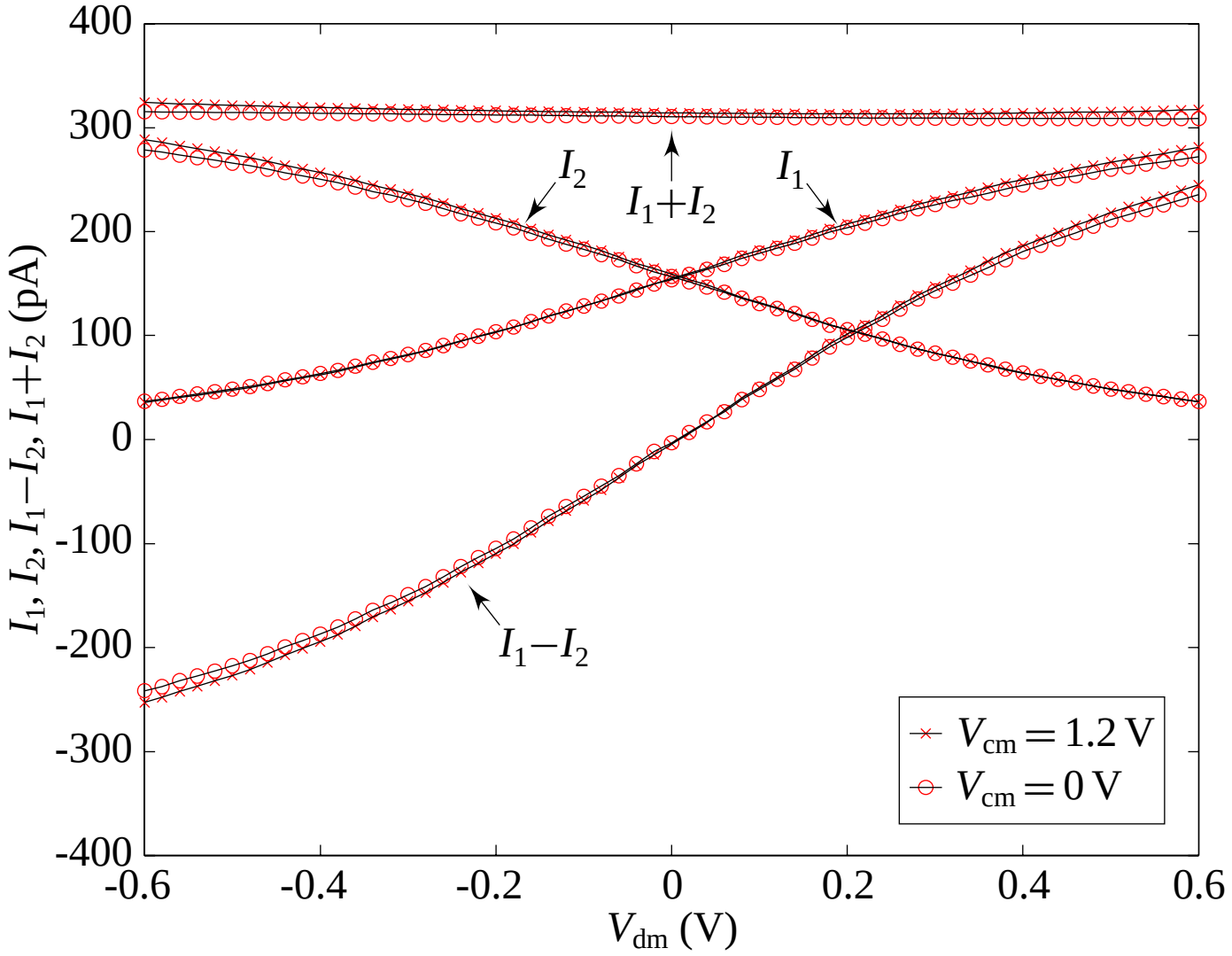
M_{1c} and M_{2c} mitigate the C_{gd}'s of transistors M_{1b} and M_{2b}.

An Inverted Floating-Gate Differential Pair

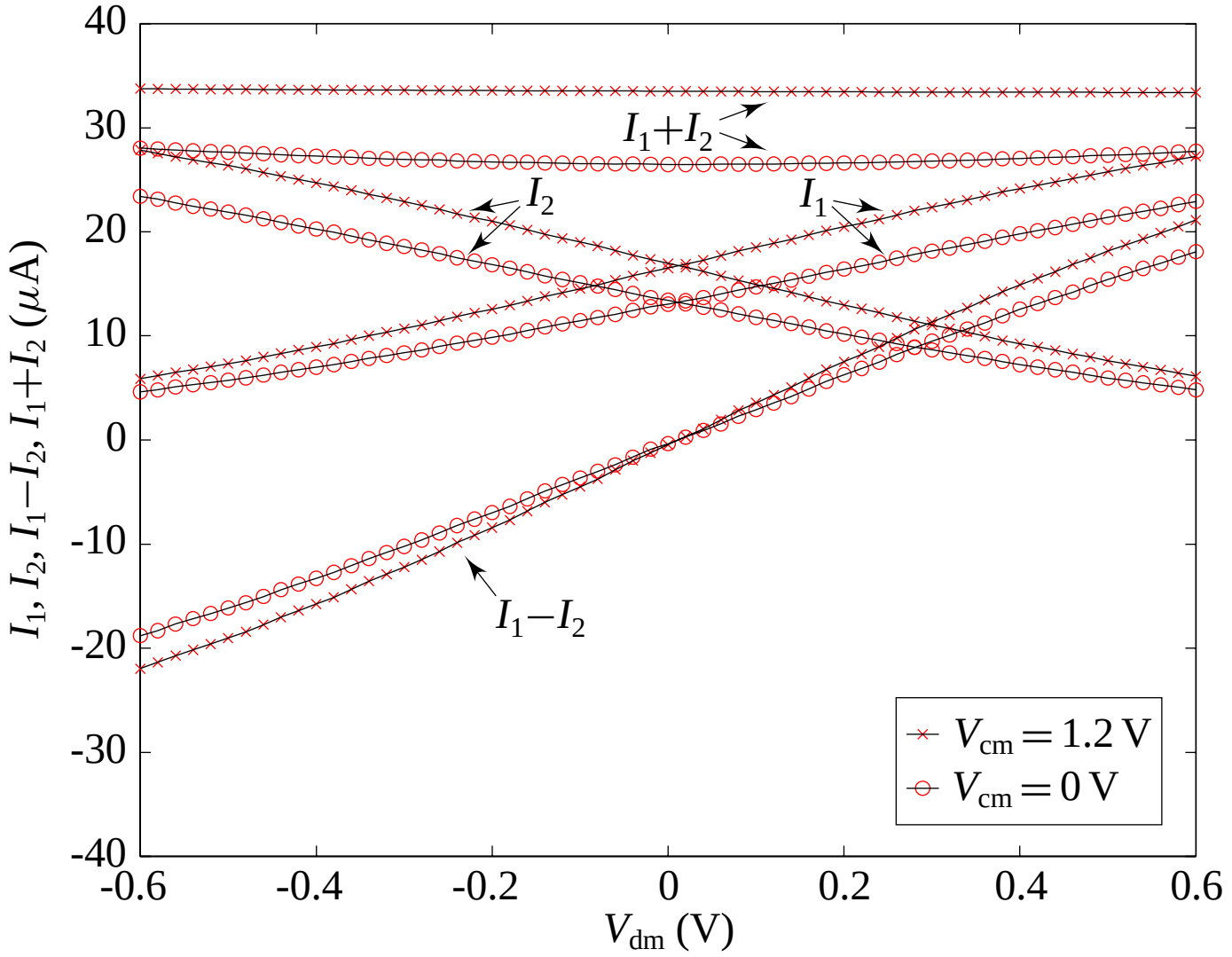


- C_1 sets the linear range and transconductance gain.
- C_2 controls by how much V changes in response to changes in either V_{cm} or I_b.
- Input and output voltage ranges are from rail-to-rail.
- Transconductance gain nearly constant with V_{cm}.

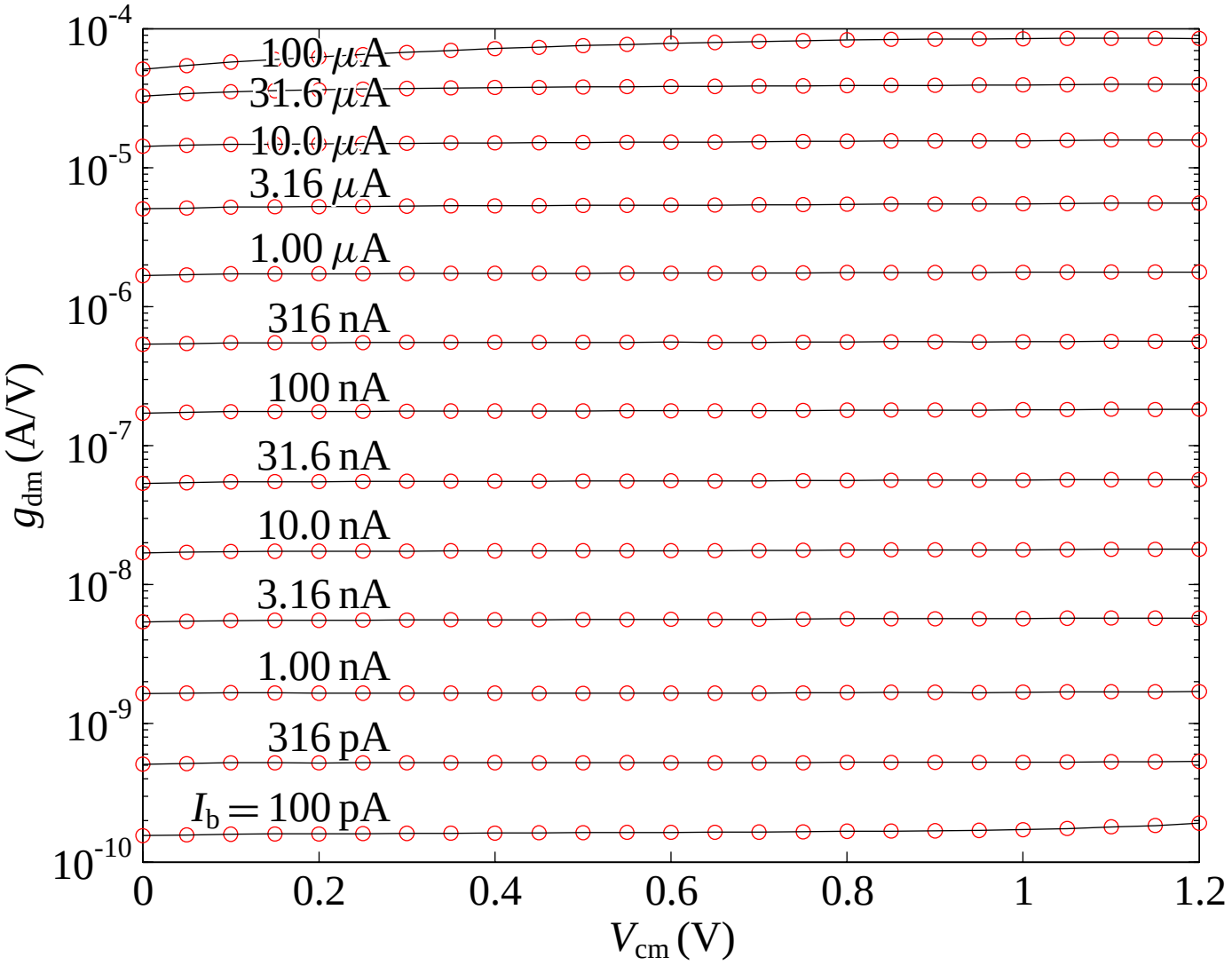
Output Currents vs. V_{dm} ($I_b = 316\,pA$)



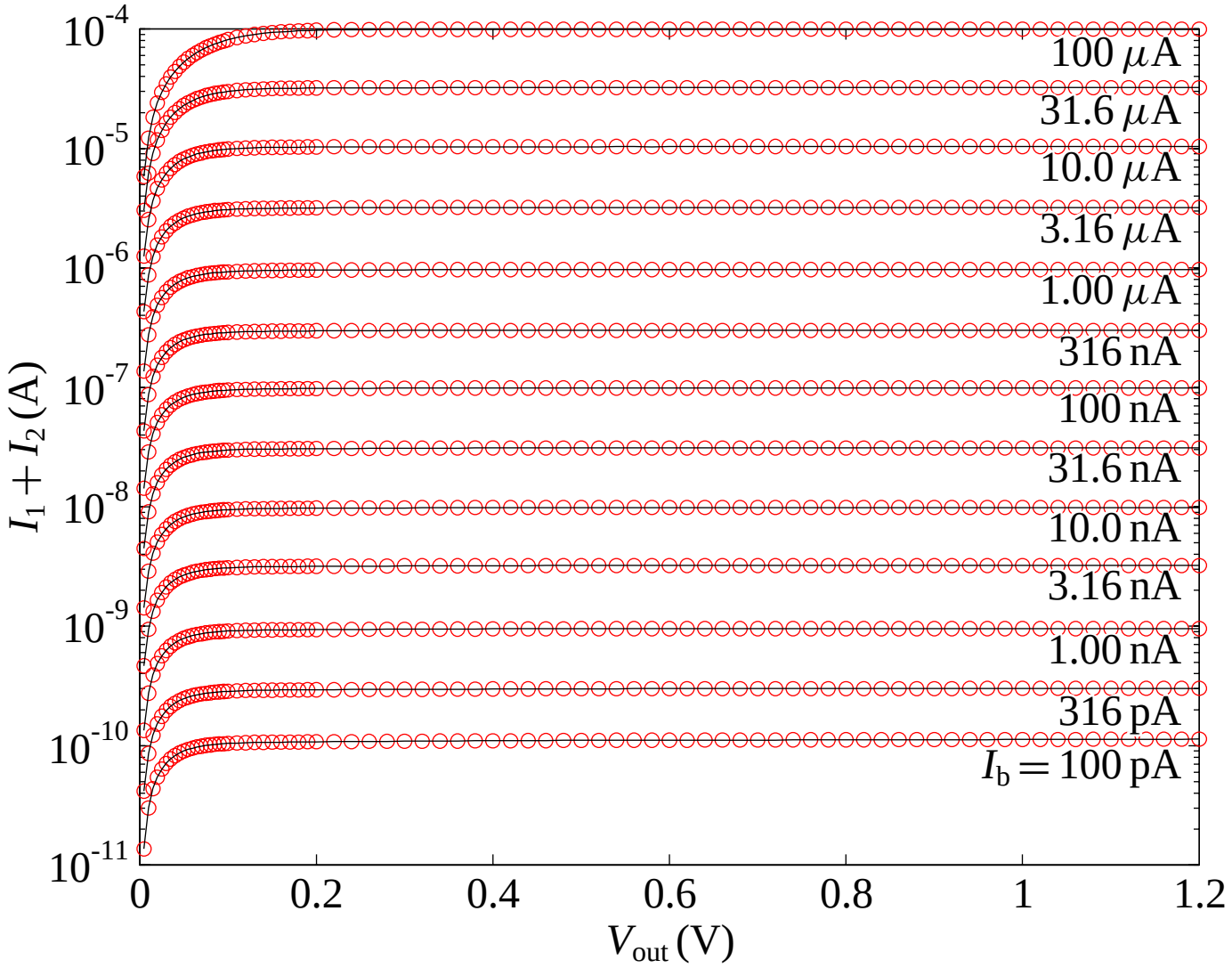
Output Currents vs. V_{dm} ($I_{\mathrm{b}} = 31.6\,\mu\mathrm{A}$)



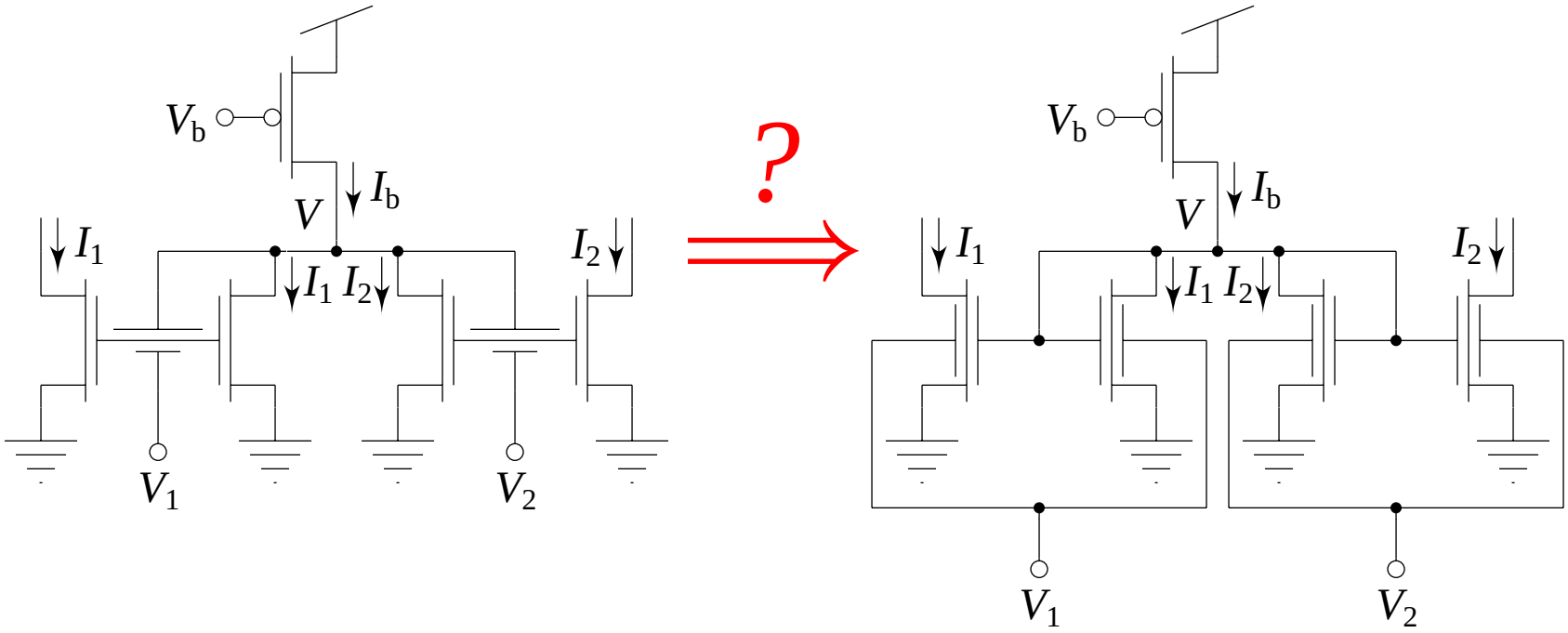
Transconductance Gain vs. V_{cm}



Common-Mode Output Current vs. V_{out}



A Double-Gate MOS Inverted Differential Pair?



- Requirements for DGMOS version to be feasible:
  - Independent front and back gates
  - V_1 and V affect I_1 in a similar manner
  - V_2 and V affect I_2 in a similar manner
  - V transconductance larger than V_1 and V_2
  - V_1, V_2, and $V \geq$ ground