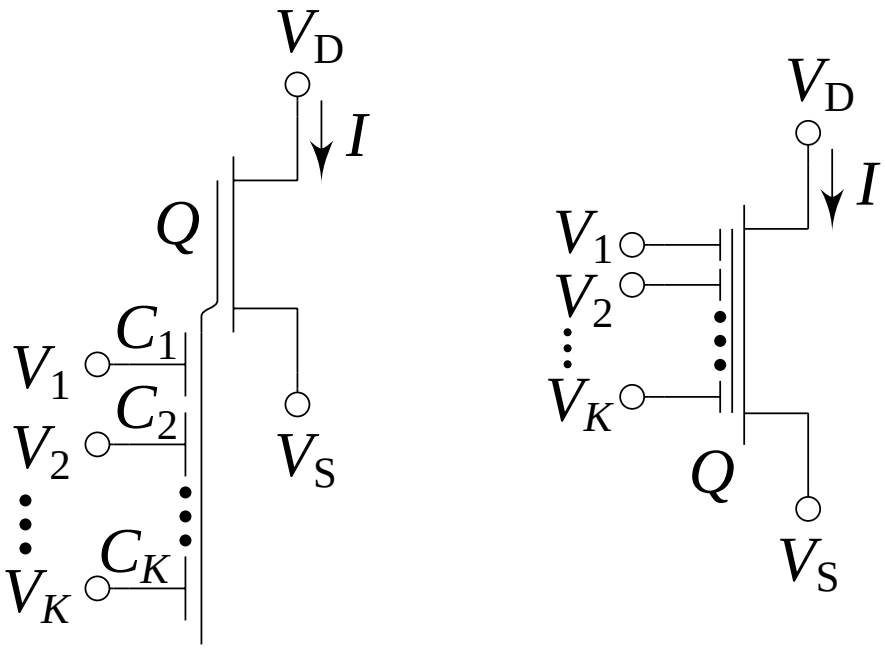
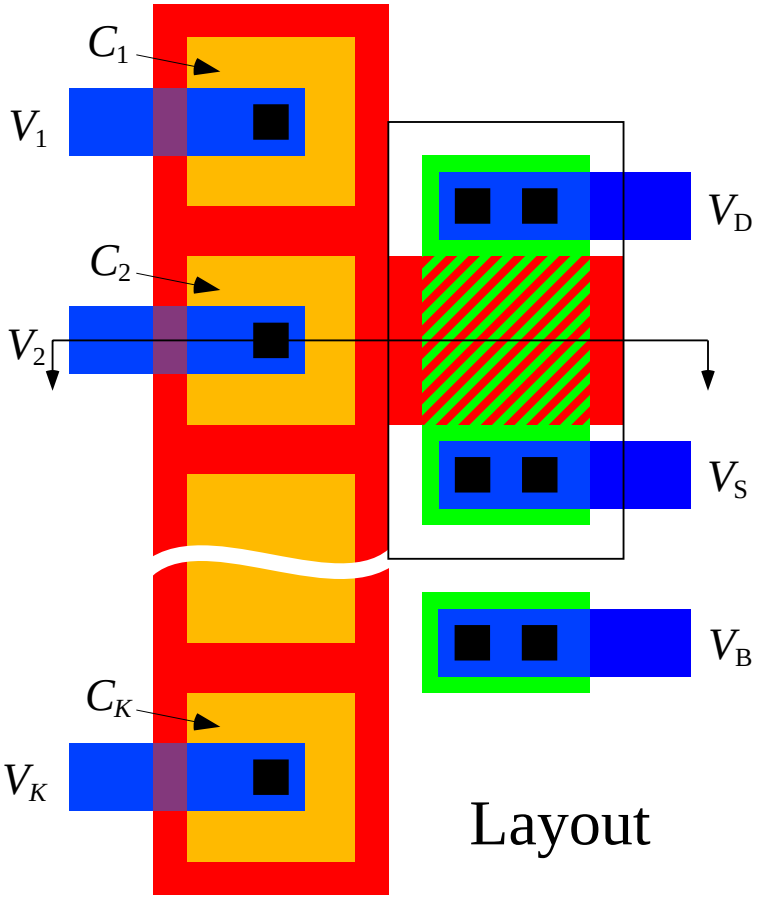
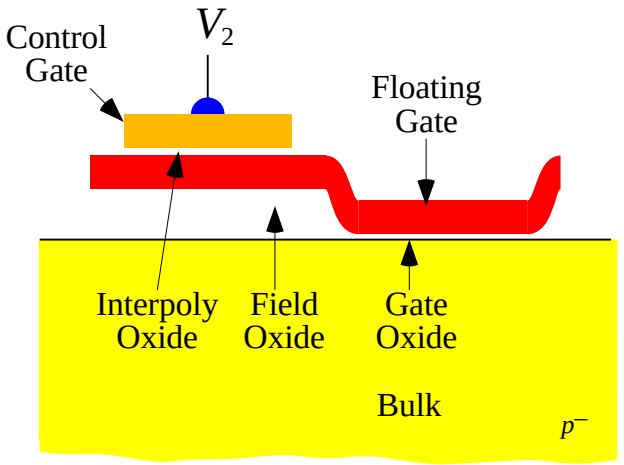
The *K*-Input Floating-Gate MOS (FGMOS) Transistor



Circuit Symbols



Layout

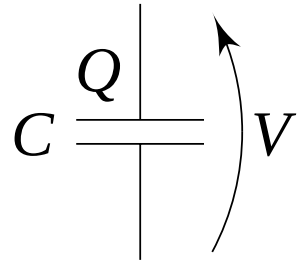


Cross-section

Capacitive Voltage Dividers

- When trying to solve capacitor networks, it pays to think $Q = CV$ rather than

$$I = C\frac{dV}{dt}$$

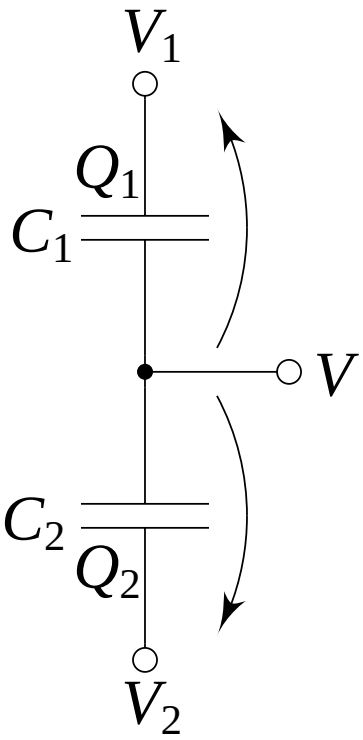


- Assume no net charge on the middle node.
- By conservation of charge,

$$-Q_1 - Q_2 = 0$$

$$\Rightarrow -C_1(V_1 - V) - C_2(V_2 - V) = 0$$

$$\Rightarrow \boxed{V = \frac{C_1}{C_1 + C_2}V_1 + \frac{C_2}{C_1 + C_2}V_2}$$



Capacitive Voltage Dividers

- For all k, $Q_k = C_k(V_k - V)$
- Net charge Q on the common node.
- By conservation of charge,

$$-\sum_{k=1}^{K} Q_k = Q$$

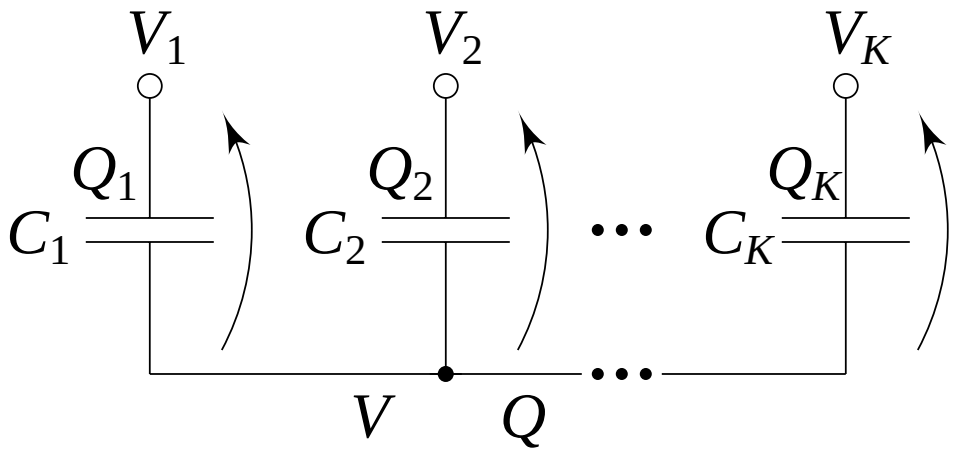
$$\Rightarrow -\sum_{k=1}^{K} C_k(V_k - V) = Q$$

$$\Rightarrow V\sum_{k=1}^{K} C_k = Q + \sum_{k=1}^{K} C_k V_k$$

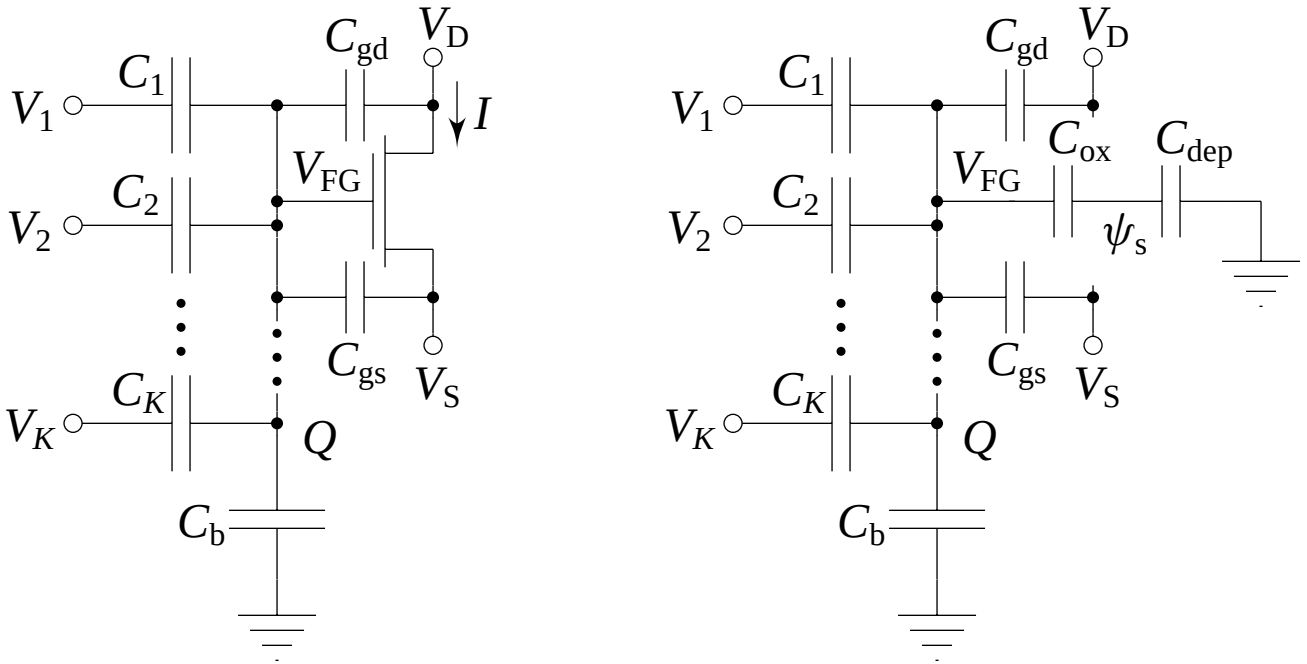
$$\Rightarrow \boxed{V = \frac{Q}{C_\mathrm{T}} + \sum_{k=1}^{K} \frac{C_k}{C_\mathrm{T}} V_k}$$

where

$$C_\mathrm{T} \equiv \sum_{k=1}^{K} C_k$$



Capacitive-Divider Model of the Subthreshold FGMOS Transistor



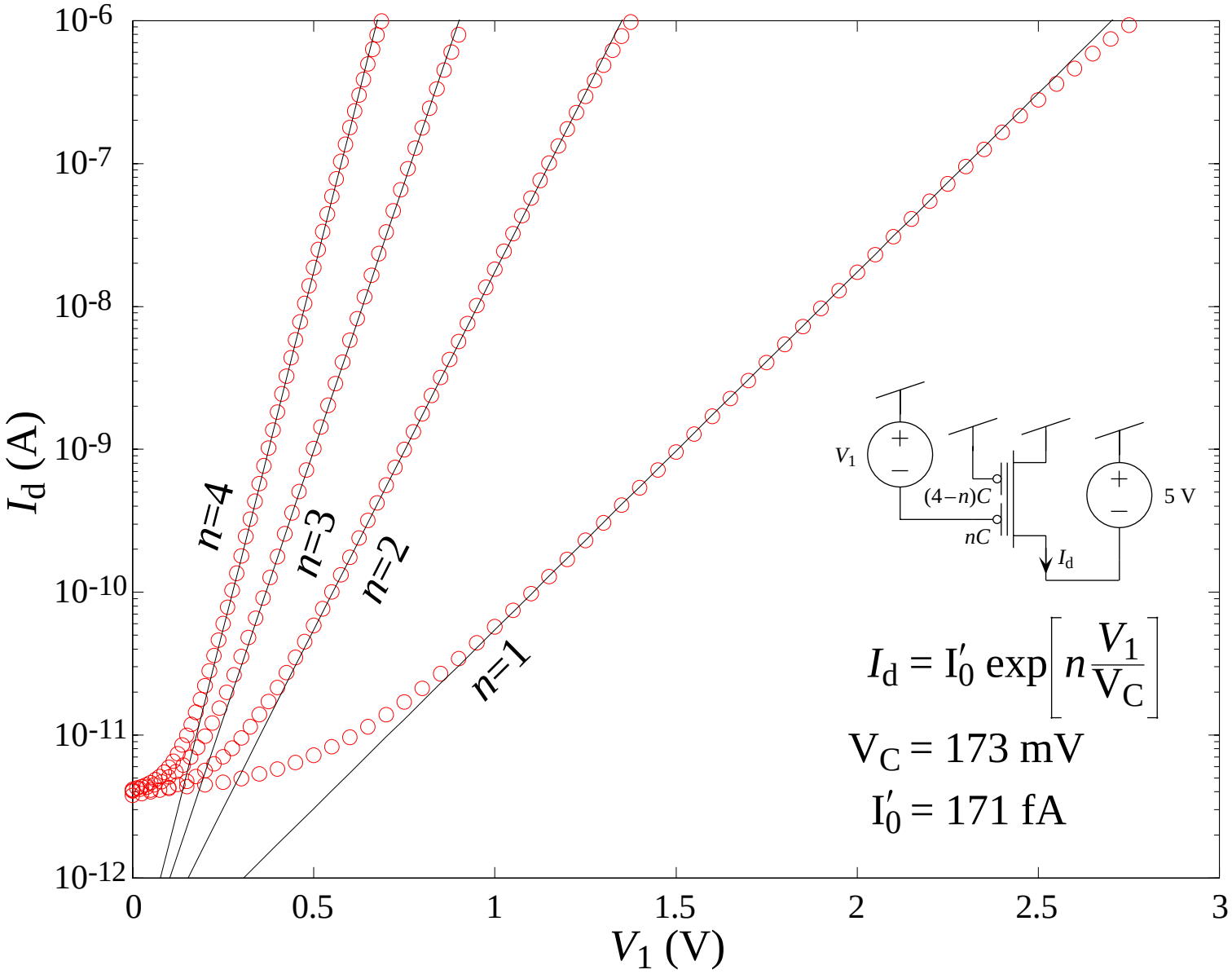
$$V_{FG} = \frac{Q}{C_T} + \frac{C_{gs}}{C_T}V_S + \frac{C_{gd}}{C_T}V_D + \sum_{k=1}^{K}\frac{C_k}{C_T}V_k$$

$$C_T = \left(C_{ox} \| C_{dep}\right) + C_b + C_{gs} + C_{gd} + \sum_{k=1}^{K} C_k$$

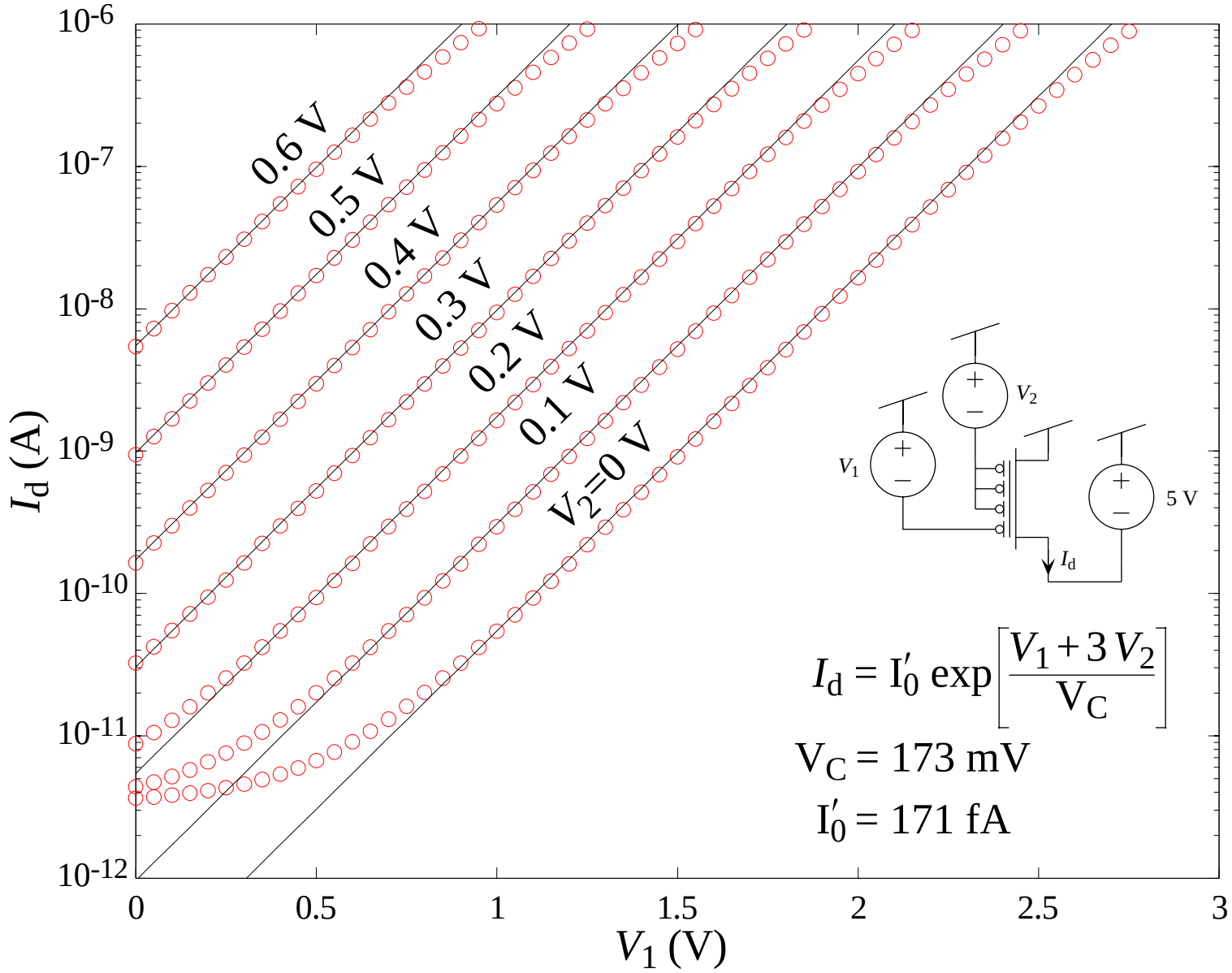
$$I = I_0 e^{\kappa V_{FG}/U_T}\left(e^{-V_S/U_T} - e^{-V_D/U_T}\right)$$

$$I = I_0 e^{\kappa Q/C_T U_T}\, e^{\kappa(C_1V_1+\cdots+C_KV_K)/C_T U_T}\, e^{\kappa C_{gd}V_D/C_T U_T}\, e^{\kappa C_{gs}V_S/C_T U_T}\left(e^{-V_S/U_T} - e^{-V_D/U_T}\right)$$

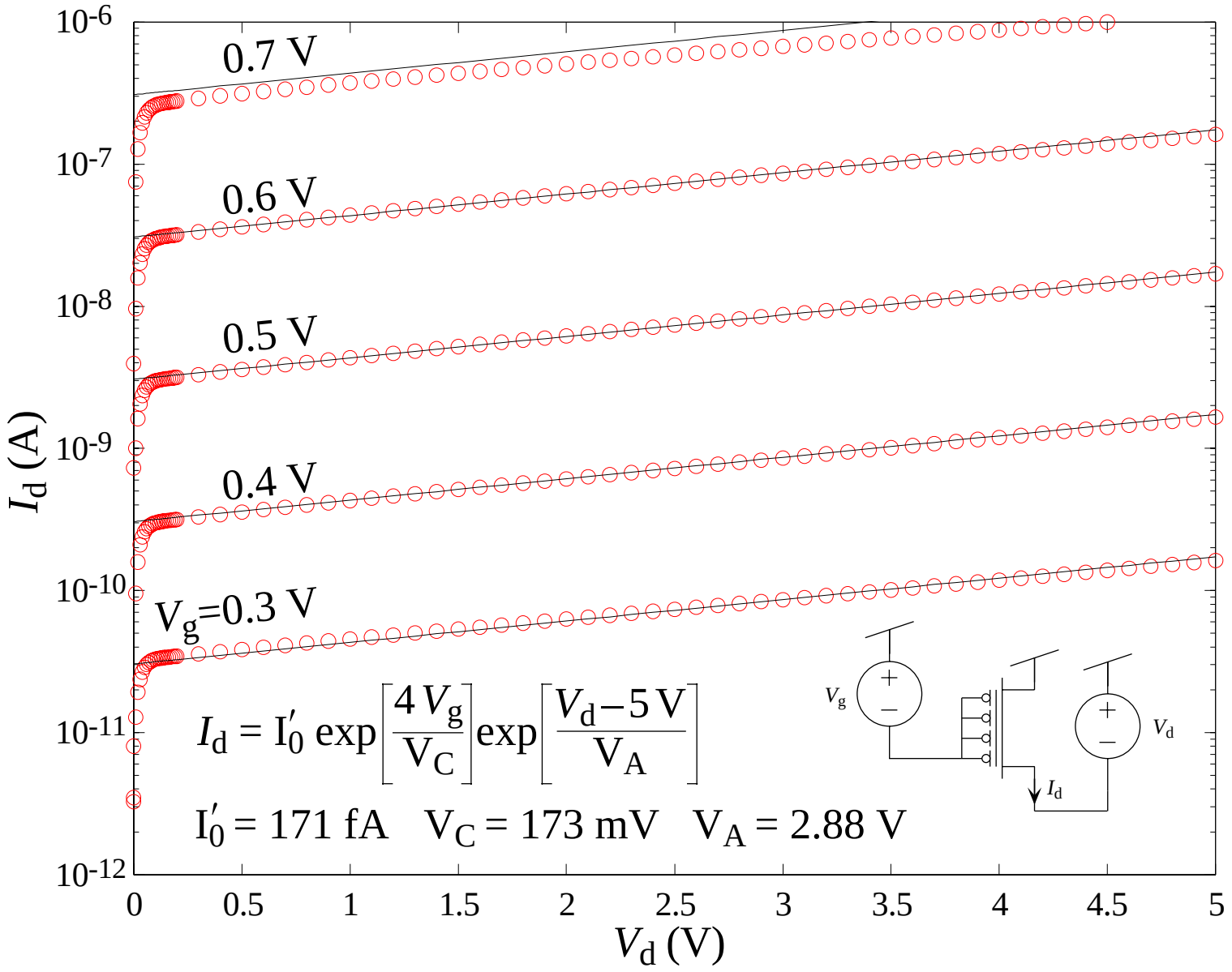
Subthreshold FGMOS Transistor



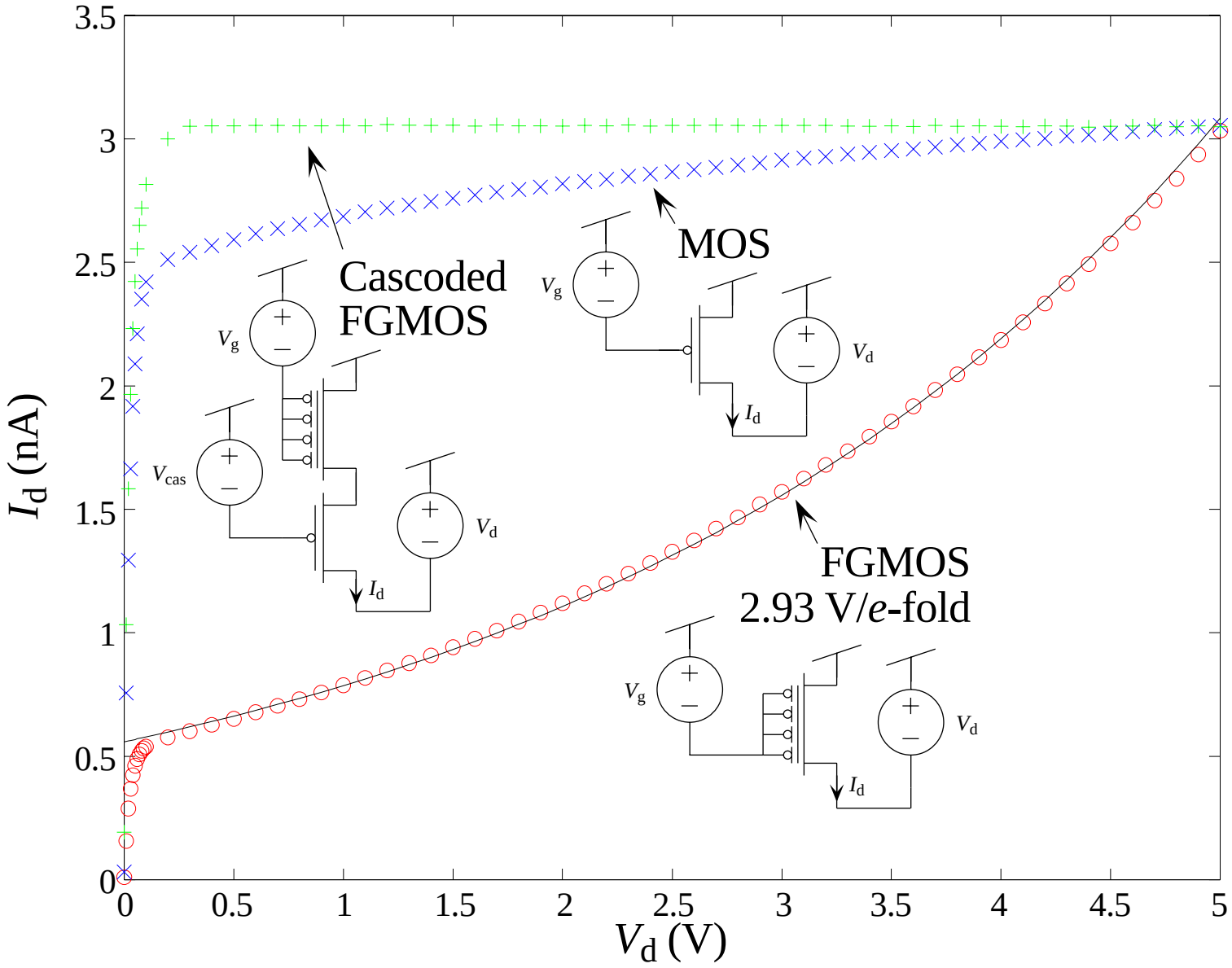
Subthreshold FGMOS Transistor



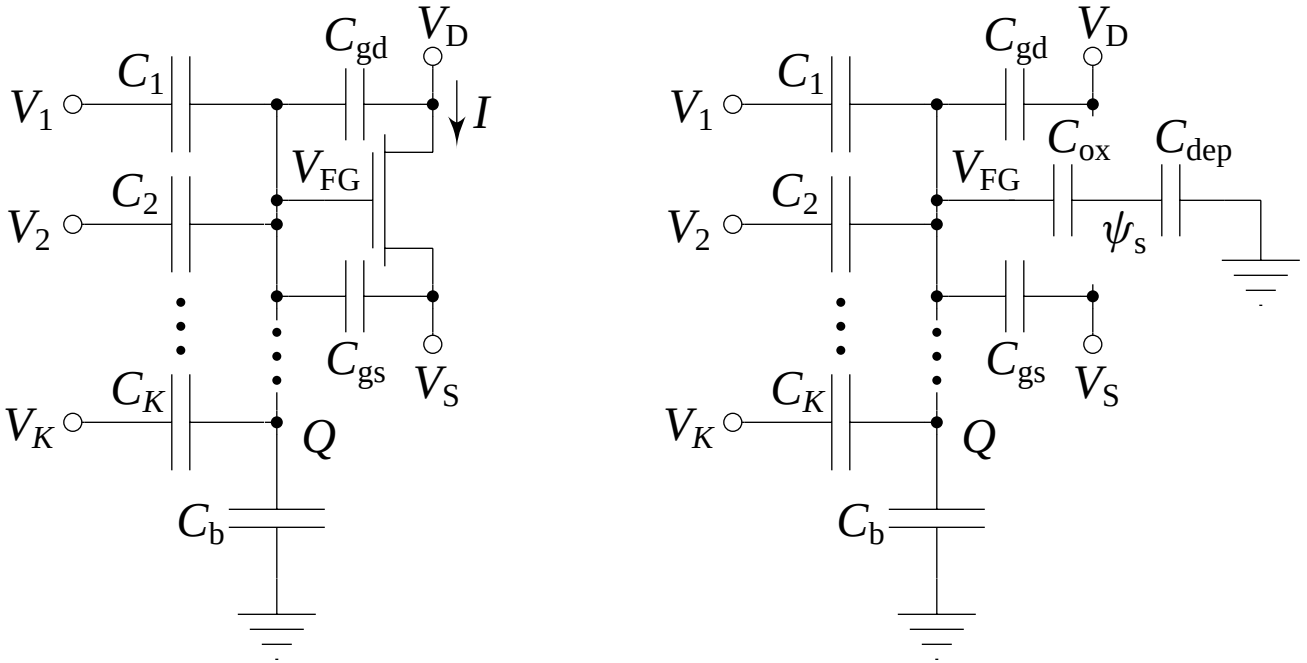
Subthreshold FGMOS Transistor: Drain Characteristics



Subthreshold FGMOS Transistor: Drain Characteristics



Capacitive-Divider Model of the Above-Threshold FGMOS Transistor

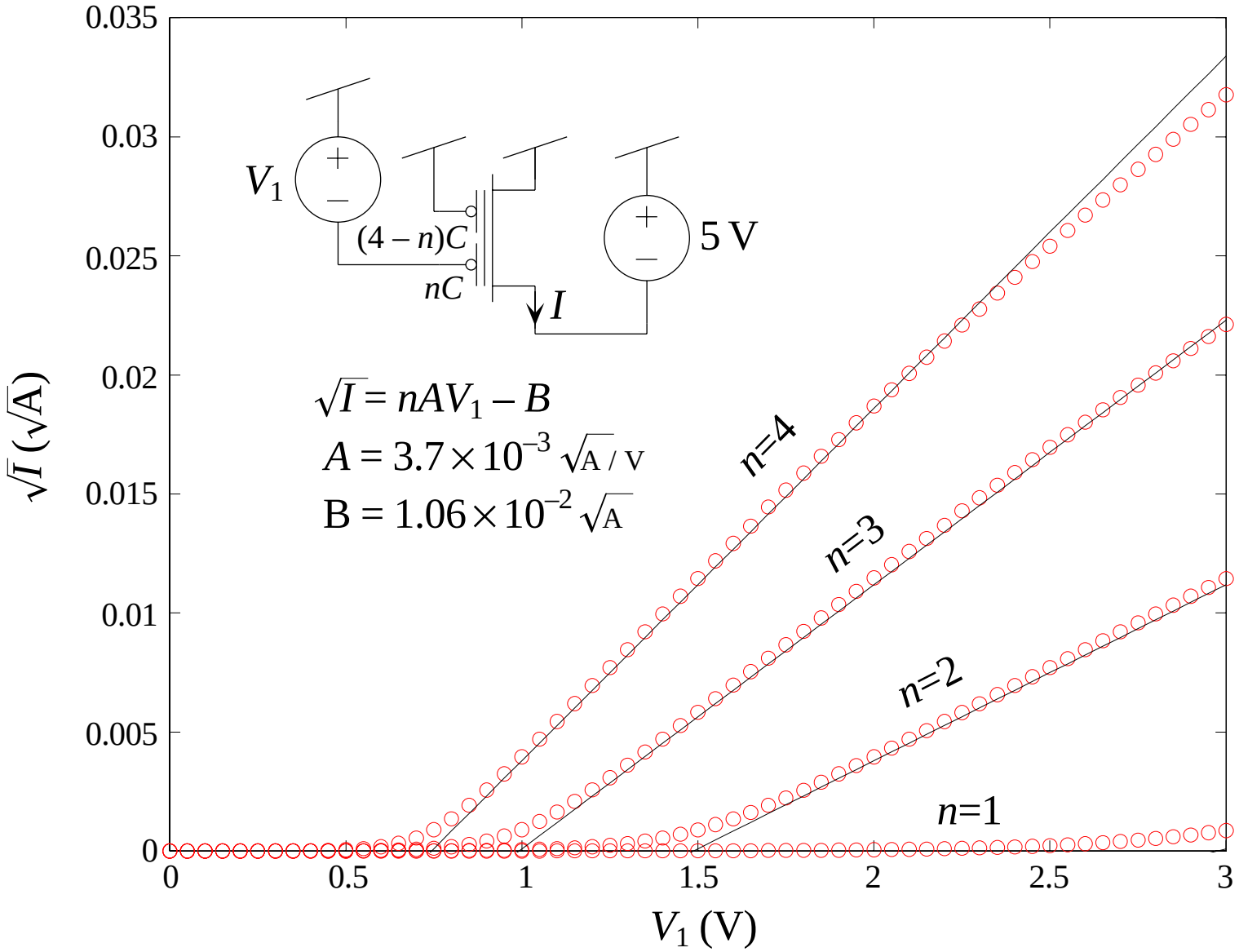


$$I = \frac{W}{L}\frac{\mu C_{ox}}{2\kappa}\left(\left(\kappa\left(V_{FG} - V_{T0}\right) - V_S\right)^2 - \left(\kappa\left(V_{FG} - V_{T0}\right) - V_D\right)^2\right)$$

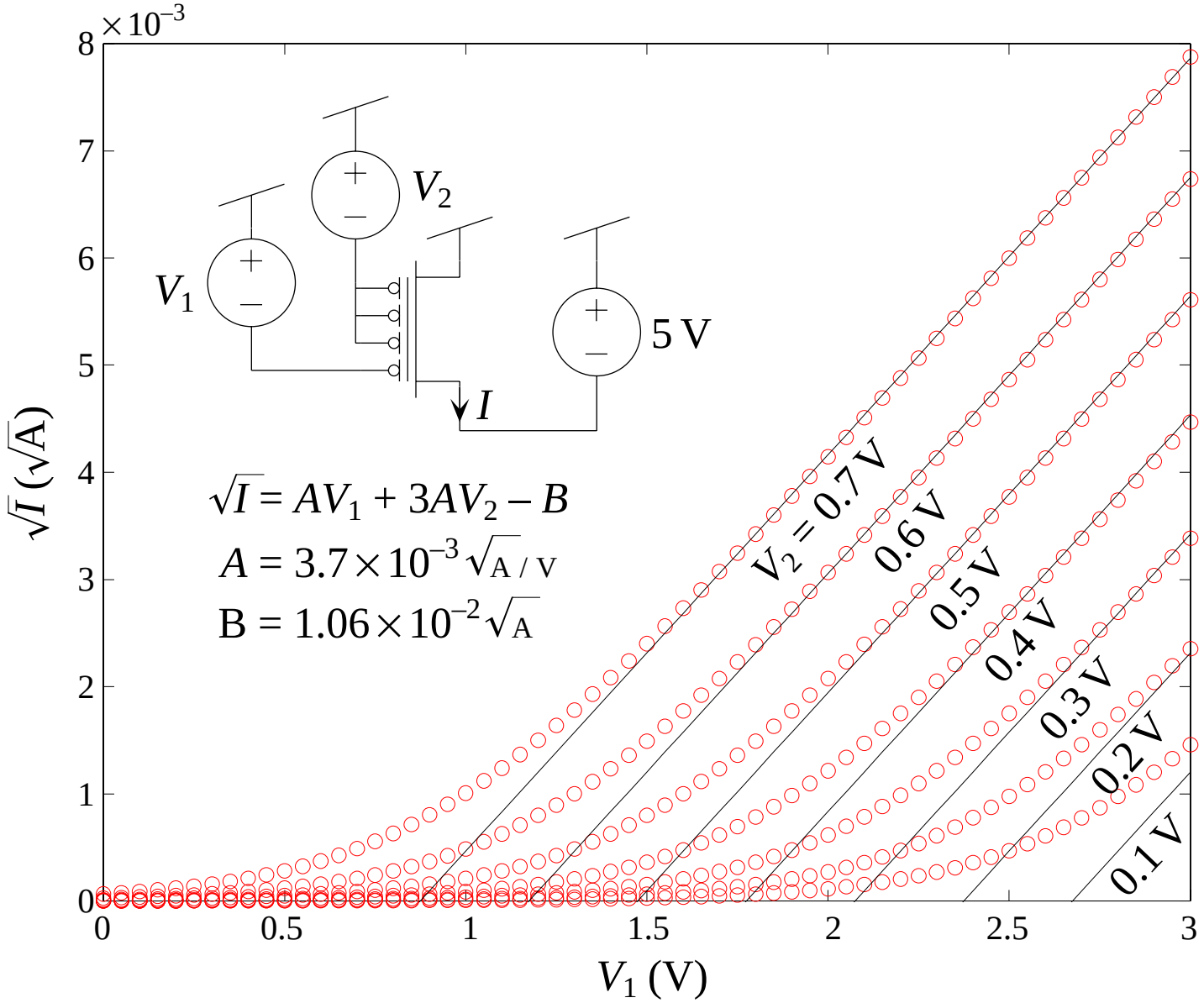
$$I = \frac{W}{L}\frac{\mu C_{ox}}{2\kappa}\left(\left(\kappa\left(\sum_{k=1}^{K}\frac{C_k}{C_T}V_k - V_{T0}^*\right) - V_S\right)^2 - \left(\kappa\left(\sum_{k=1}^{K}\frac{C_k}{C_T}V_k - V_{T0}^*\right) - V_D\right)^2\right)$$

$$V_{T0}^* = V_{T0} - \frac{Q}{C_T} - \frac{C_{gs}}{C_T}V_S - \frac{C_{gd}}{C_T}V_D$$

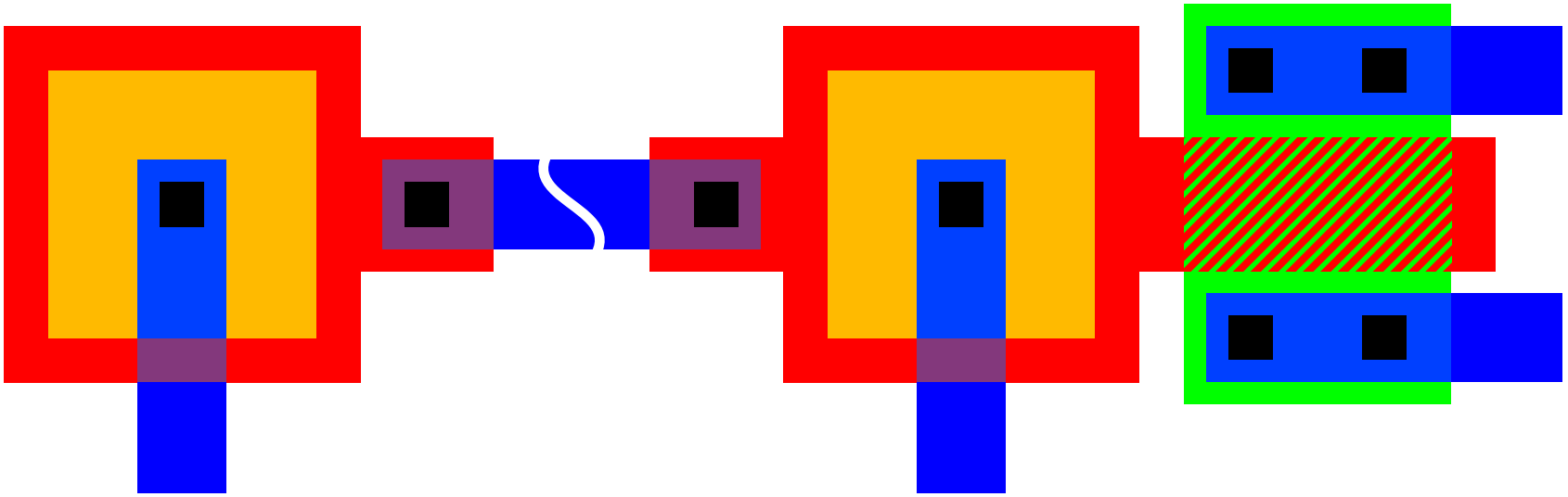
Above-Threshold FGMOS Transistor



Above-Threshold FGMOS Transistor

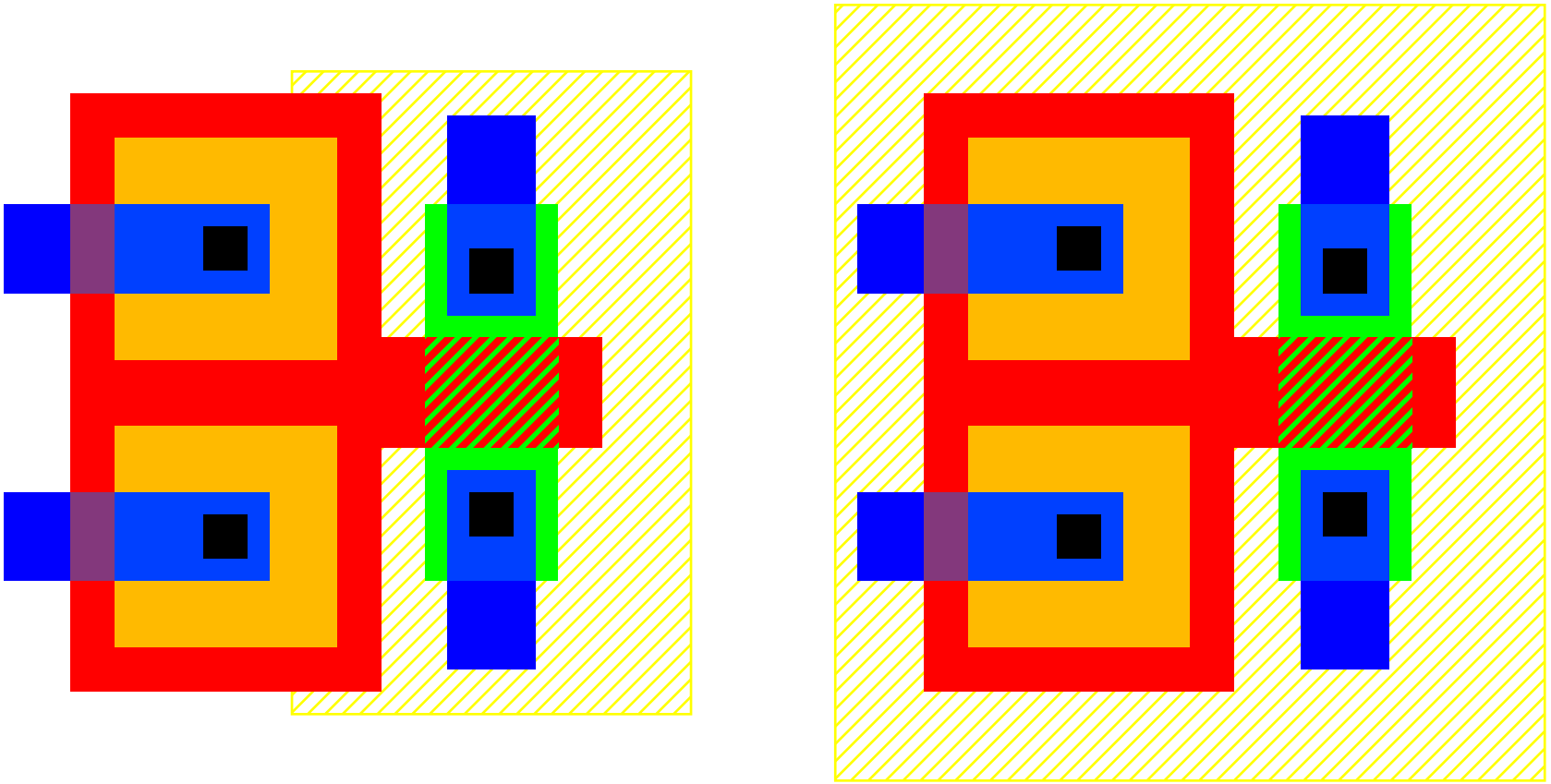


How to Make Leaky Floating Gates...



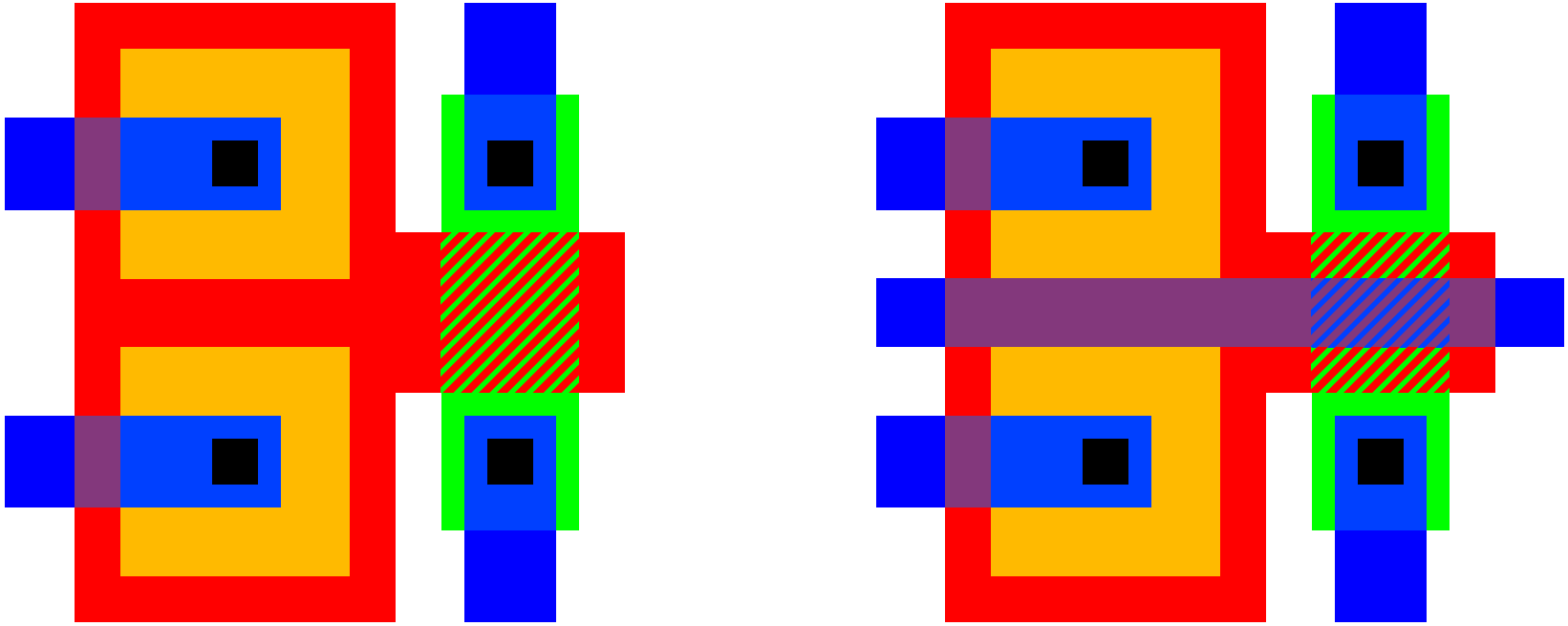
- Keep your floating gates on poly1.
- If you make a contact to metal, your gate will probably leak, because the oxide surrounding the metal layers are typically deposited rather than thermally grown.

Beware of Capacitive Coupling from Below...



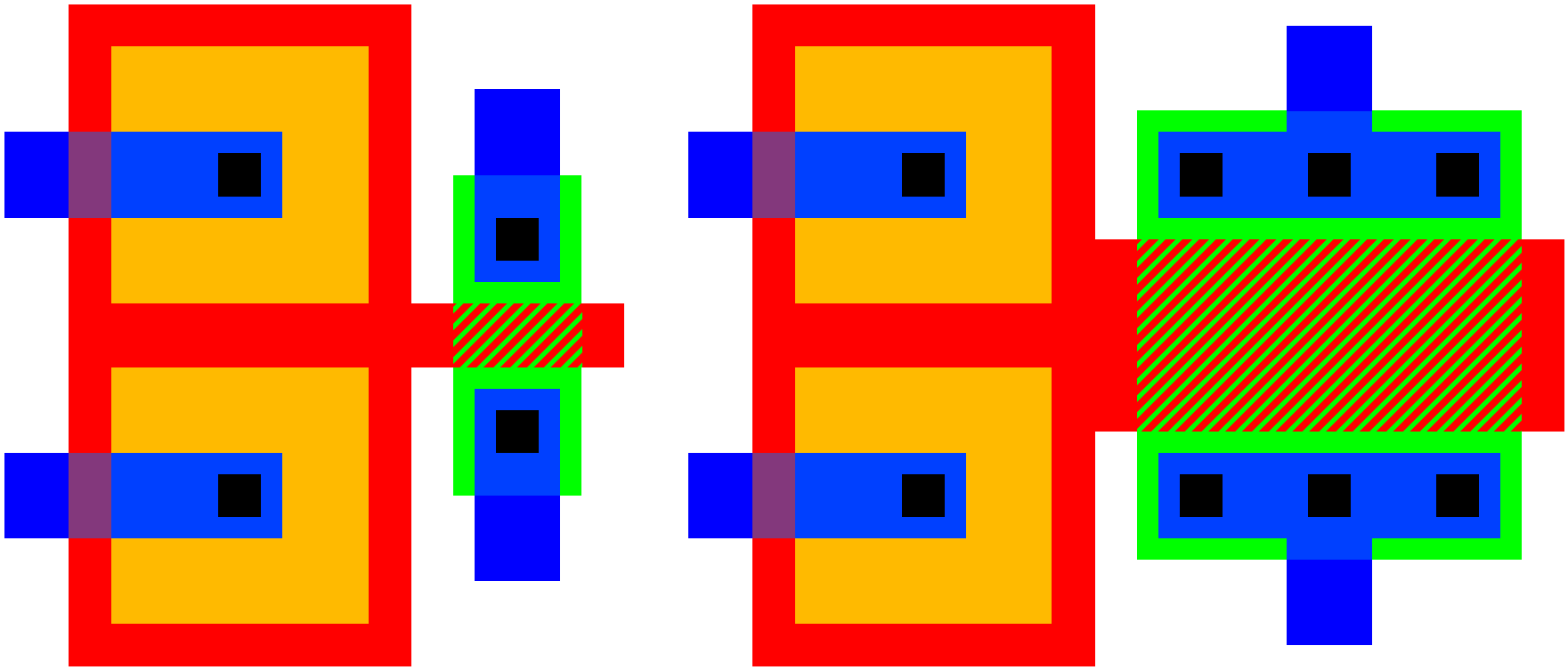
- If possible, don't allow a floating gate to cross a well boundary. For a *p*FGMOS, keep it entirely over the well. For an *n*FGMOS, keep it entirely over the substrate.
- If you split the area evenly between the substrate and the well, your floating-gate voltage will have a dependence on V_{DD} that you didn't expect...

Beware of Capacitive Coupling from Above...

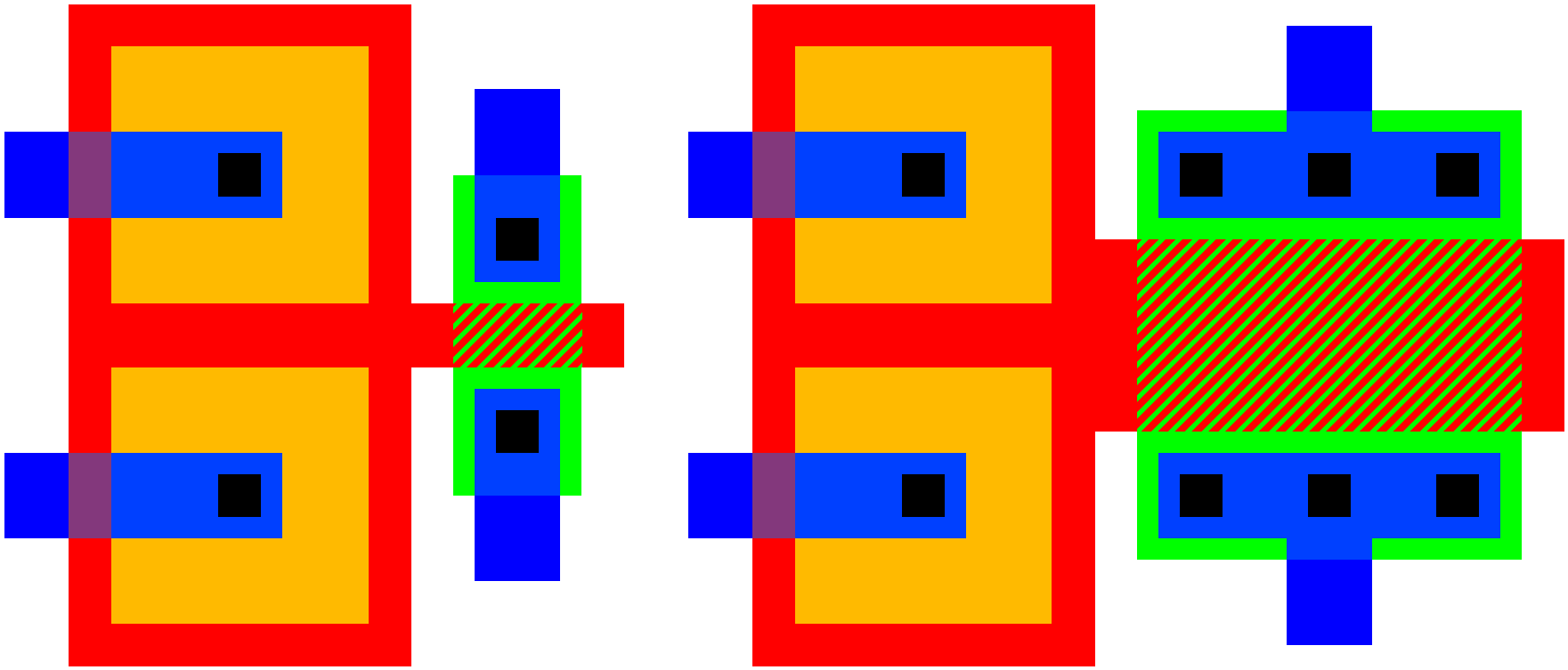


- Be careful about routing metal lines over top of your floating gates. The voltages on such lines couple into the floating gate just like the control-gate voltages.
- Moreover, if you are trying to carefuly match C_T for two FGMOS transistors, then you have to count the stray capacitance between these lines and the floating-gate too...

Which FGMOS Transistor Has a Higher Output Resistance?

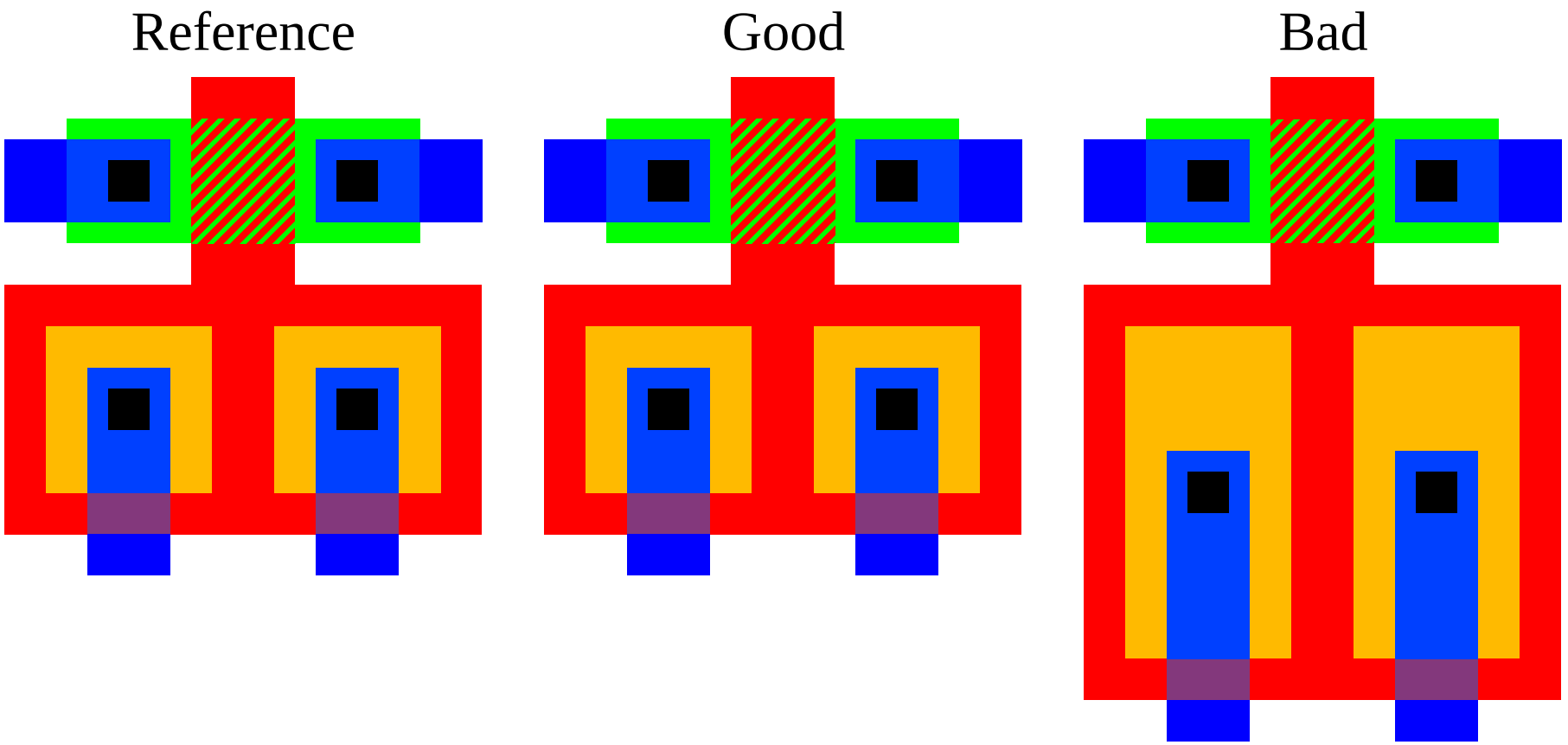


Which FGMOS Transistor Has a Higher Output Resistance?



- The transistor on the *left*...
- For a FGMOS transistor, the Early effect (i.e., channel-length modulation) is always negligible compared to the effect of V_D coupling through C_{gd} to the floating gate. Increasing L does *not* increase r_o.
- $C_{gd} \propto W$, so making the transistor wider *decreases* r_o.

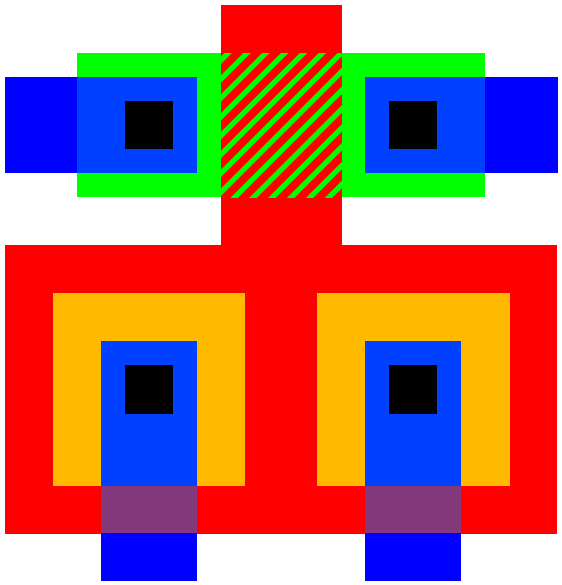
Matching: Same Size & Shape



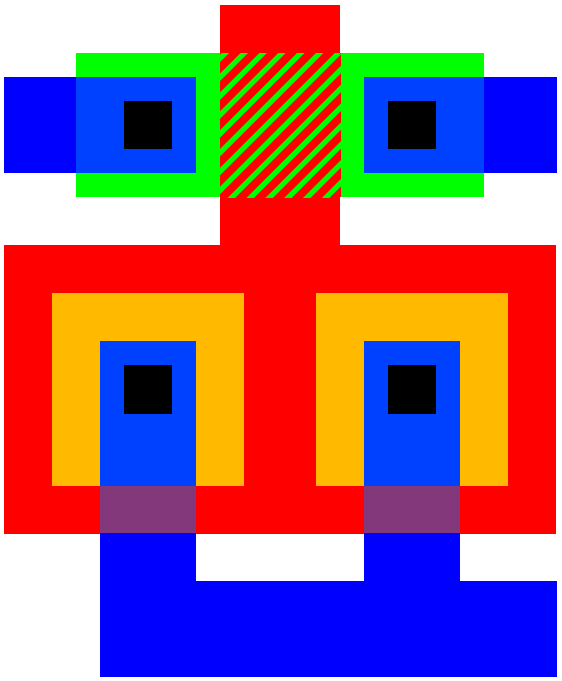
- To obtain matched capacitive-divider ratios in different FGMOS transistors, use floating gates with identical geometries.
- Don't forget that C_T includes parasitics that you won't be able to predict properly at design time.

Matching: Parallel Unit-Sized Control Gates

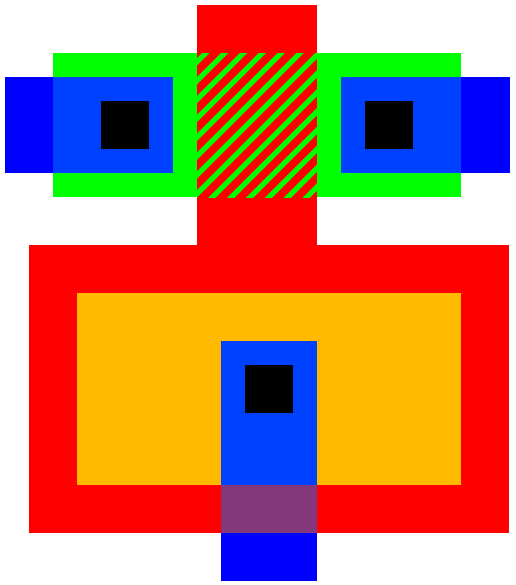
Refernce



Good

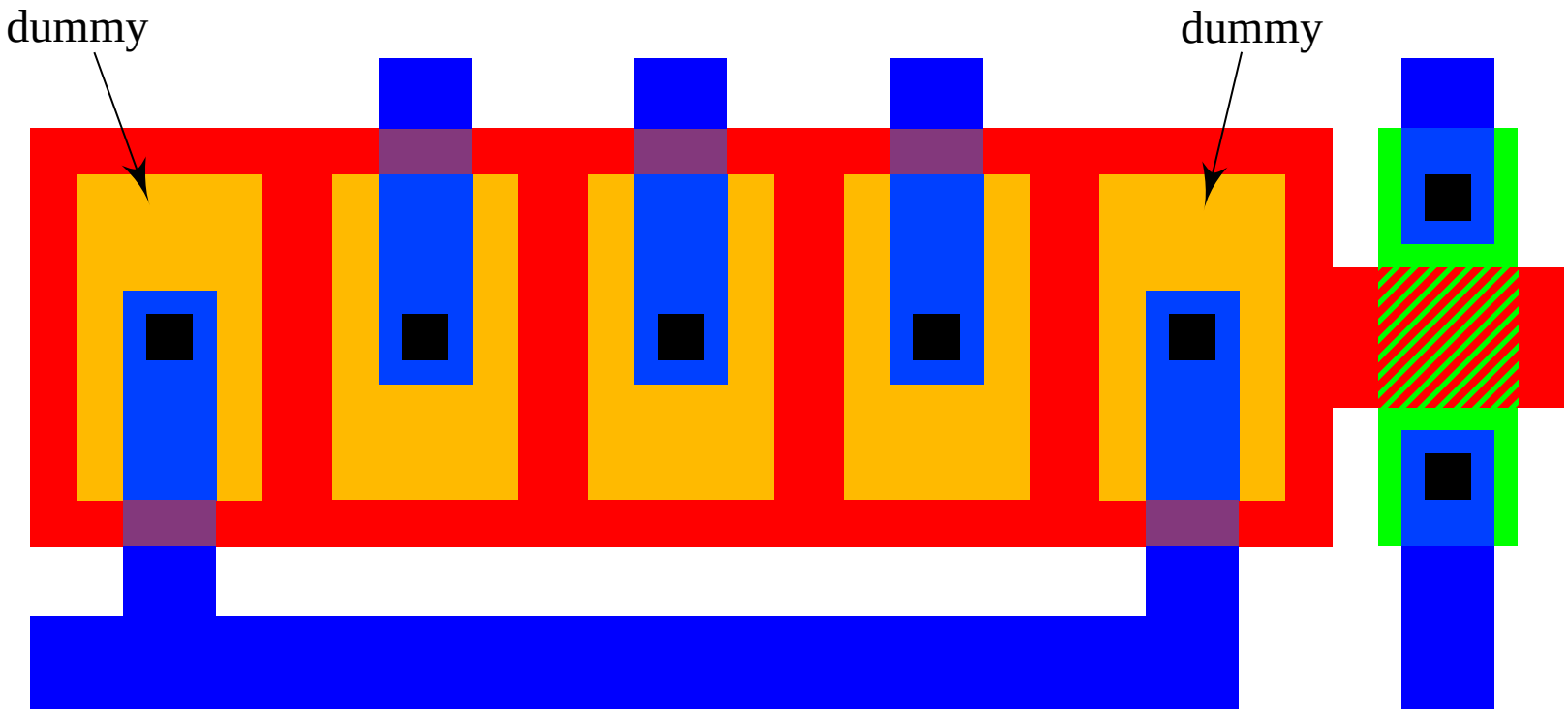


Bad



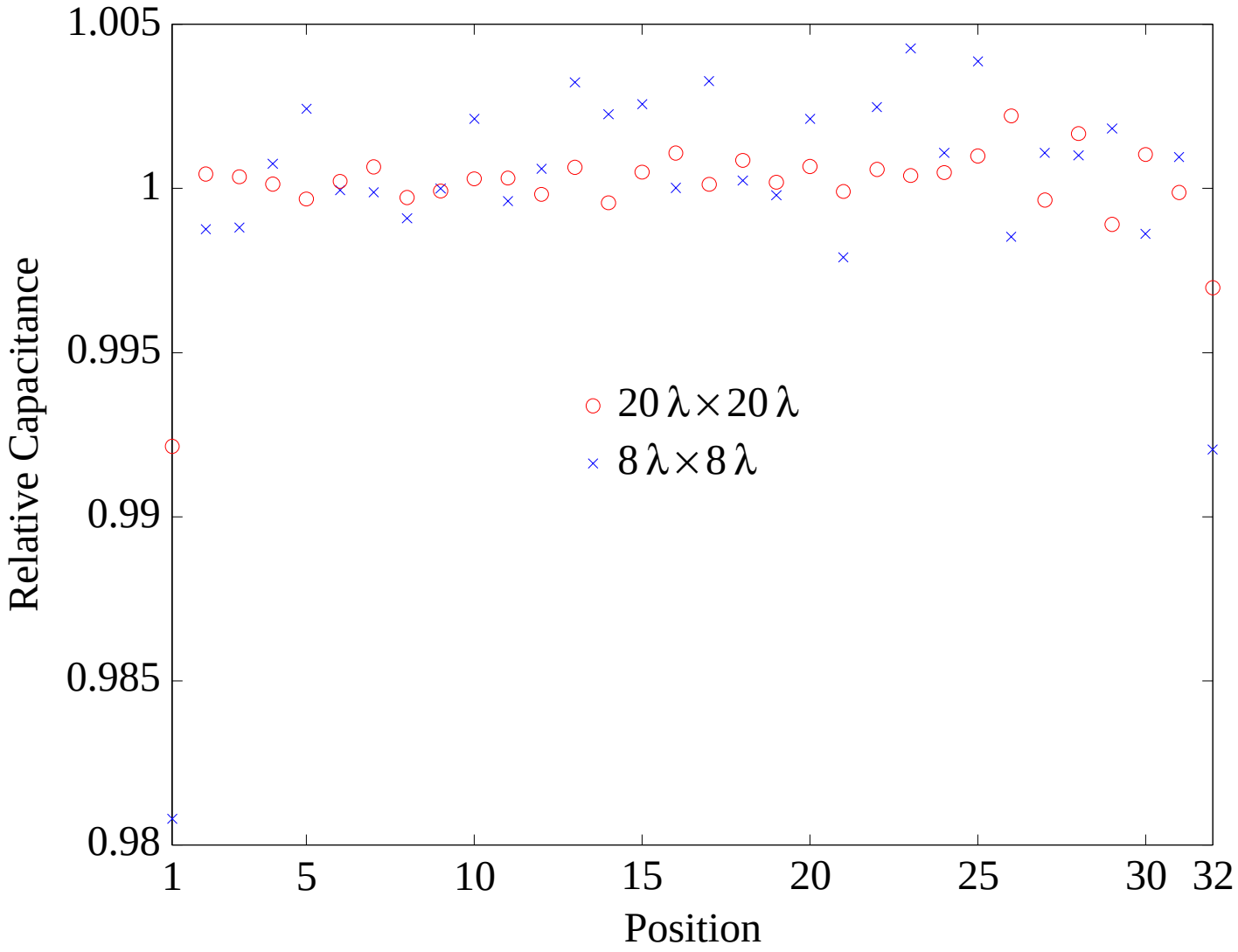
- To obtain accurate control-gate capacitor ratios (e.g., 2:1), connect unit-sized control gates in parallel rather than making composite control gates with the correct area ratios.
- If you are trying to carefuly match C_T, don't connect the unit-sized control gates on top of the floating gate.

Matching: Same Surround

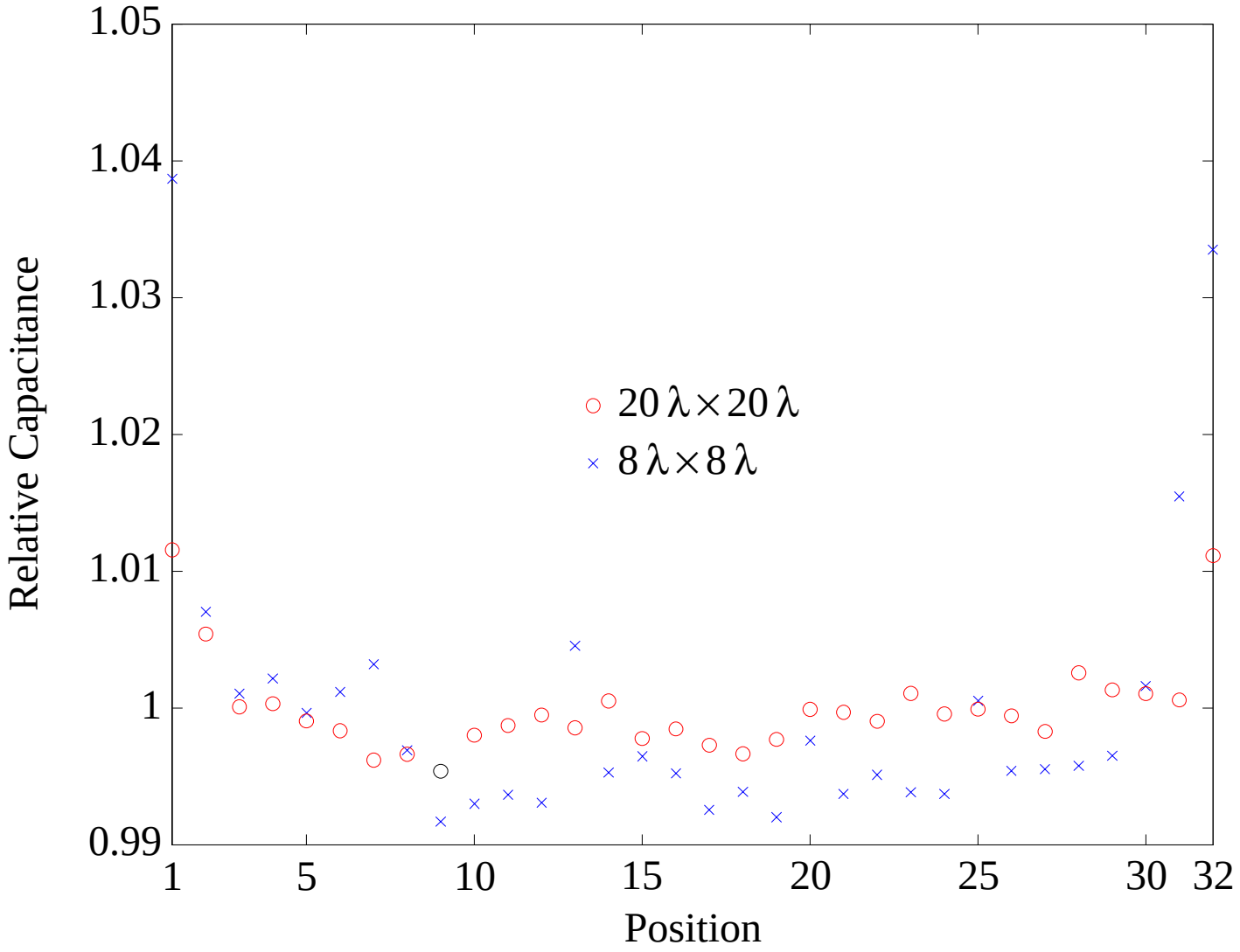


- To improve control-gate matching, use “dummy” control gates at each end to make each “real” control gate have an identical surround.
- Systematic edge effects are ubiquitous, but the underlying mechanisms are not always clear (e.g., fringing fields, non-uniform etching rates).

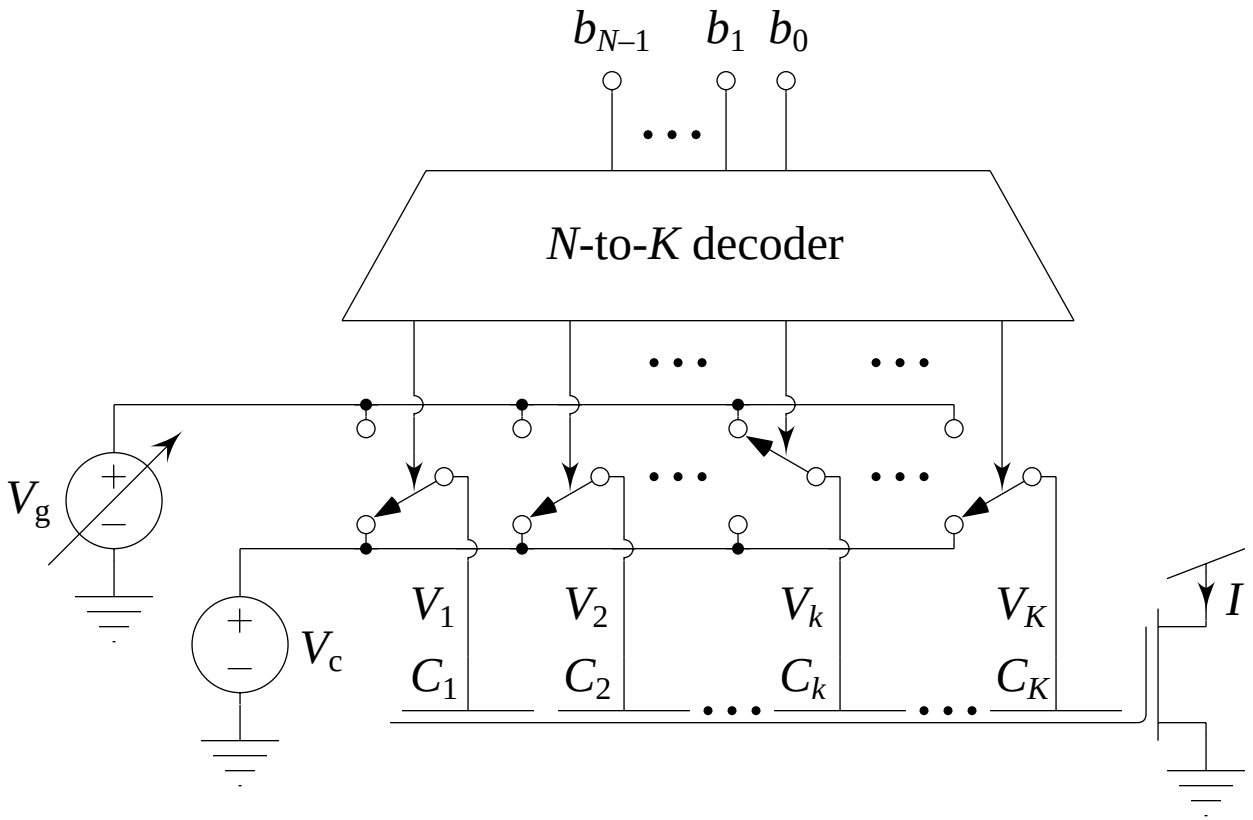
Relative Capacitance vs Position (1.2–μm Process)



Relative Capacitance vs Position (.35–μm Process)



Experimental Method for Measuring Capacitor Matching



- In subthreshold,

$$I \propto e^{\kappa C_i V_i / C_T U_T} \Rightarrow \frac{\partial \log I}{\partial V_i} = \frac{\kappa C_i}{C_T U_T} \propto C_i$$

$\Rightarrow$ Mismatch in the slope of log I vs V_i directly reflects mismatch in C_i.