Complementary Metal-Oxide-Semiconductor Very Large-Scale Integrated Circuit Design

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Simplified Periodic Table of the Elements

I							VIII
H 1 Hydrogen	II	III	IV	V	VI	VII	He 2 Helium
Li 3 Lithium	Be 4 Beryllium	B 5 Boron	C 6 Carbon	N 7 Nitrogen	O 8 Oxygen	F 9 Flourine	Ne 10 Neon
Na 11 Sodium	Mg 12 Magnesium	Al 13 Aluminum	Si 14 Silicon	P 15 Phosphorus	S 16 Sulfur	Cl 17 Chlorine	Ar 18 Argon
K 19 Potassium	Ca 20 Calcium	Ga 31 Gallium	Ge 32 Germanium	As 33 Arsenic	Se 34 Selenium	Br 35 Bromine	Kr 36 Krypton
Rb 37 Rubidium	Sr 38 Strontium	In 49 Indium	Sn 50 Tin	Sb 51 Antimony	Te 52 Tellurium	I 53 Iodine	Xe 54 Xenon
Cs 55 Cesium	Ba 56 Barium	Tl 81 Thallium	Pb 82 Lead	Bl 83 Bismuth	Po 84 Polonium	At 85 Astatine	Rn 86 Radon

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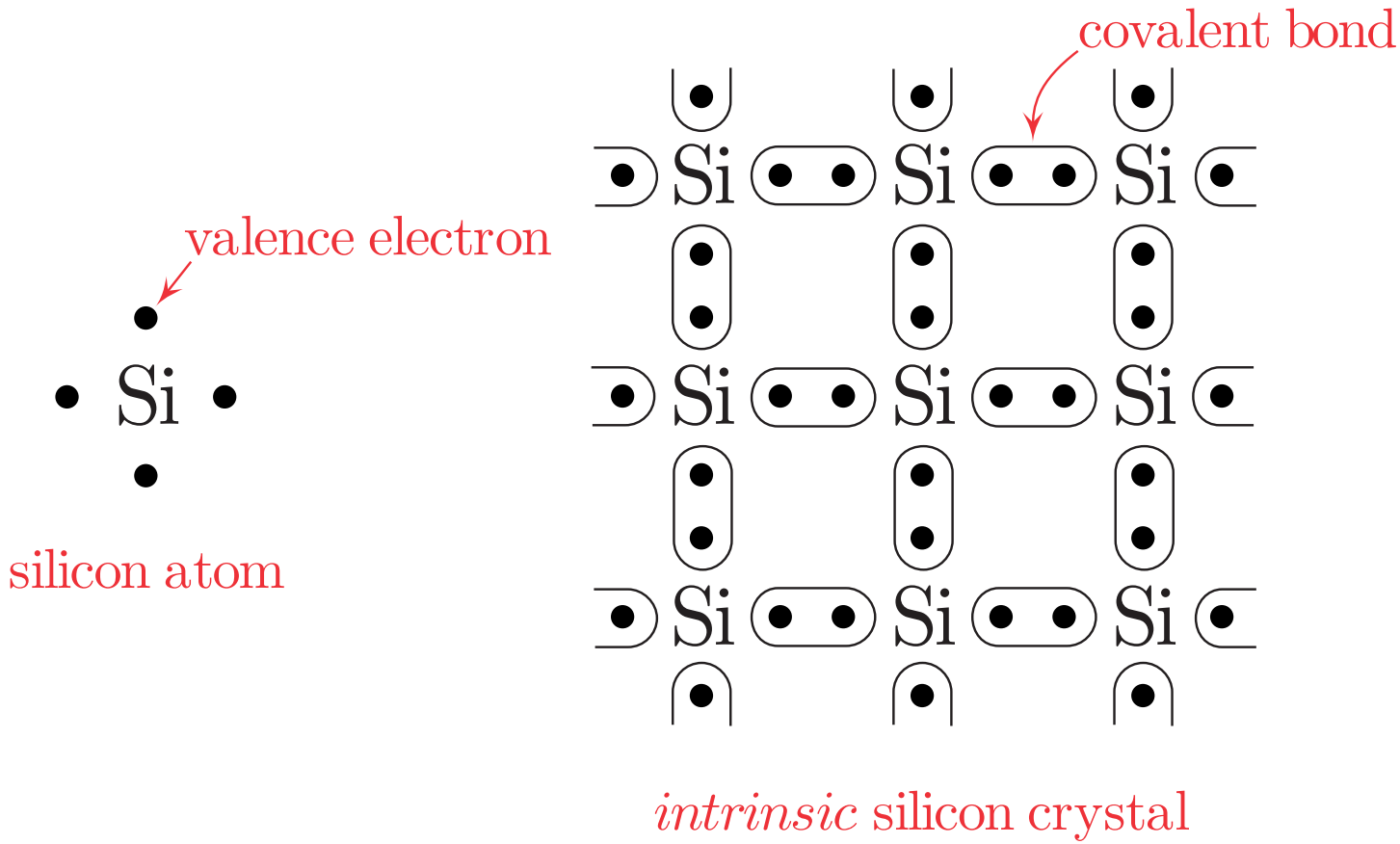
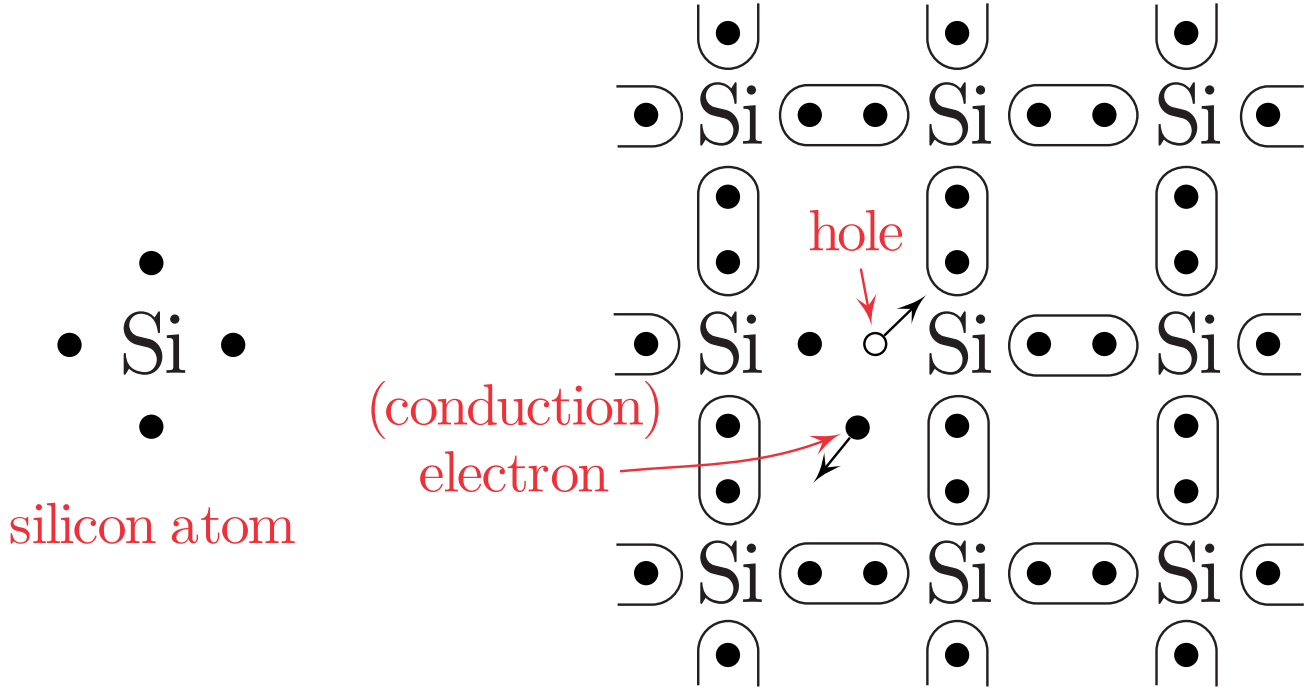
Schematic Representation of a Silicon Crystal

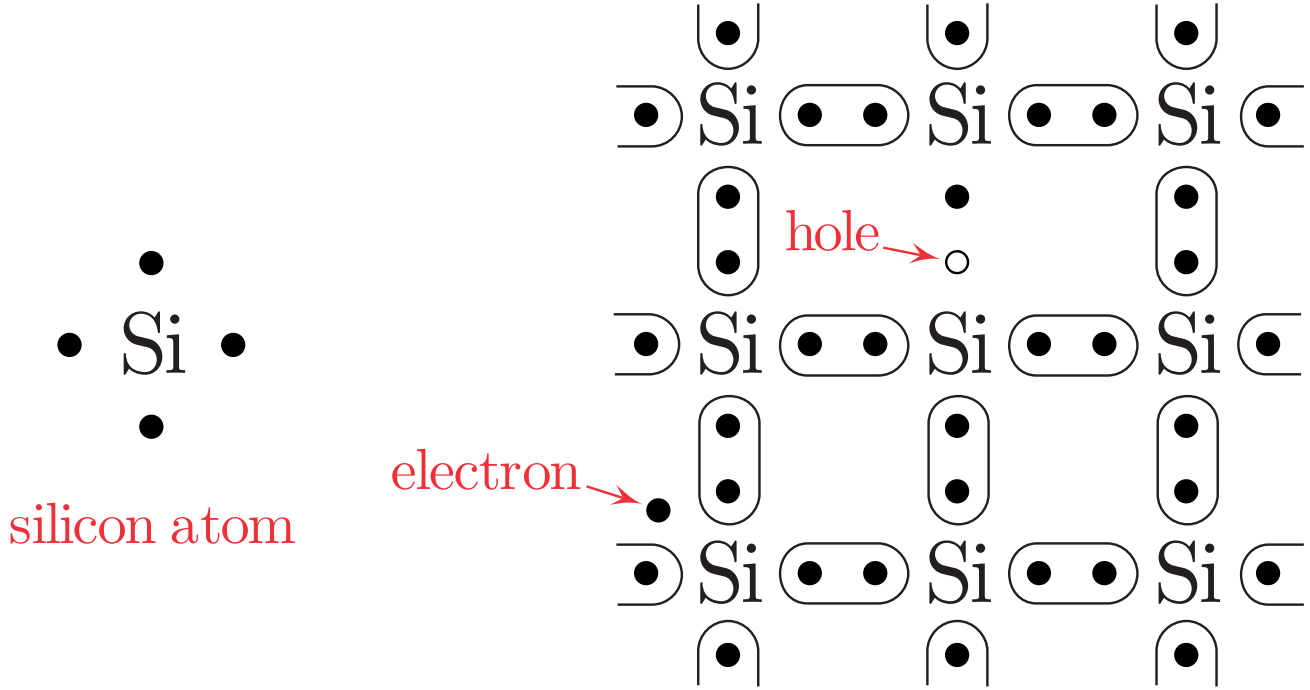


Electrons and Holes in the Silicon Crystal



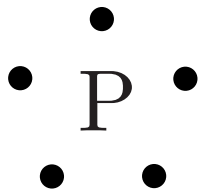
intrinsic silicon crystal

Electrons and Holes in the Silicon Crystal

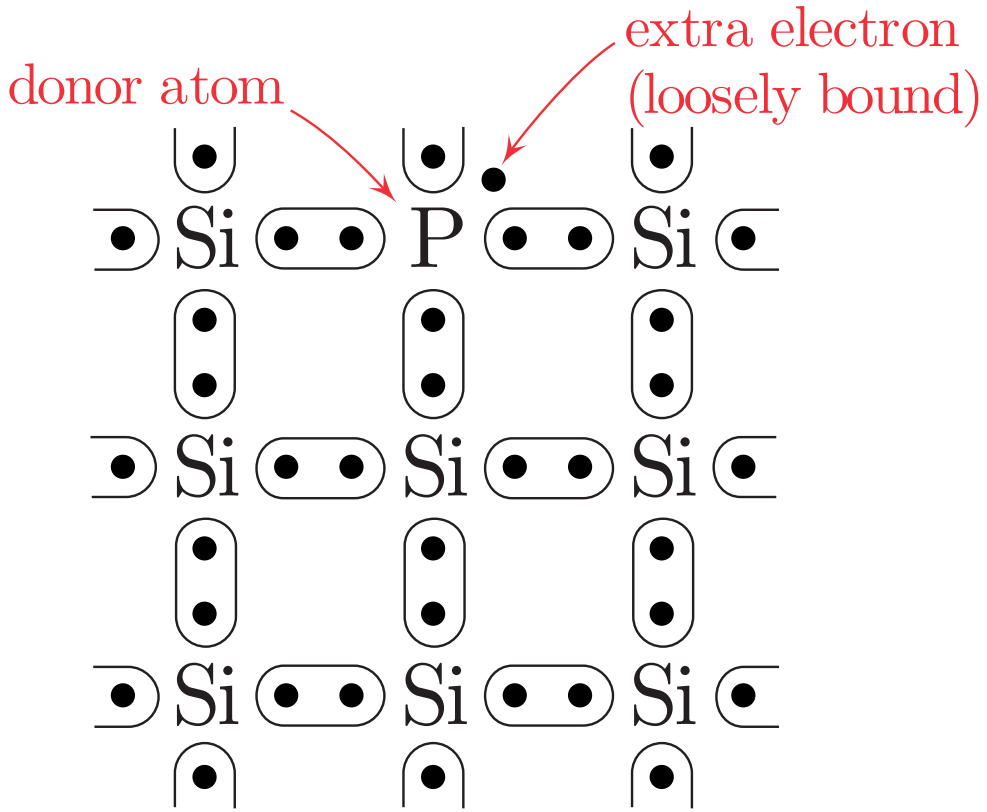


intrinsic silicon crystal

Silicon Crystal Doped with Donor Impurities

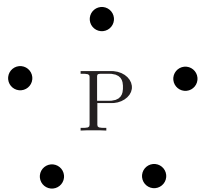


phosphorus atom
(*donor* for silicon)



doped silicon crystal: *n*-type

Silicon Crystal Doped with Donor Impurities



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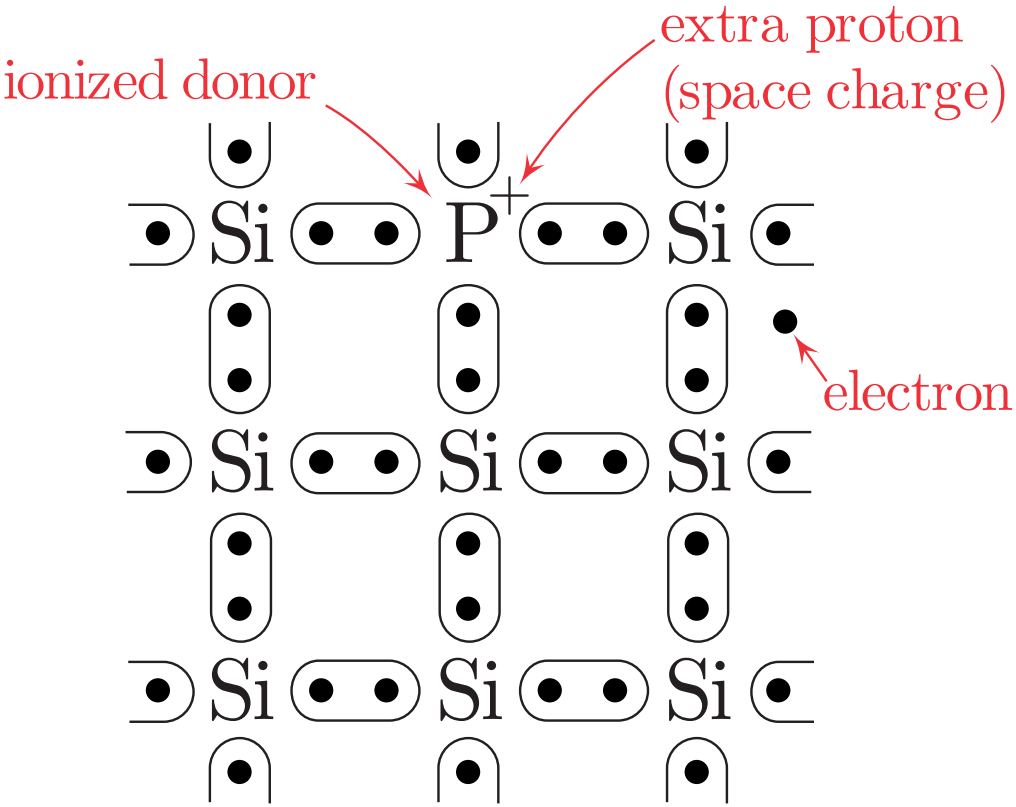
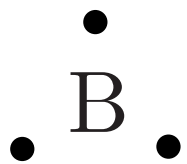
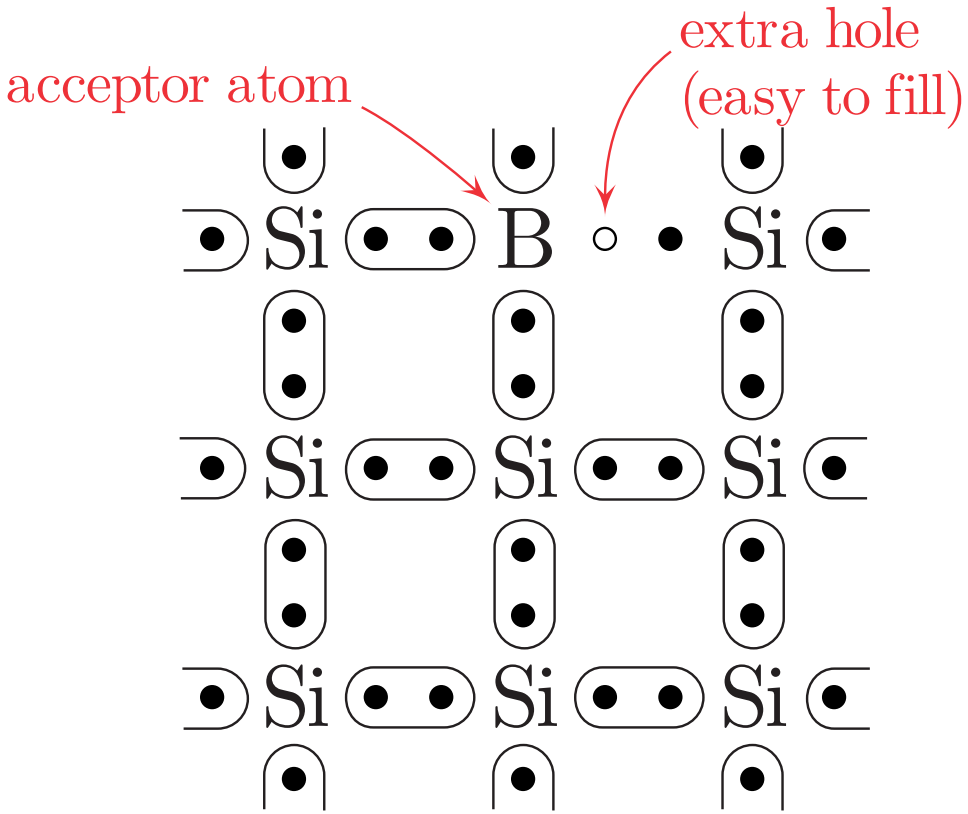


doped silicon crystal: *n*-type

Silicon Crystal Doped with Acceptor Impurities

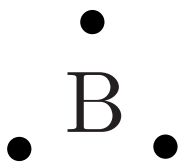


boron atom
(*acceptor* for silicon)

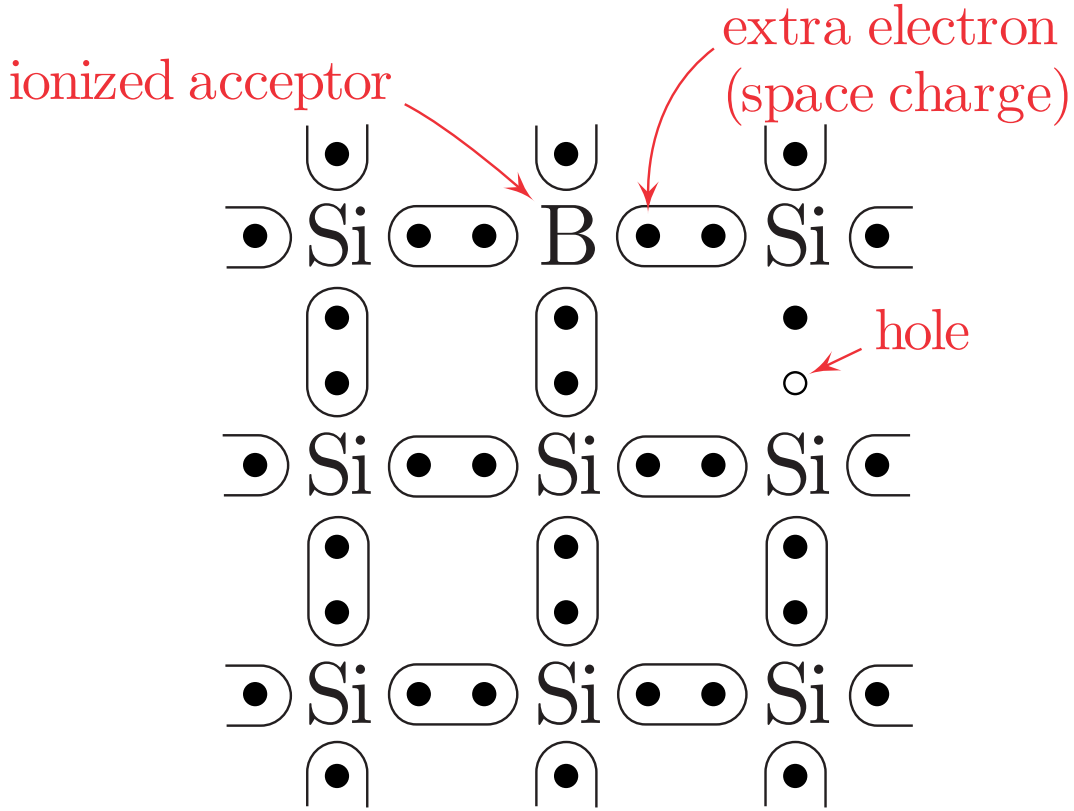


doped silicon crystal: *p*-type

Silicon Crystal Doped with Acceptor Impurities

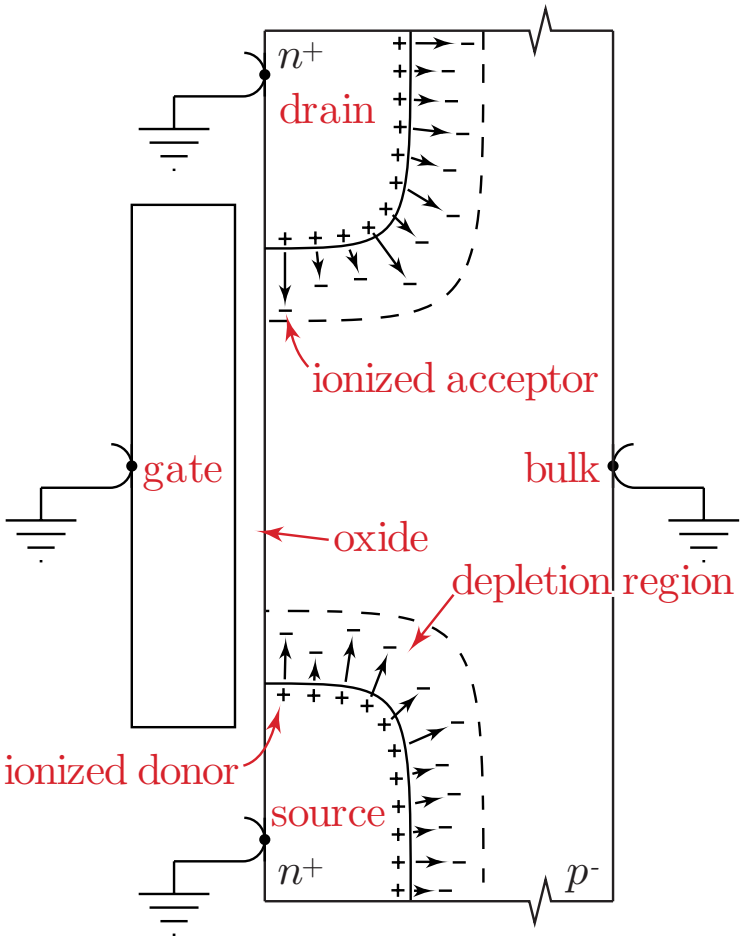


boron atom
(*acceptor* for silicon)

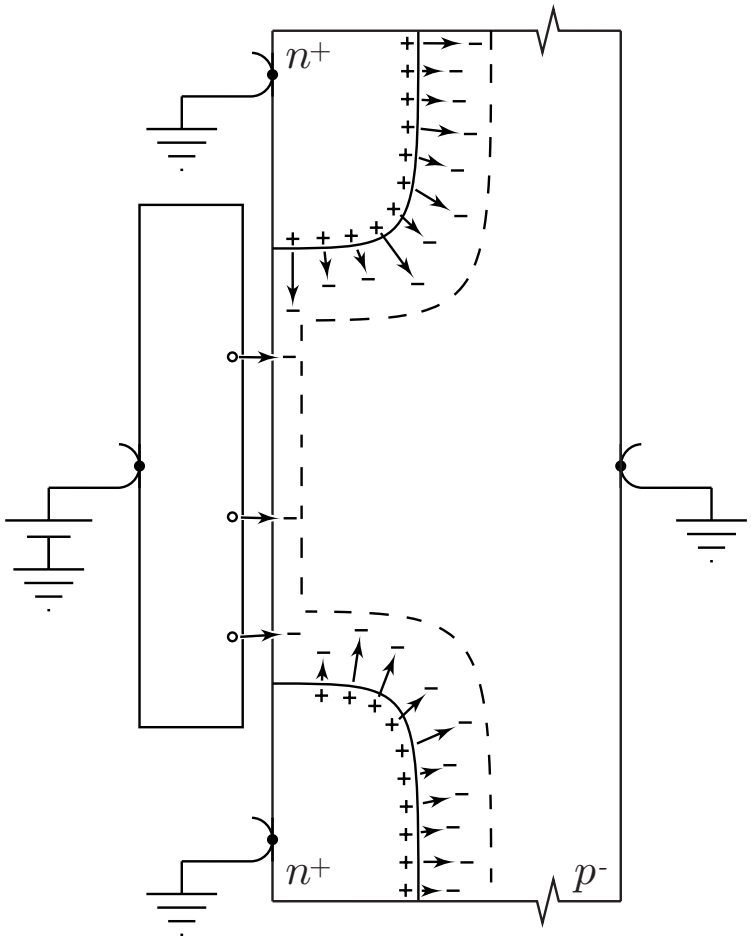


doped silicon crystal: *p*-type

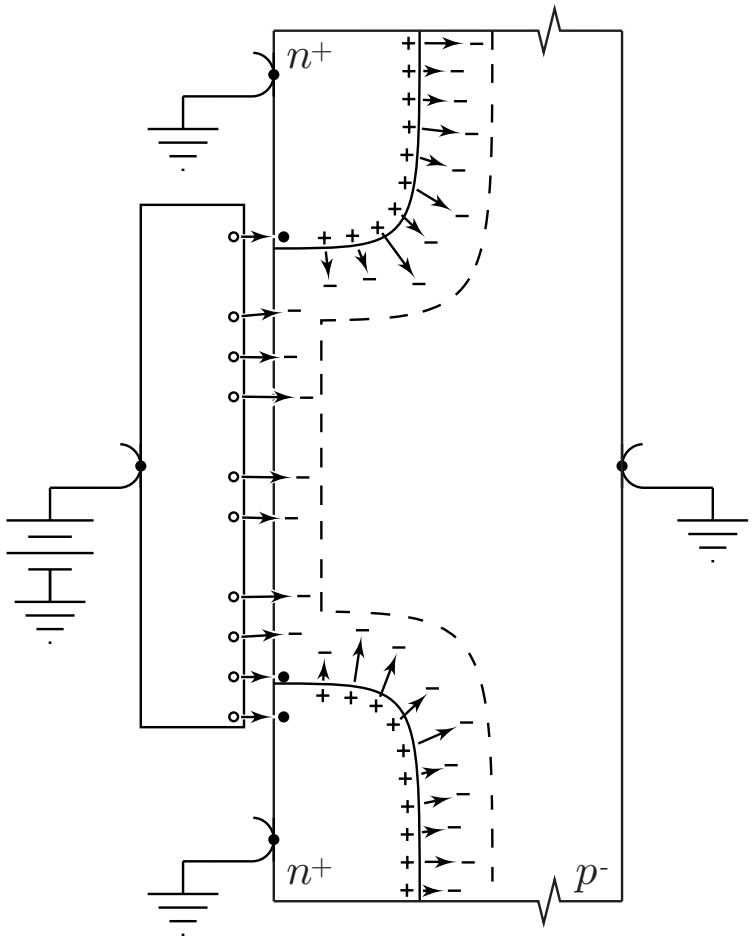
N-Channel Metal-Oxide-Semiconductor Transistor



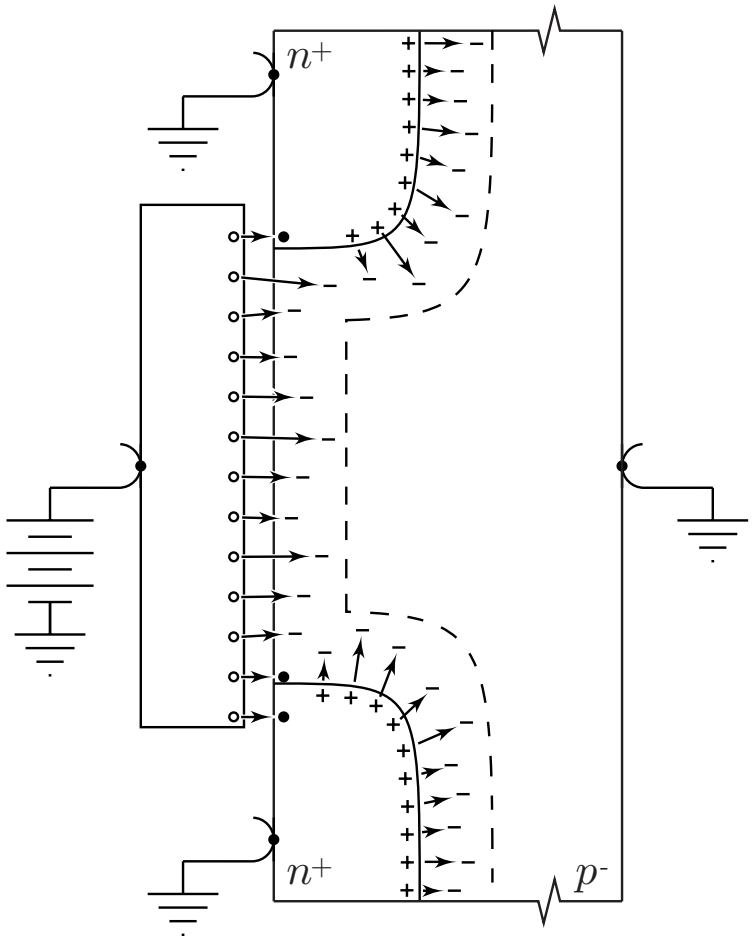
N-Channel Metal-Oxide-Semiconductor Transistor



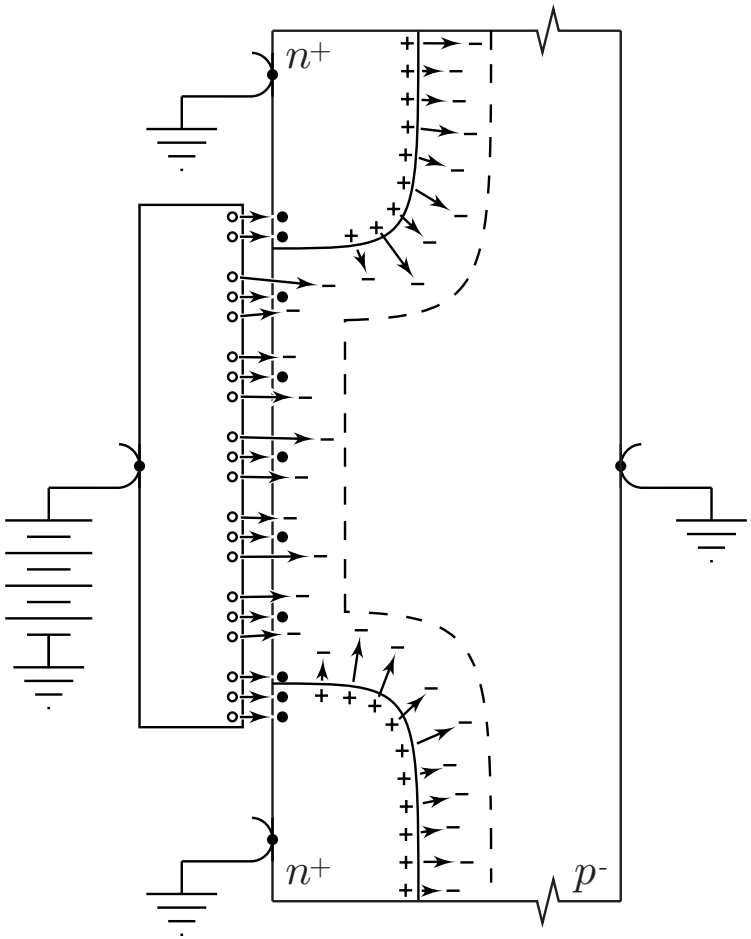
N-Channel Metal-Oxide-Semiconductor Transistor



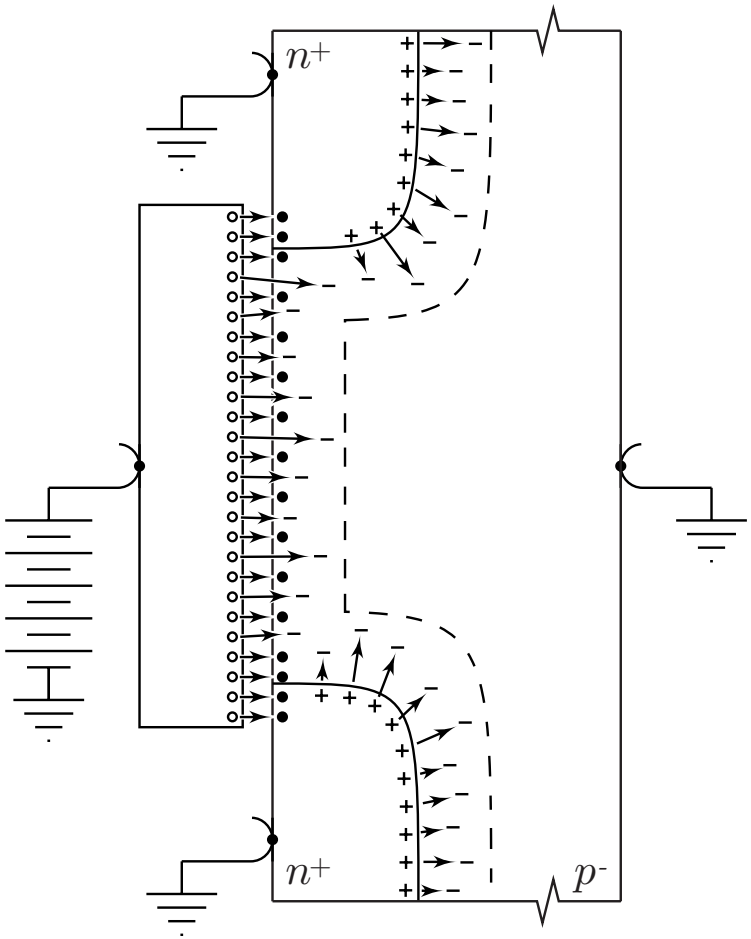
N-Channel Metal-Oxide-Semiconductor Transistor



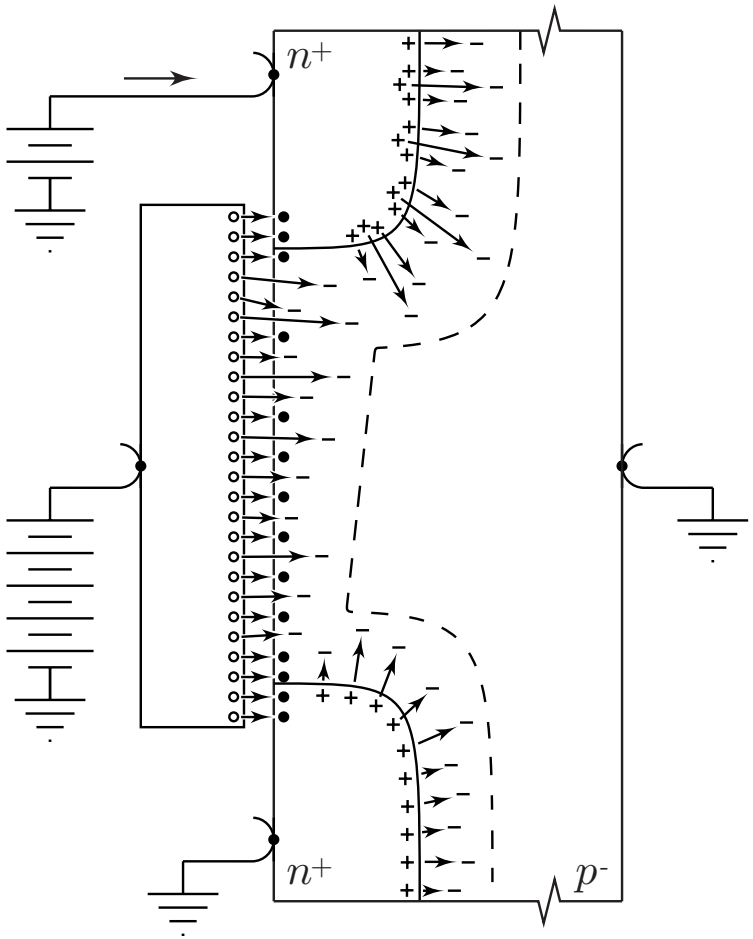
N-Channel Metal-Oxide-Semiconductor Transistor



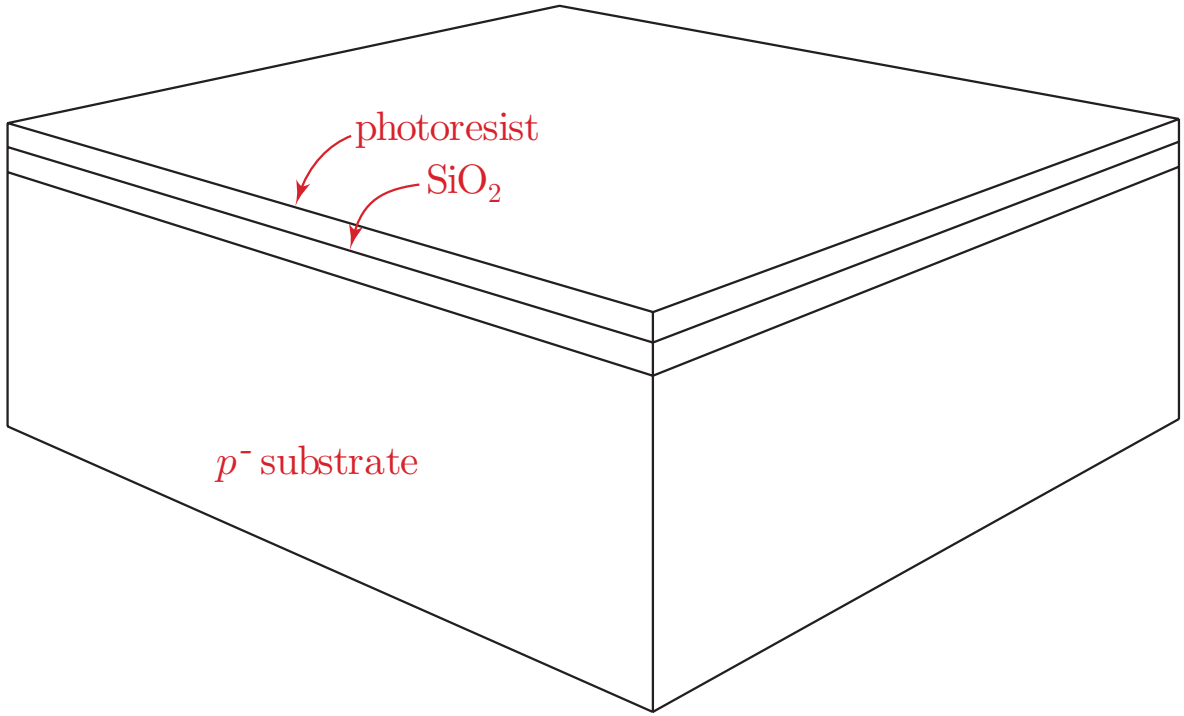
N-Channel Metal-Oxide-Semiconductor Transistor



N-Channel Metal-Oxide-Semiconductor Transistor

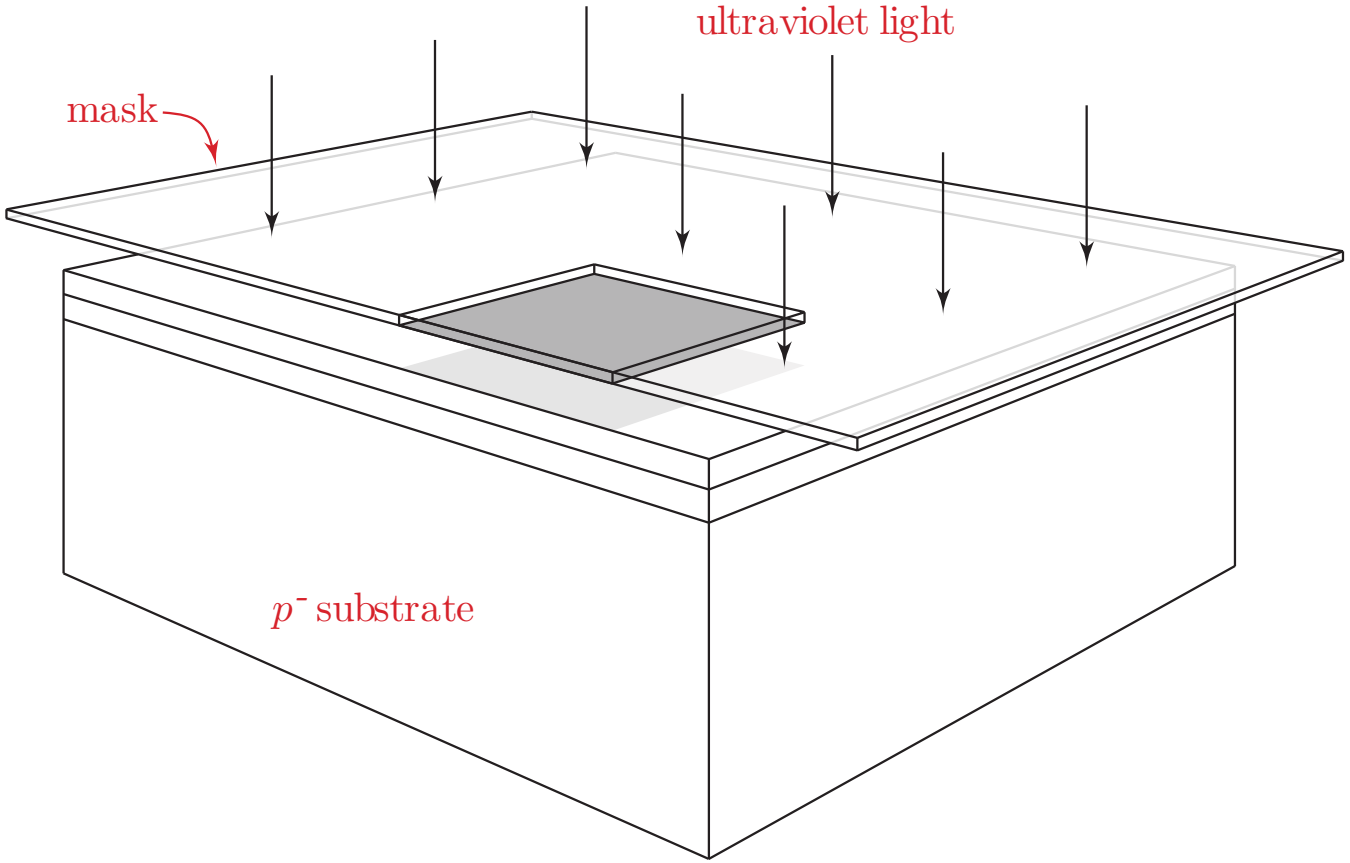


CMOS Fabrication



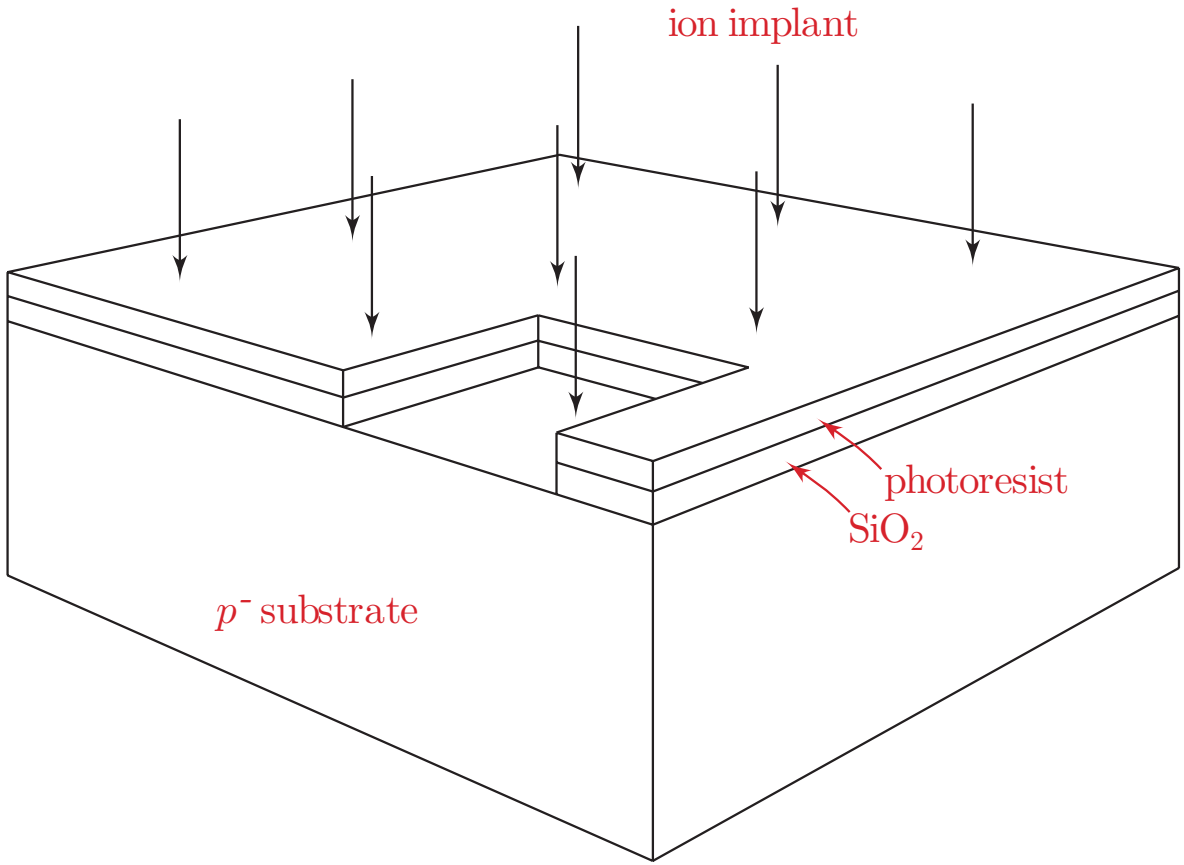
Oxidize silicon surface and coat with photoresist

CMOS Fabrication



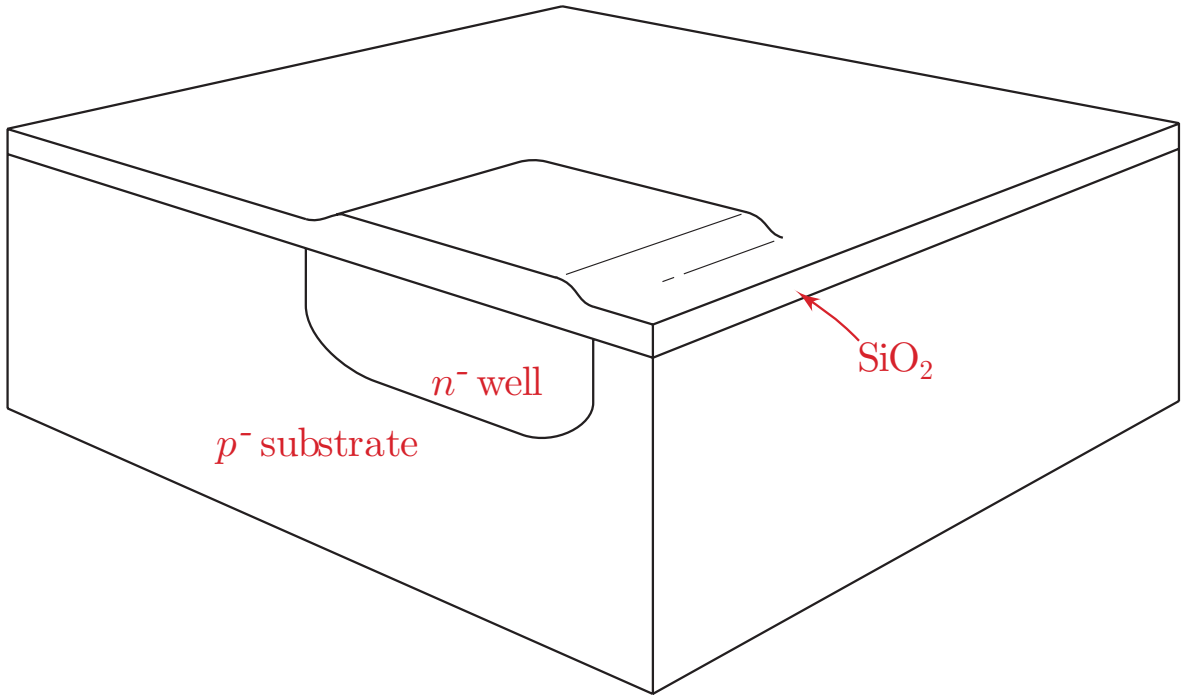
Pattern and selectively etch oxide layer

CMOS Fabrication



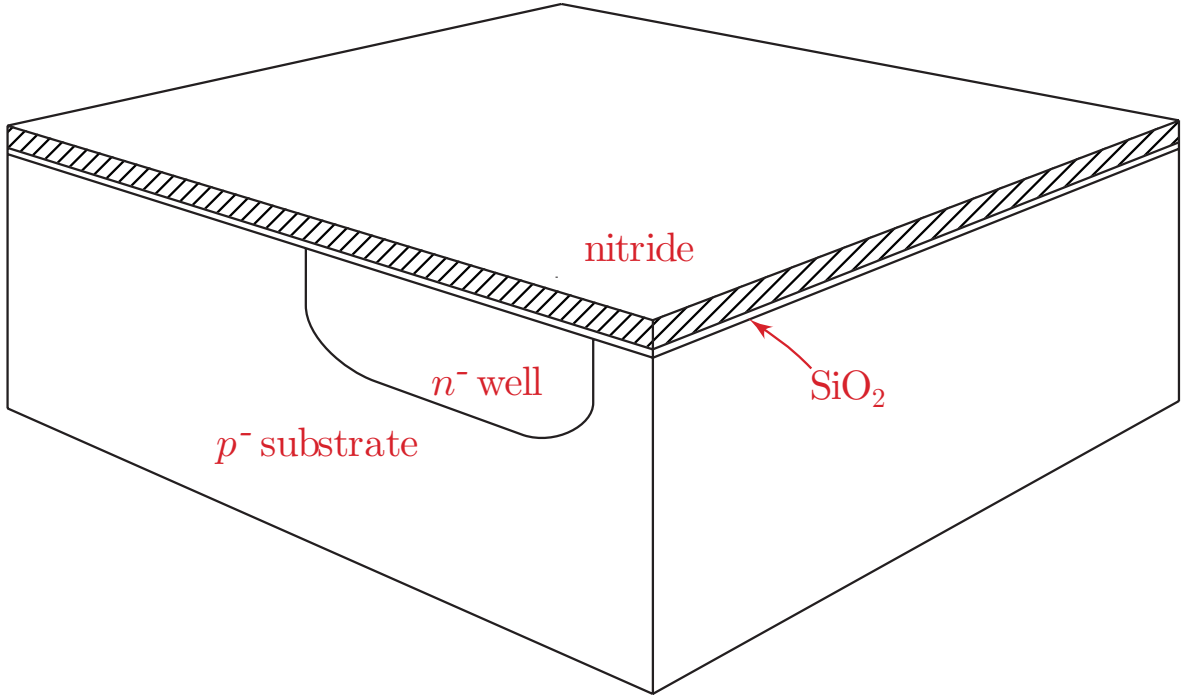
Ion implant for n-well regions

CMOS Fabrication



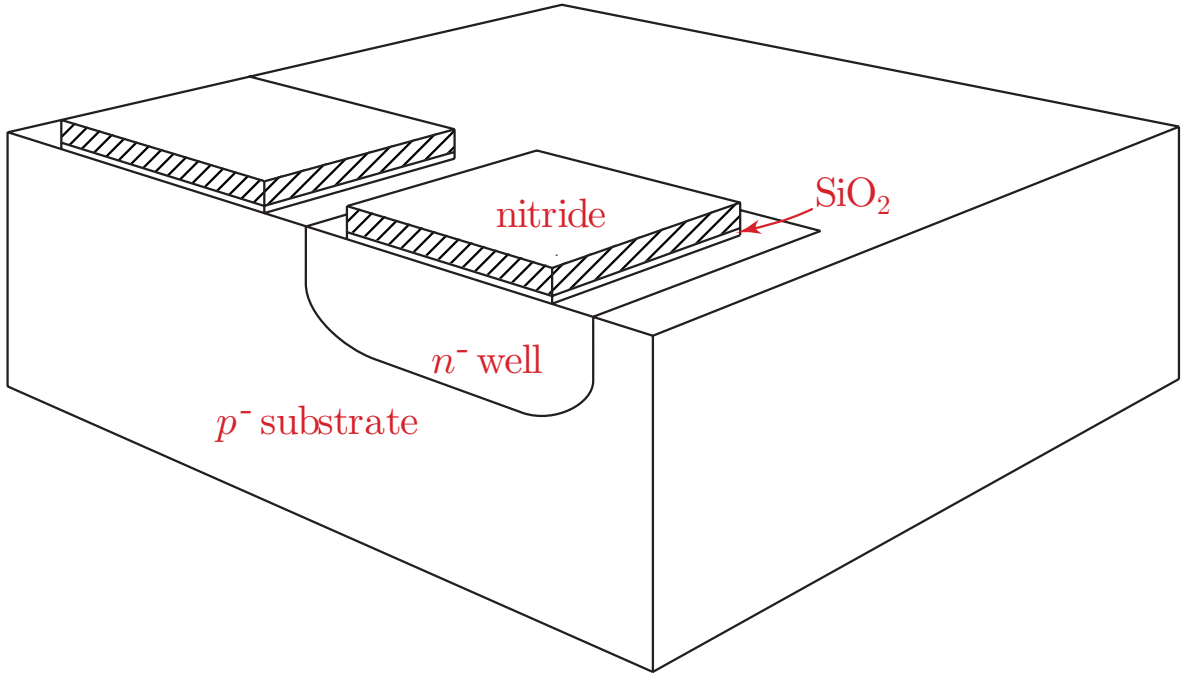
Anneal n-well implant and grow oxide

CMOS Fabrication



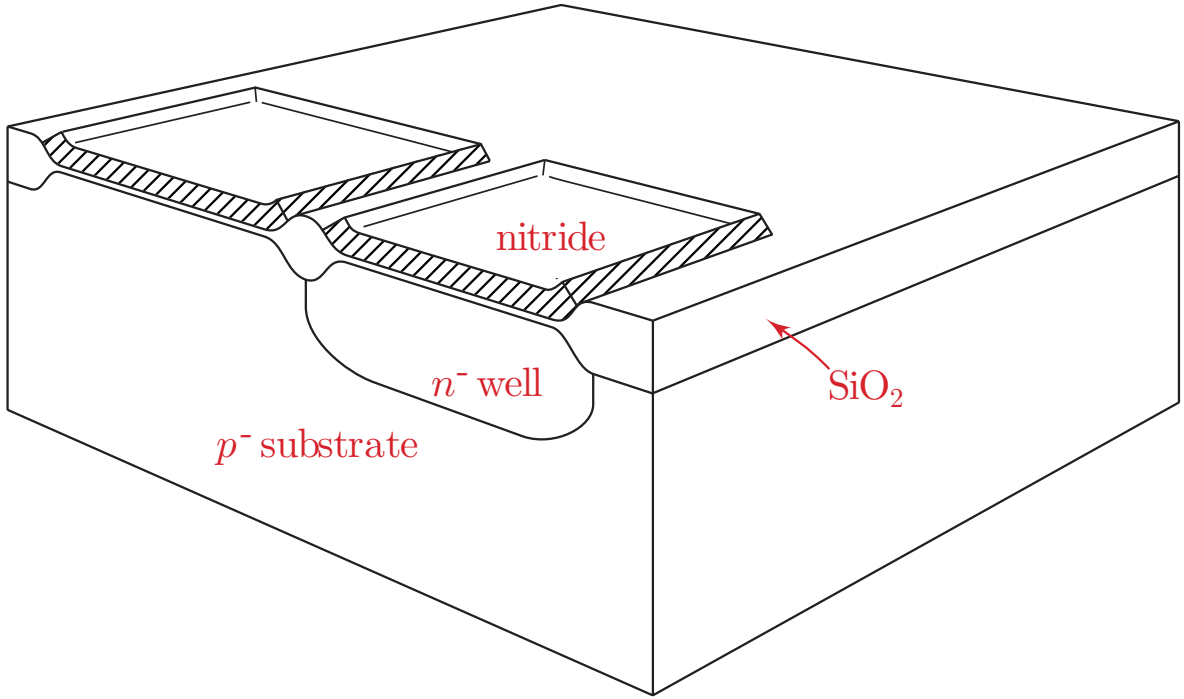
Remove all oxide, regrow thin oxide, and deposit nitride layer

CMOS Fabrication



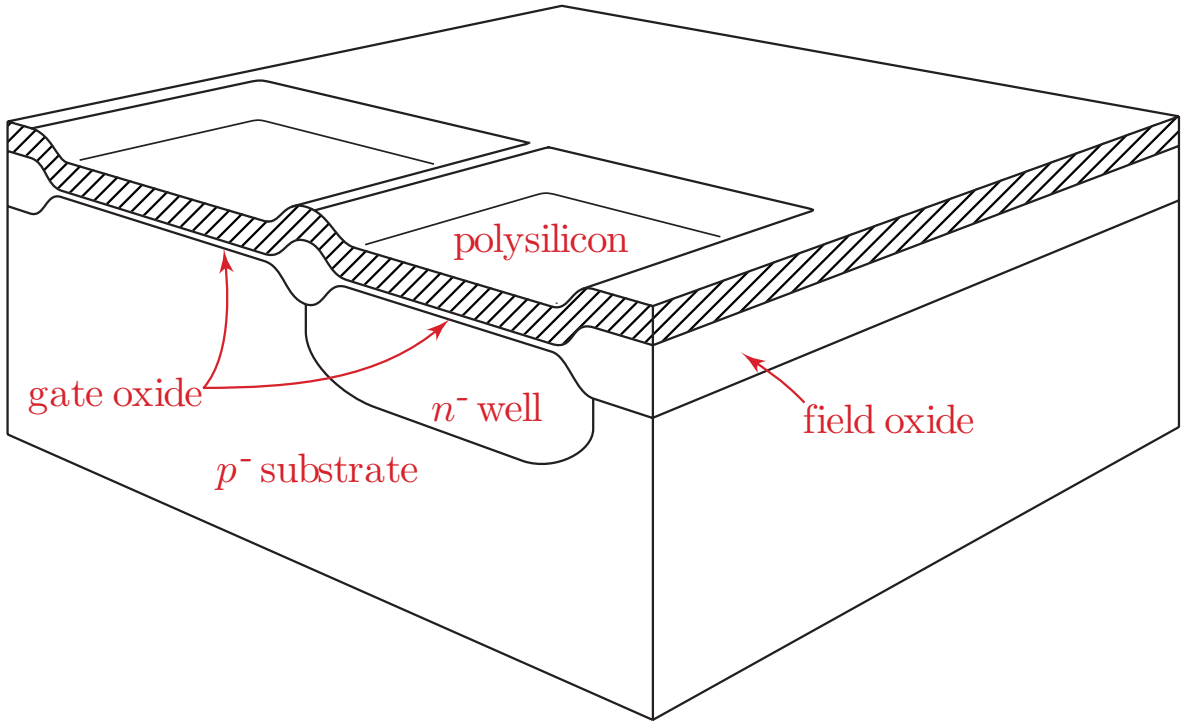
Pattern and selectively etch oxide and nitride layers

CMOS Fabrication



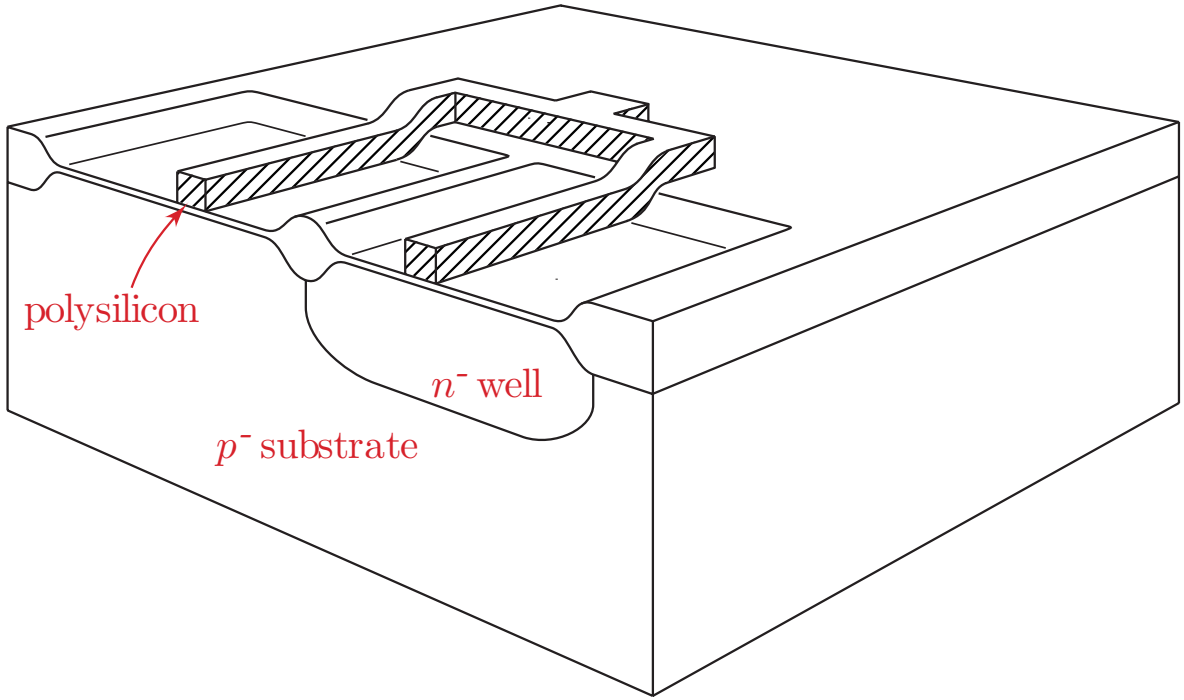
Grow field oxide in areas without nitride

CMOS Fabrication



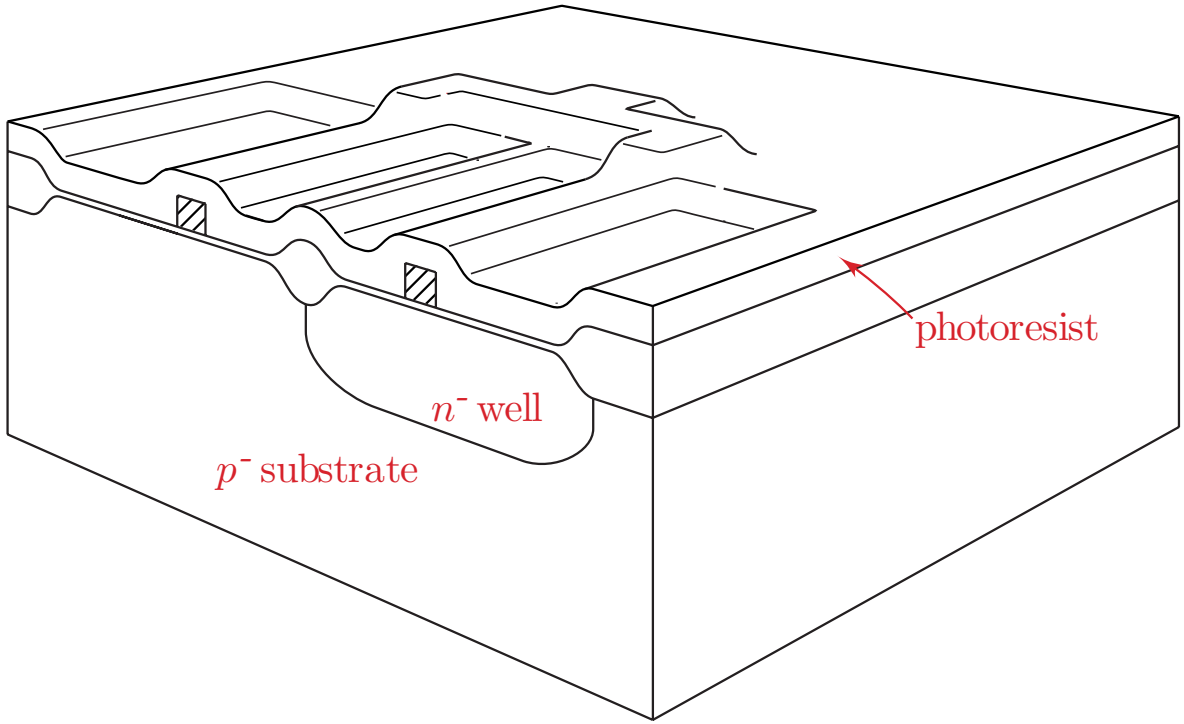
Remove nitride and thin oxide, grow gate oxide, and deposit poly

CMOS Fabrication



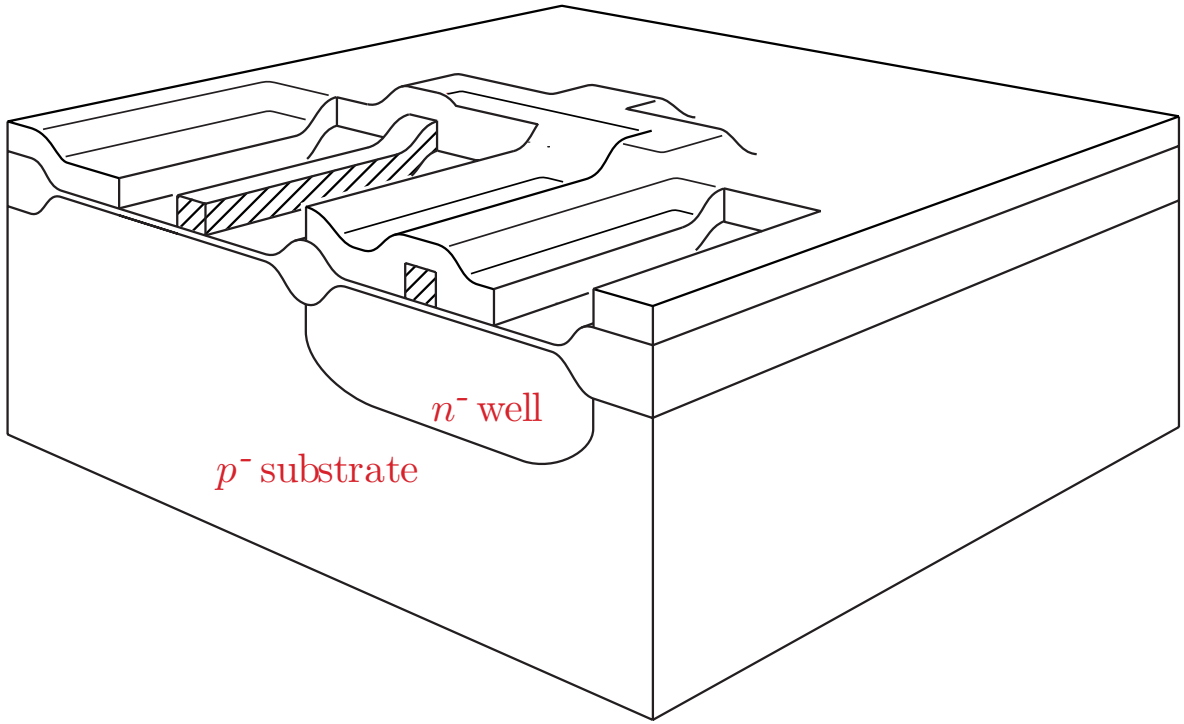
Pattern and selectively etch polysilicon

CMOS Fabrication



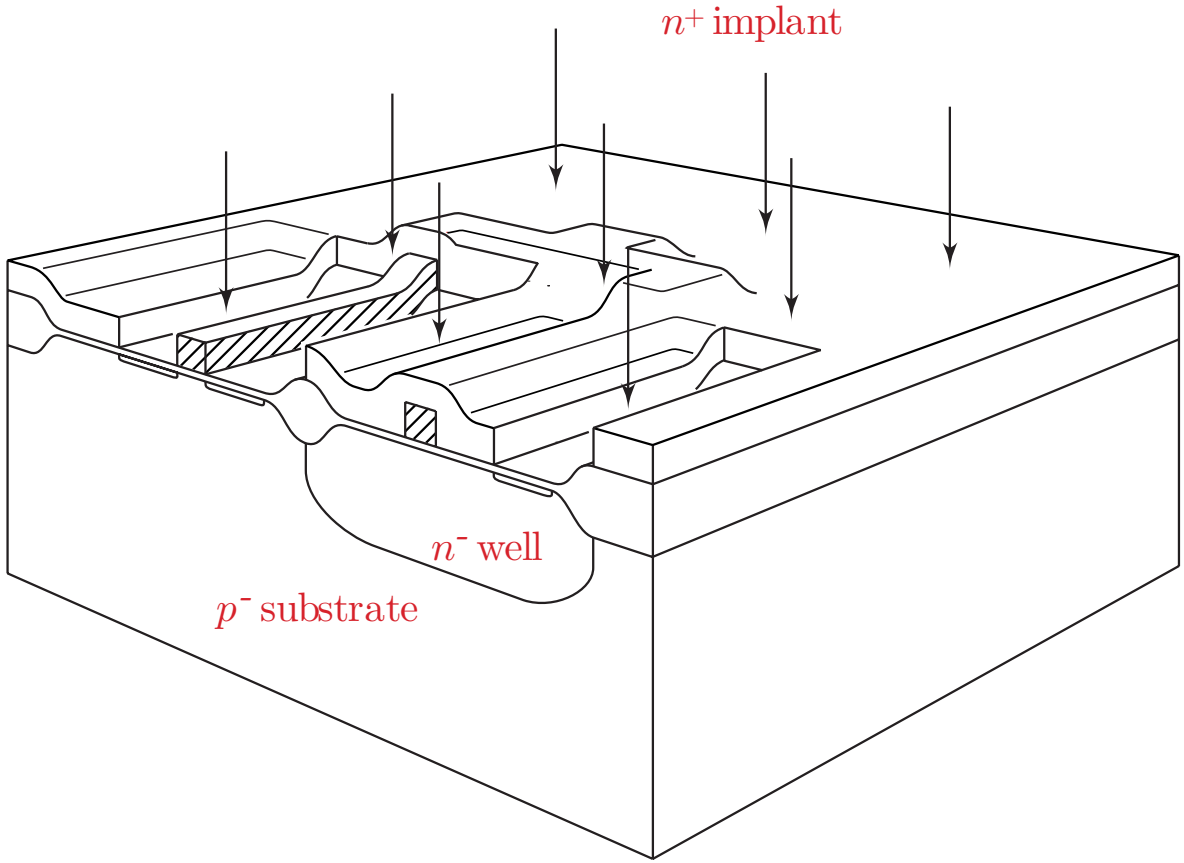
Conformally coat entire surface with photoresist

CMOS Fabrication



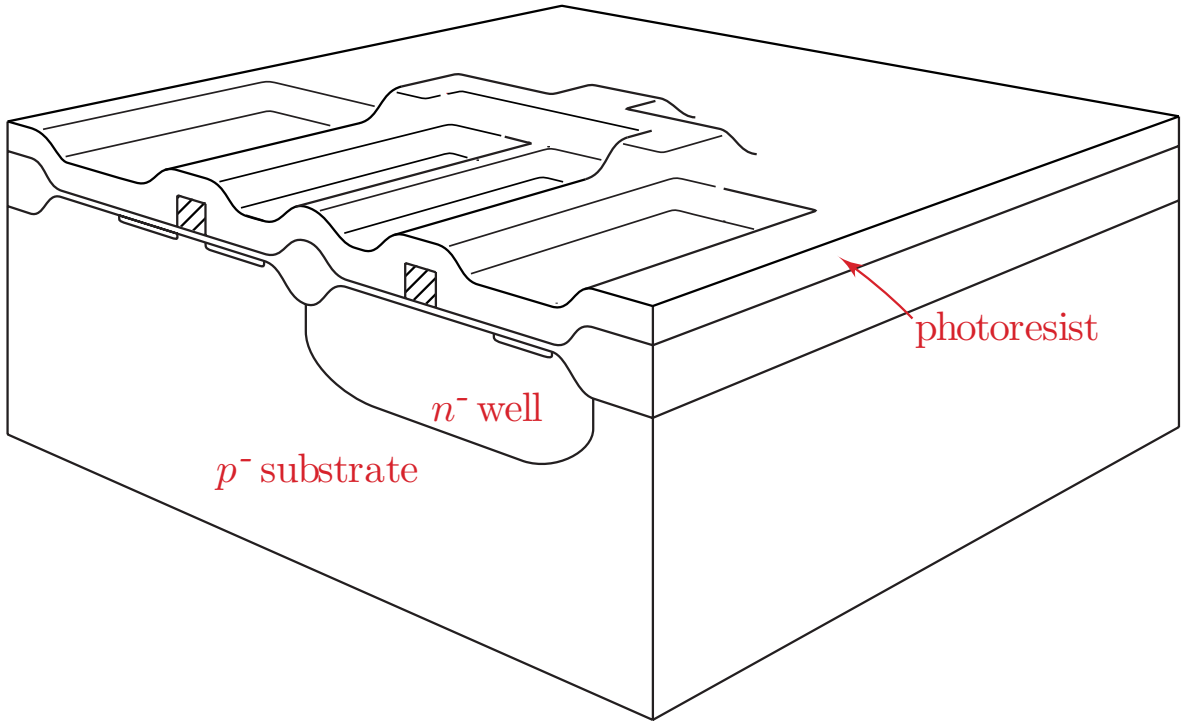
Remove photoresist to expose regions for n^+ implant

CMOS Fabrication



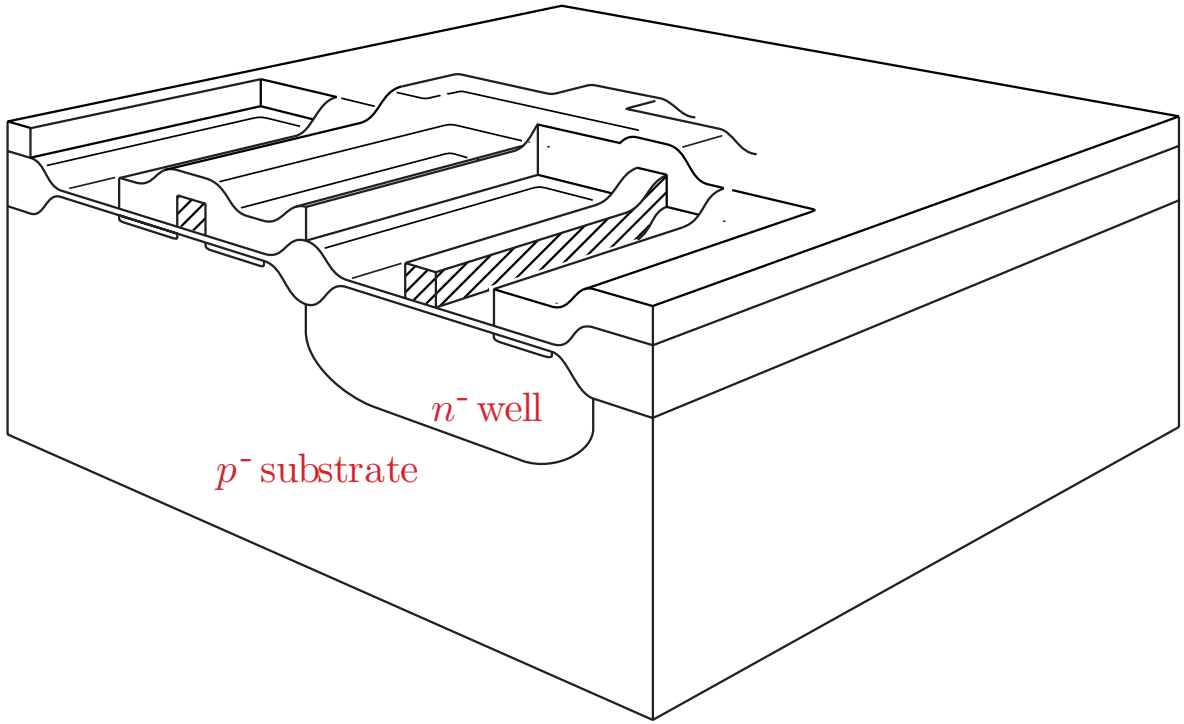
Ion implant for n^+ regions and remove all photoresist

CMOS Fabrication



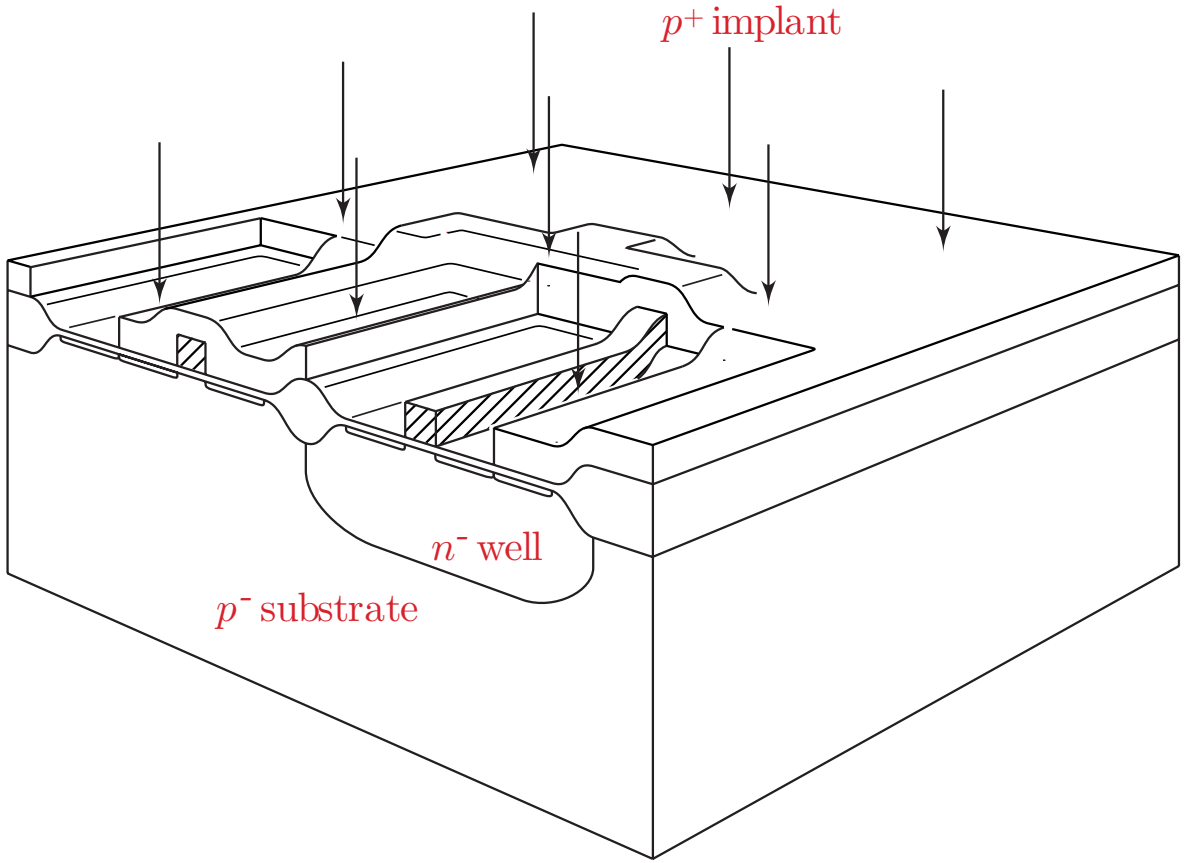
Conformally coat entire surface with photoresist

CMOS Fabrication



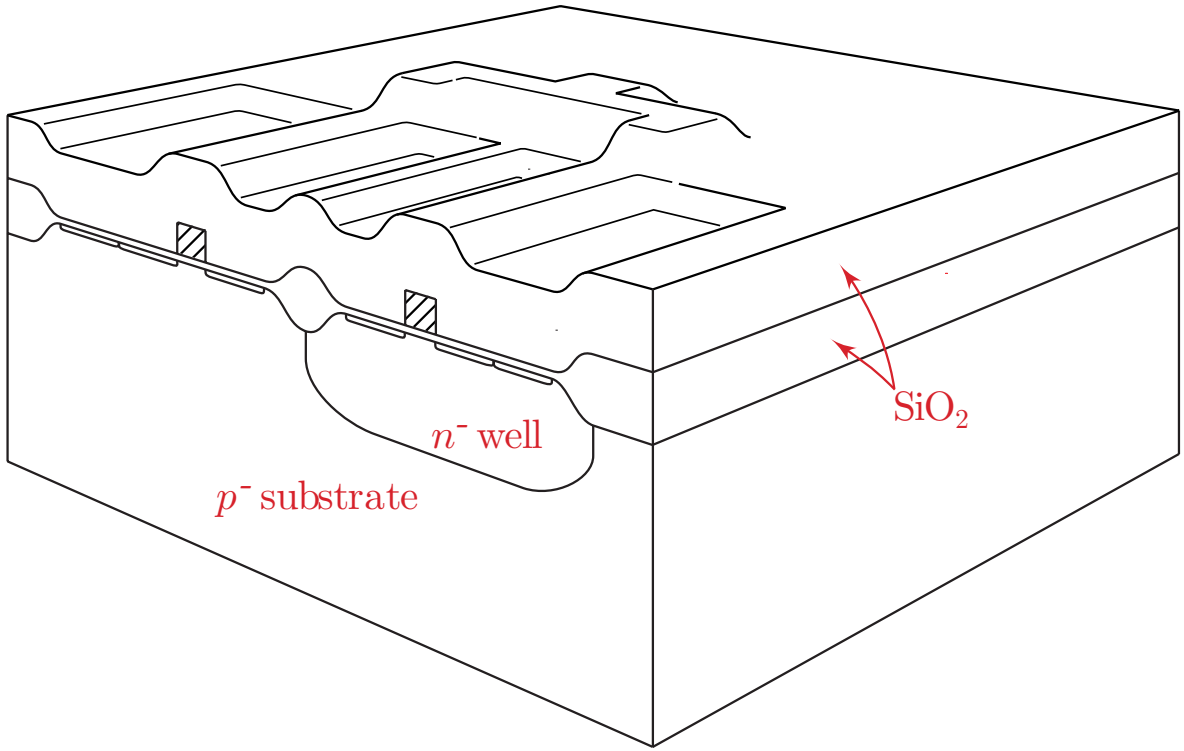
Remove photoresist to expose regions for p^+ implant

CMOS Fabrication



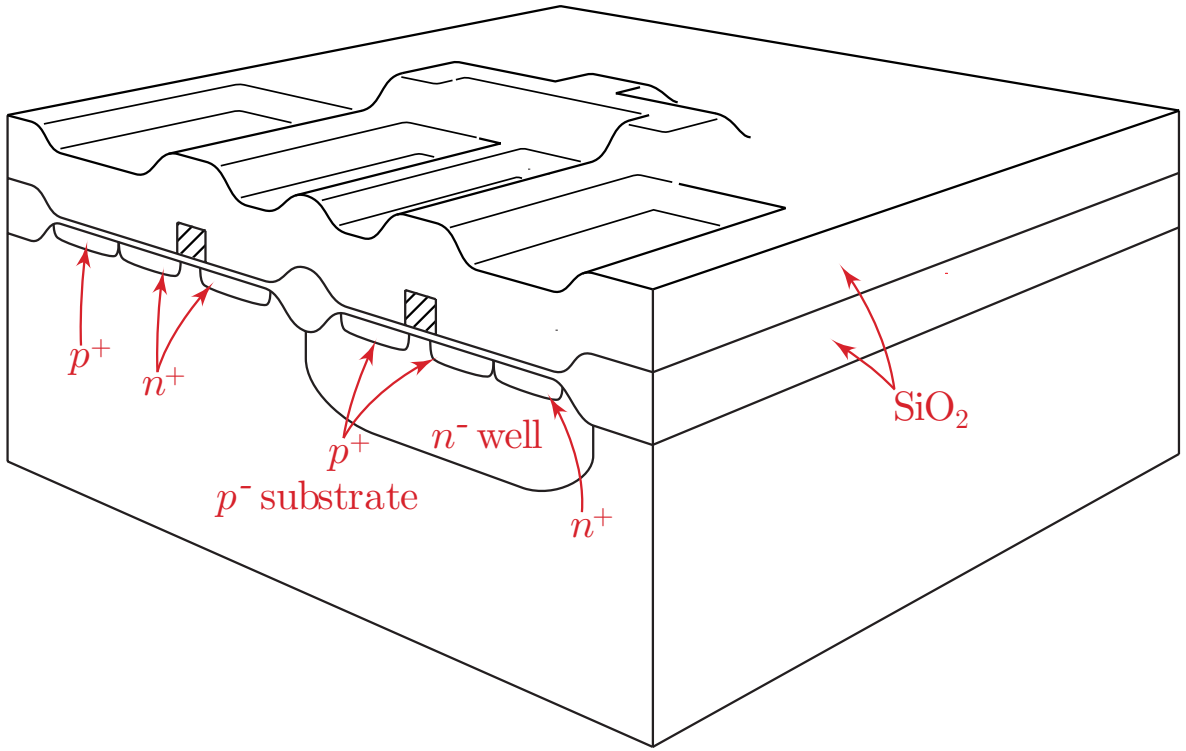
Ion implant for p^+ regions and remove all photoresist

CMOS Fabrication



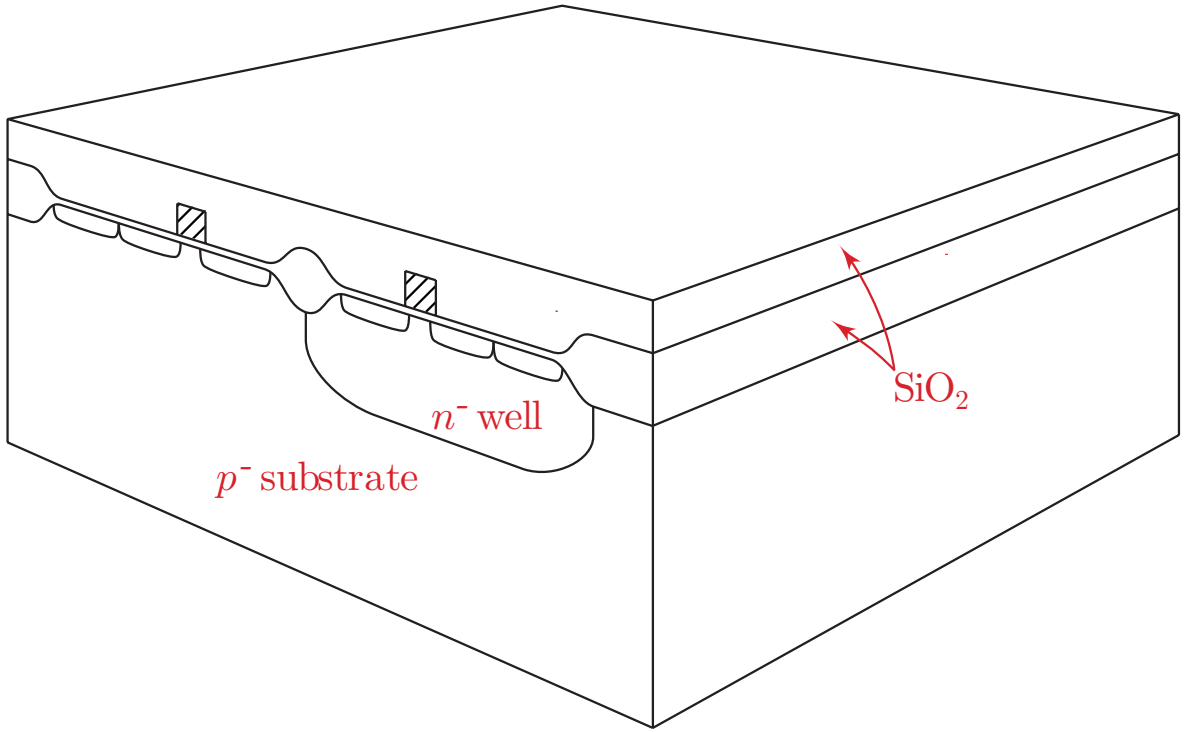
Deposit thick oxide layer over entire surface

CMOS Fabrication



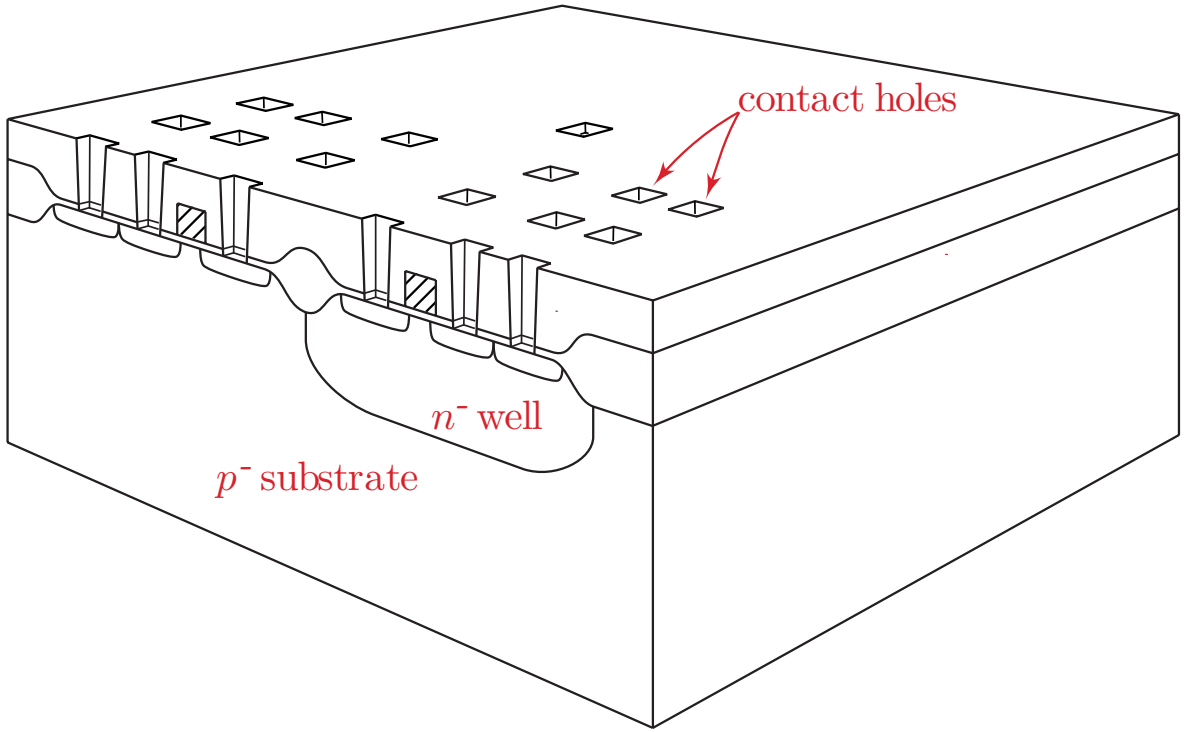
Anneal and drive in both implants

CMOS Fabrication



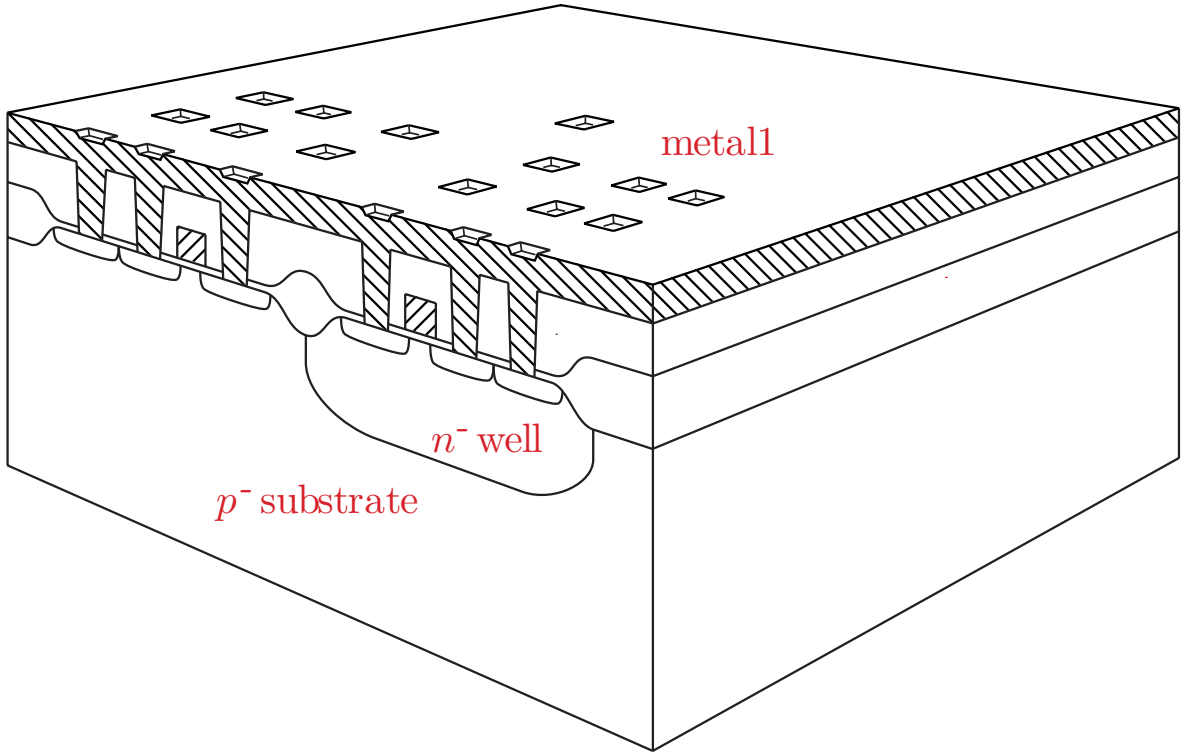
Planarize surface by chemical-mechanical polishing

CMOS Fabrication



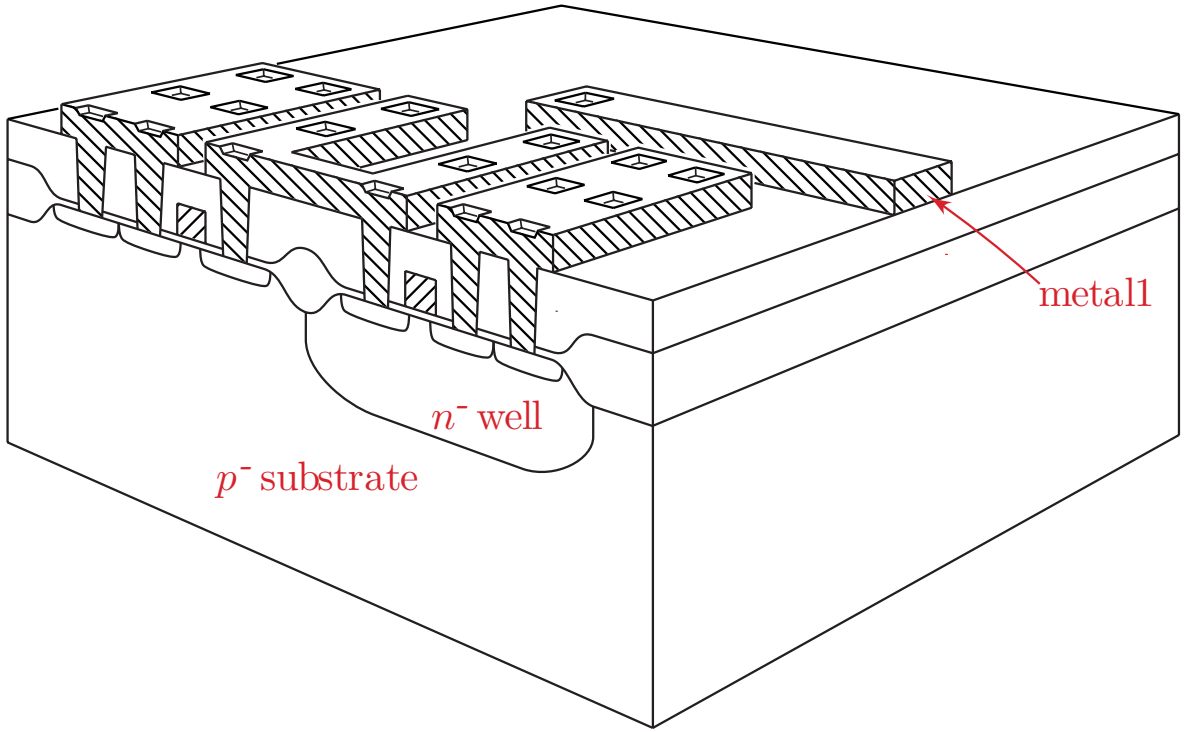
Open contact windows in the oxide

CMOS Fabrication



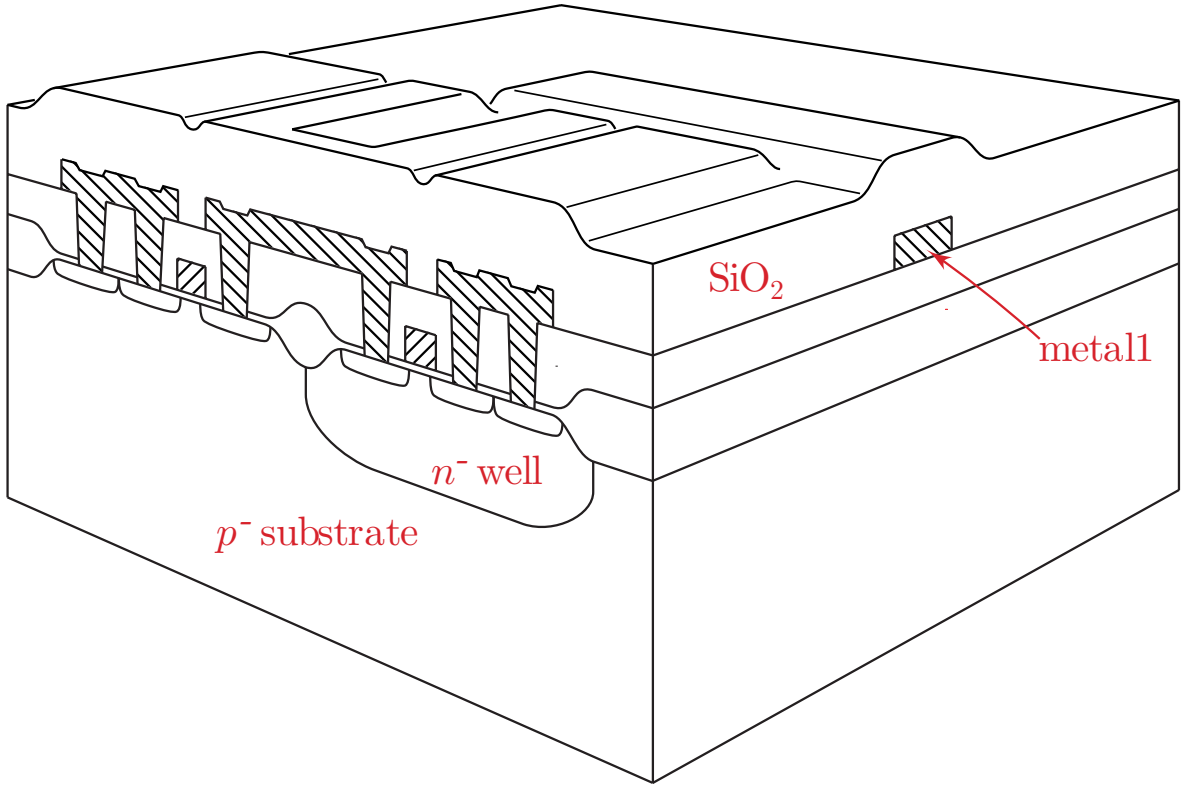
Fill contact holes with metal and deposit metal1

CMOS Fabrication



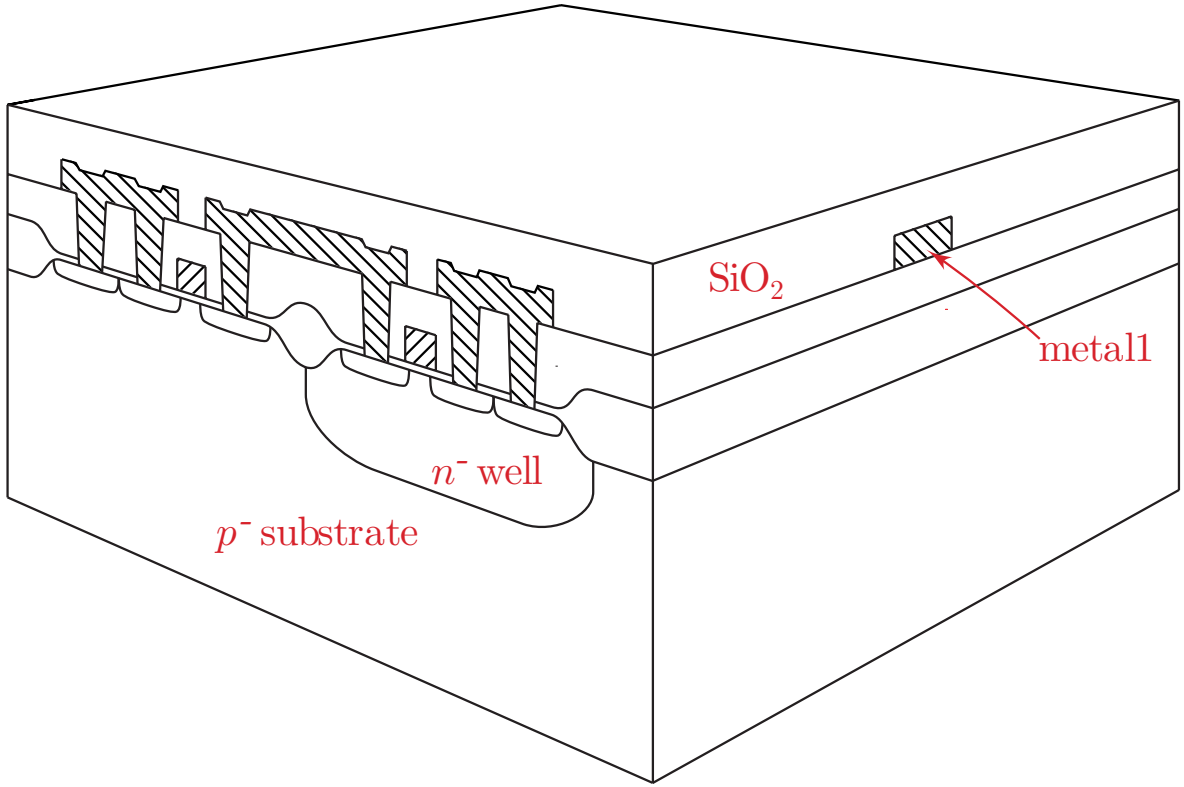
Pattern and selectively etch metal1

CMOS Fabrication



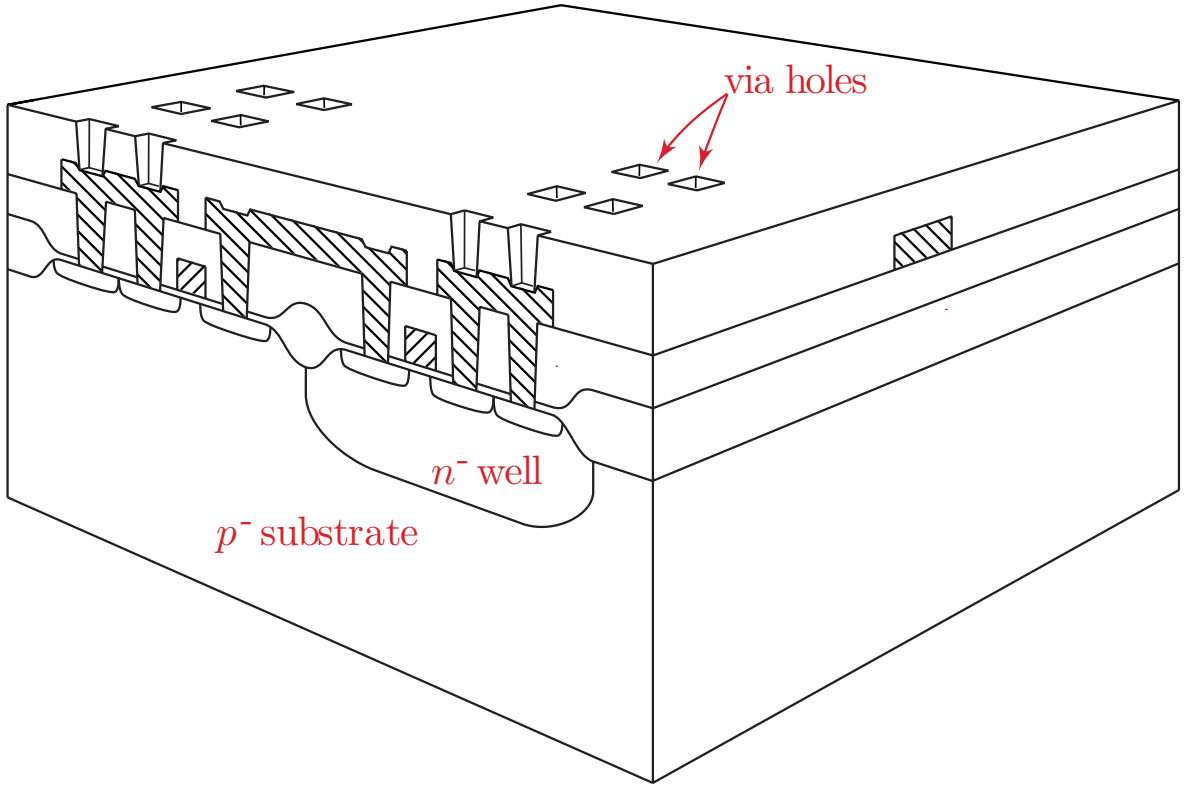
Deposit thick oxide layer over entire surface

CMOS Fabrication



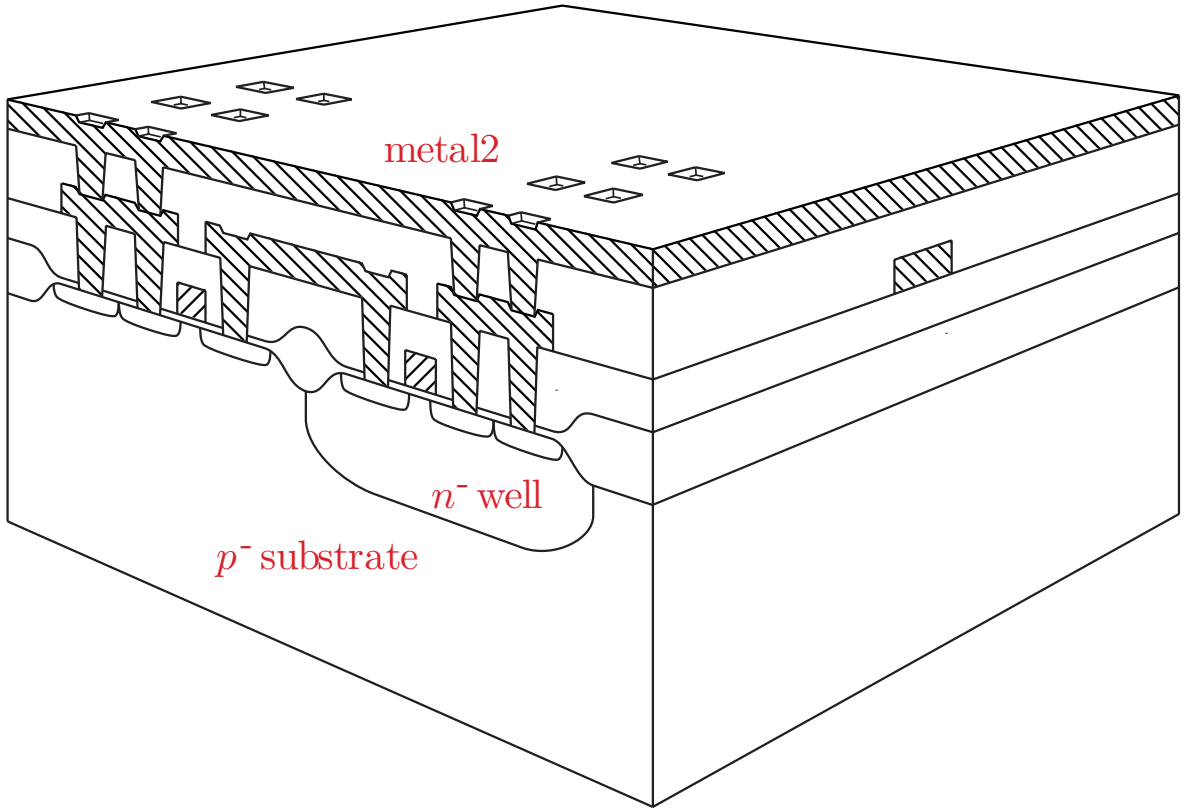
Planarize surface by chemical-mechanical polishing

CMOS Fabrication



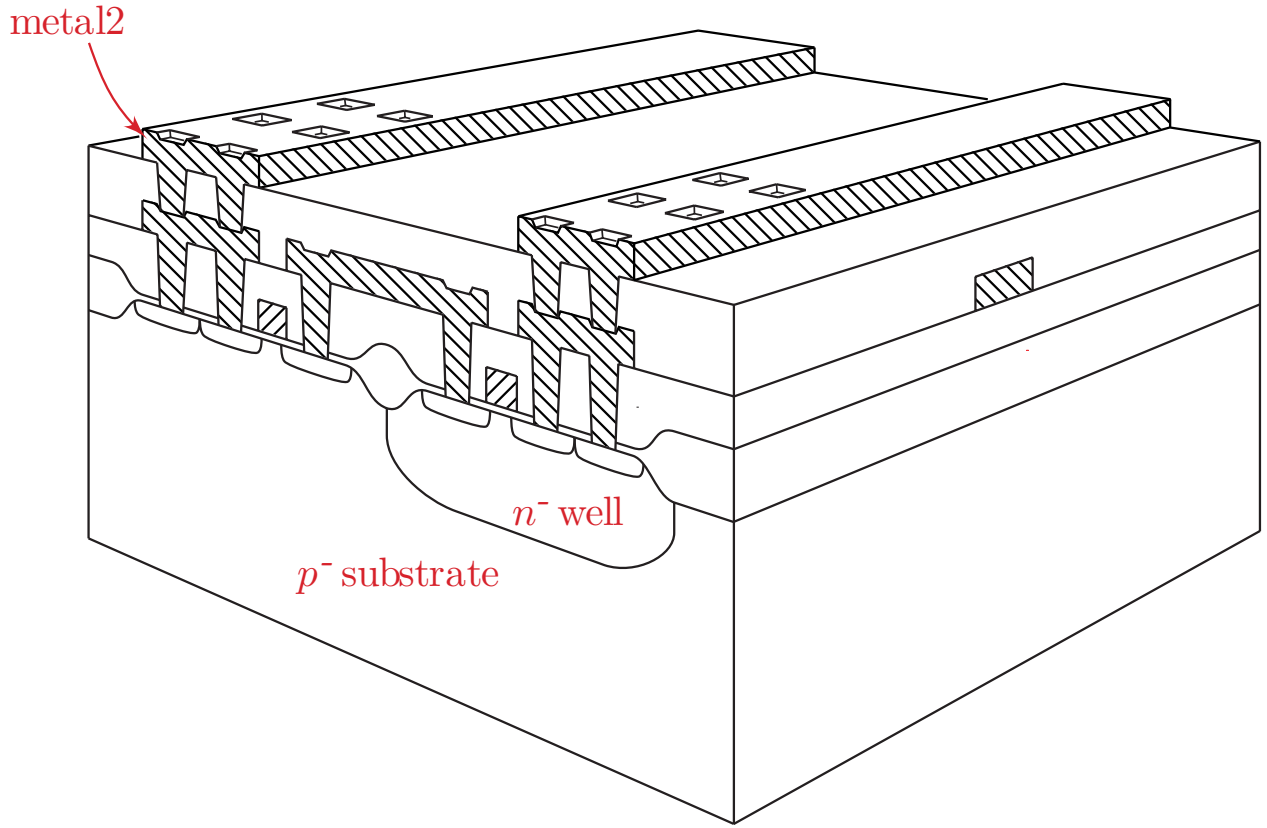
Open via windows in the oxide

CMOS Fabrication



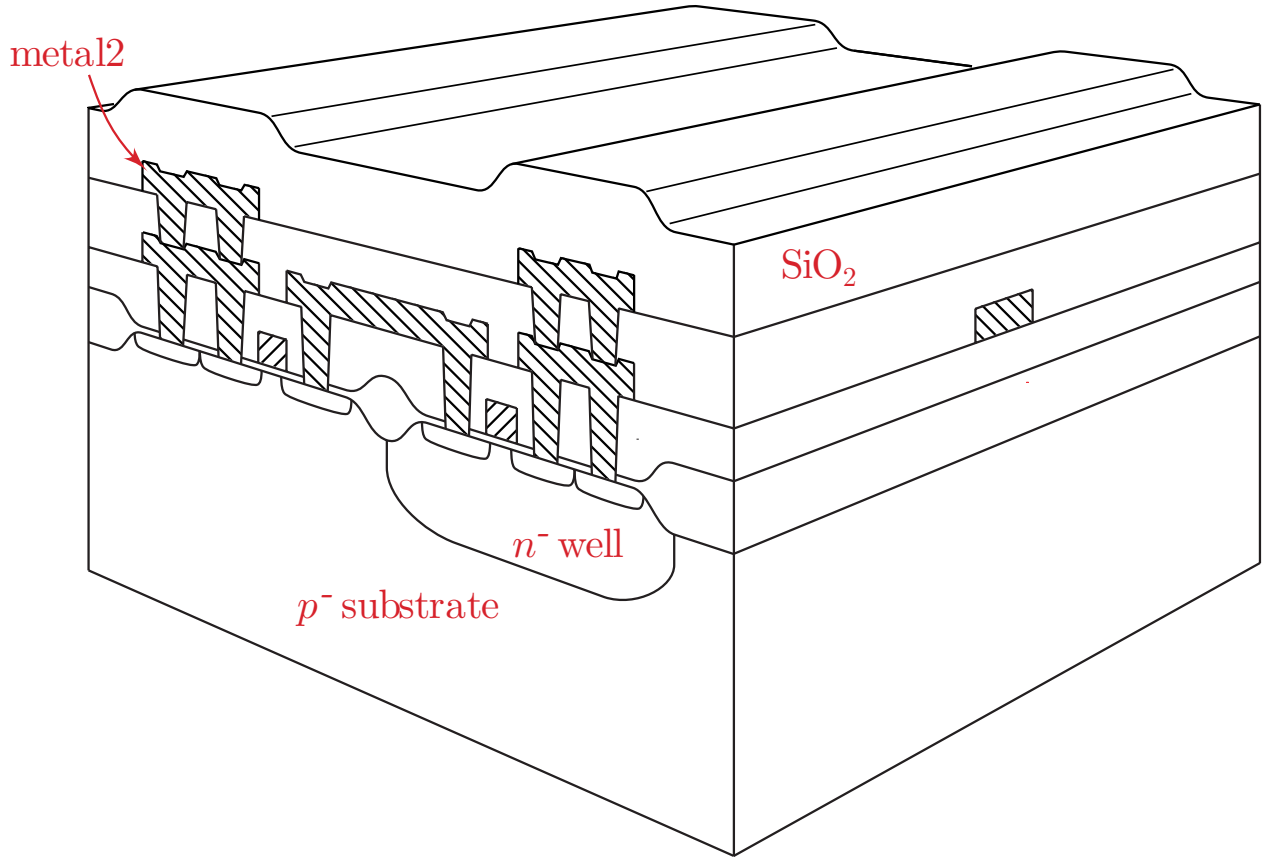
Fill via holes with metal and deposit metal2

CMOS Fabrication



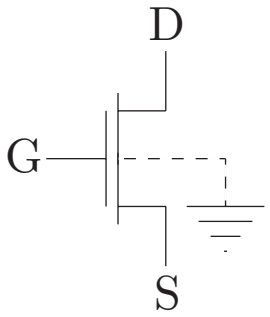
Pattern and selectively remove metal2

CMOS Fabrication

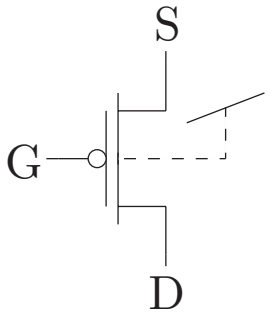


Deposit thick oxide layer over entire surface

MOS Transistor Circuit Symbols



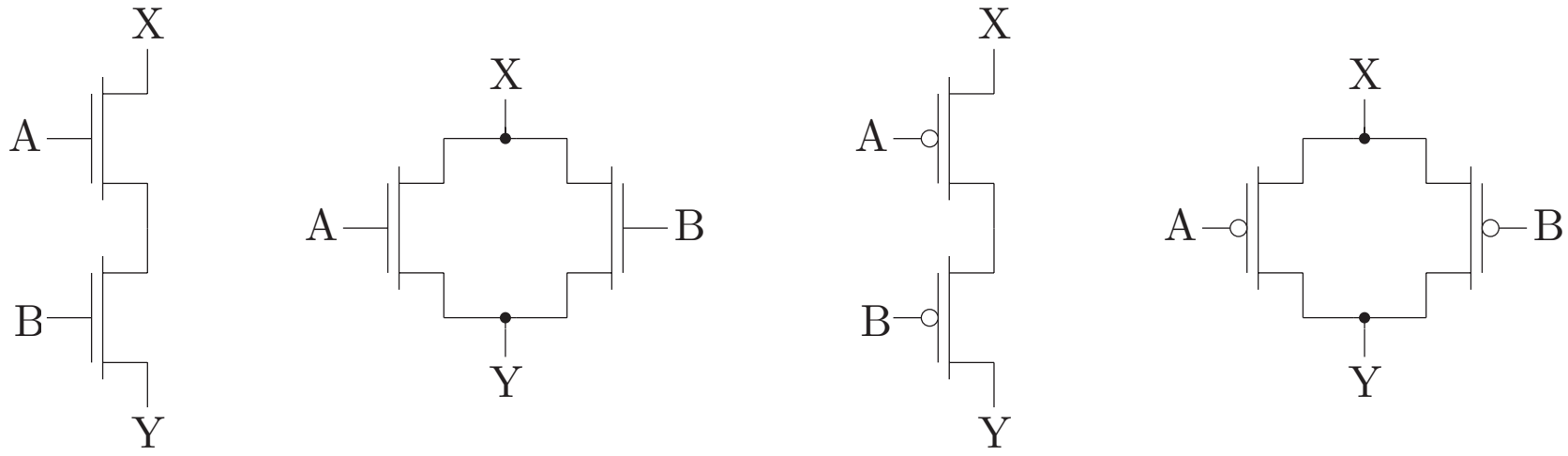
*n*MOS transistor



*p*MOS transistor

MOS Transistor Switch Networks

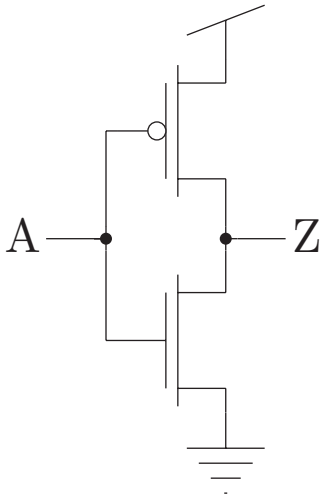
If we represent a logical 0 by 0 V and a logical 1 by V_{DD}, then points X and Y are connected electrically if

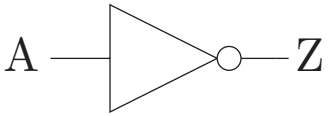


$A \wedge B$ $A \vee B$ $\neg A \wedge \neg B$ $\neg A \vee \neg B$

Transistors connected in series implement a logical AND function while transistors connected in parallel implement a logical OR function!

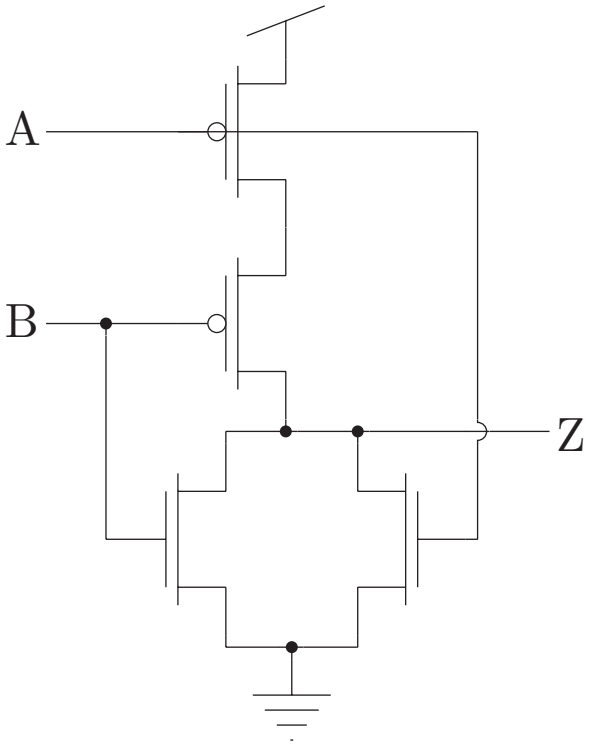
Simple CMOS Logic Gates: NOT ($Z = \neg A$)

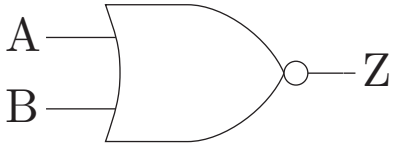




A	Z
0	1
1	0

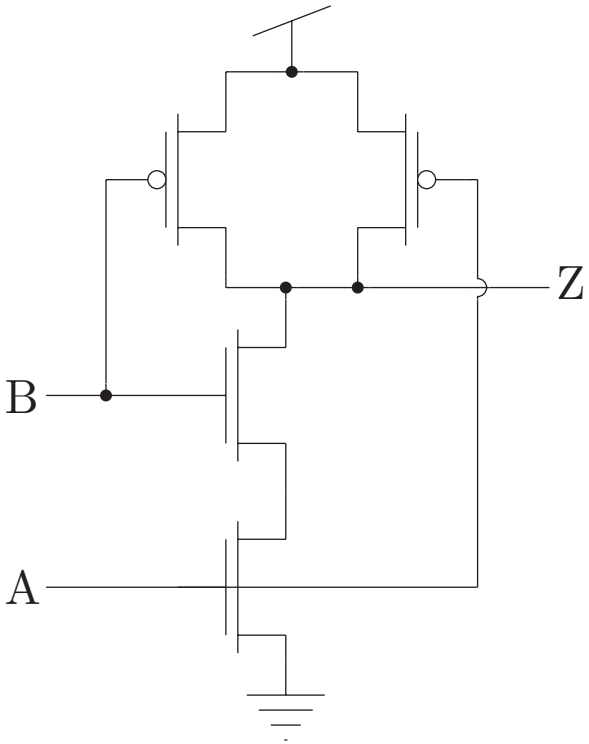
Simple CMOS Logic Gates: NOR ($Z = \neg(A \vee B)$)

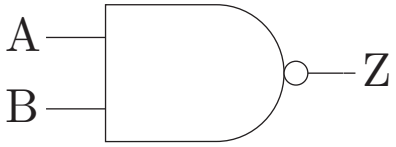




A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

Simple CMOS Logic Gates: NAND ($Z = \neg(A \wedge B)$)





A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0