Mixed Analog–Asynchronous-Digital VLSI Circuit Design

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Mixed-Signal Extensions to CHP

Suppose we extend the underlying asynchronous hardware model to include

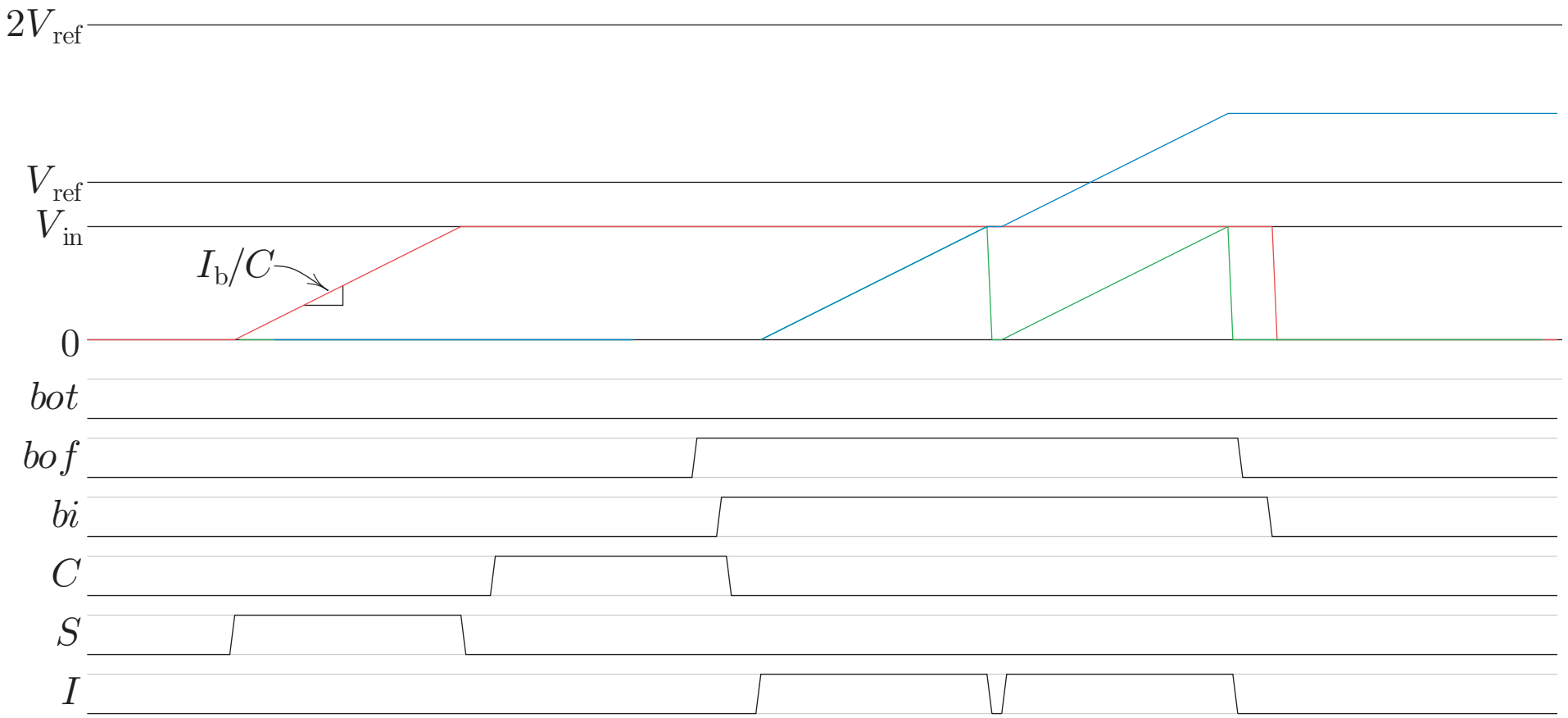
- matched explicit capacitors on certain nodes
- matched current sources/sinks that can be switched on and off
- comparators that can detect when one voltage exceeds another

What sort of MAADness might ensue?

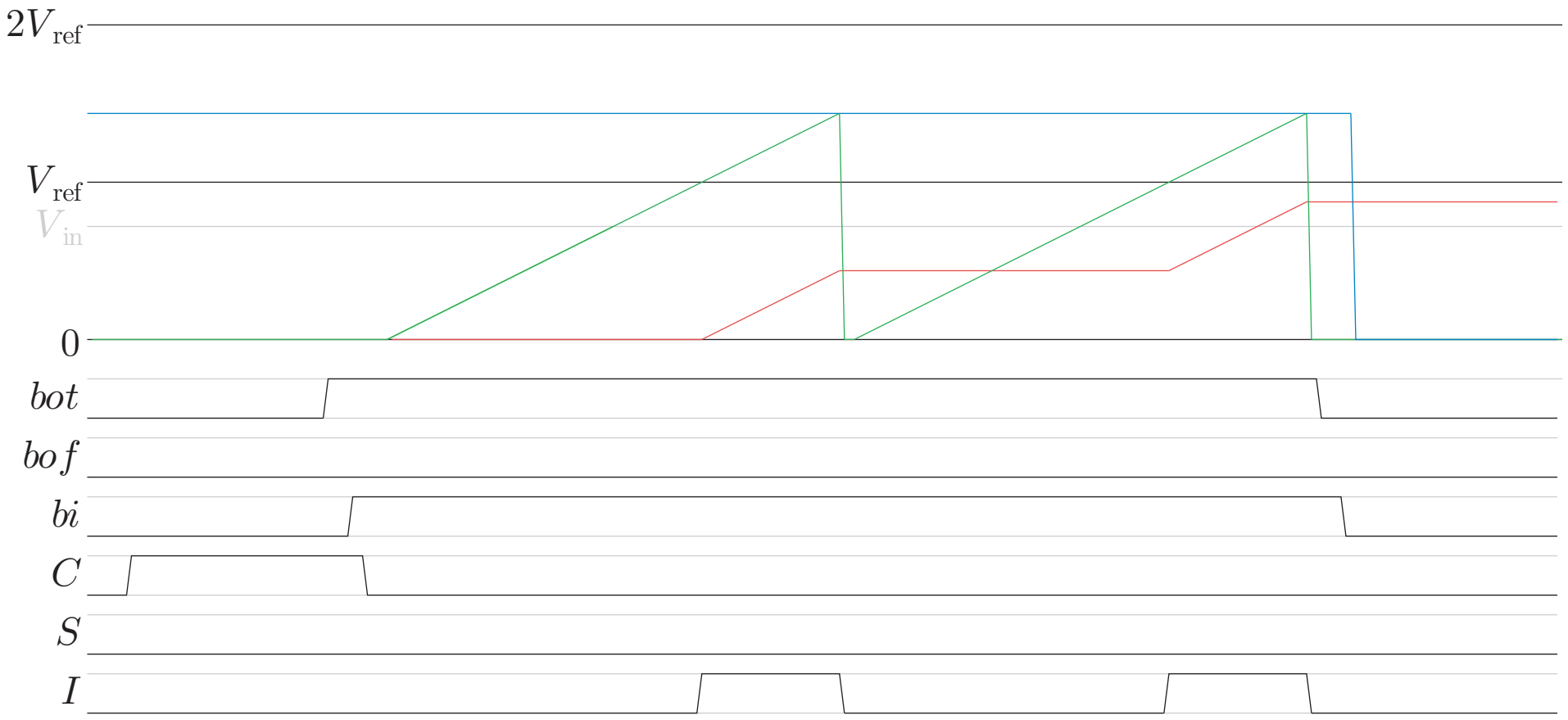
A Notional Algorithmic ADC: Algorithm

$$
\begin{array}{l}
*[[\ S?;\ V_{\text{in}}?V_{\text{red}};\ i := 0 \\
\quad *[\ i < N \longrightarrow \\
\qquad [\ i\%2 = 0 \longrightarrow \\
\qquad\quad [\ V_{\text{red}} \geq V_{\text{ref}} \longrightarrow B!1;\ V_{\text{blue}} := 2 * (V_{\text{red}} - V_{\text{ref}}) \\
\qquad\quad [\!]\ V_{\text{red}} < V_{\text{ref}} \longrightarrow B!0;\ V_{\text{blue}} := 2 * V_{\text{red}} \\
\qquad\quad];\ V_{\text{red}} := 0 \\
\qquad [\!]\ i\%2 = 1 \longrightarrow \\
\qquad\quad [\ V_{\text{blue}} \geq V_{\text{ref}} \longrightarrow B!1;\ V_{\text{red}} := 2 * (V_{\text{blue}} - V_{\text{ref}}) \\
\qquad\quad [\!]\ V_{\text{blue}} < V_{\text{ref}} \longrightarrow B!0;\ V_{\text{red}} := 2 * V_{\text{blue}} \\
\qquad\quad];\ V_{\text{blue}} := 0 \\
\qquad];\ i := i + 1 \\
\quad] \\
]]
\end{array}
$$

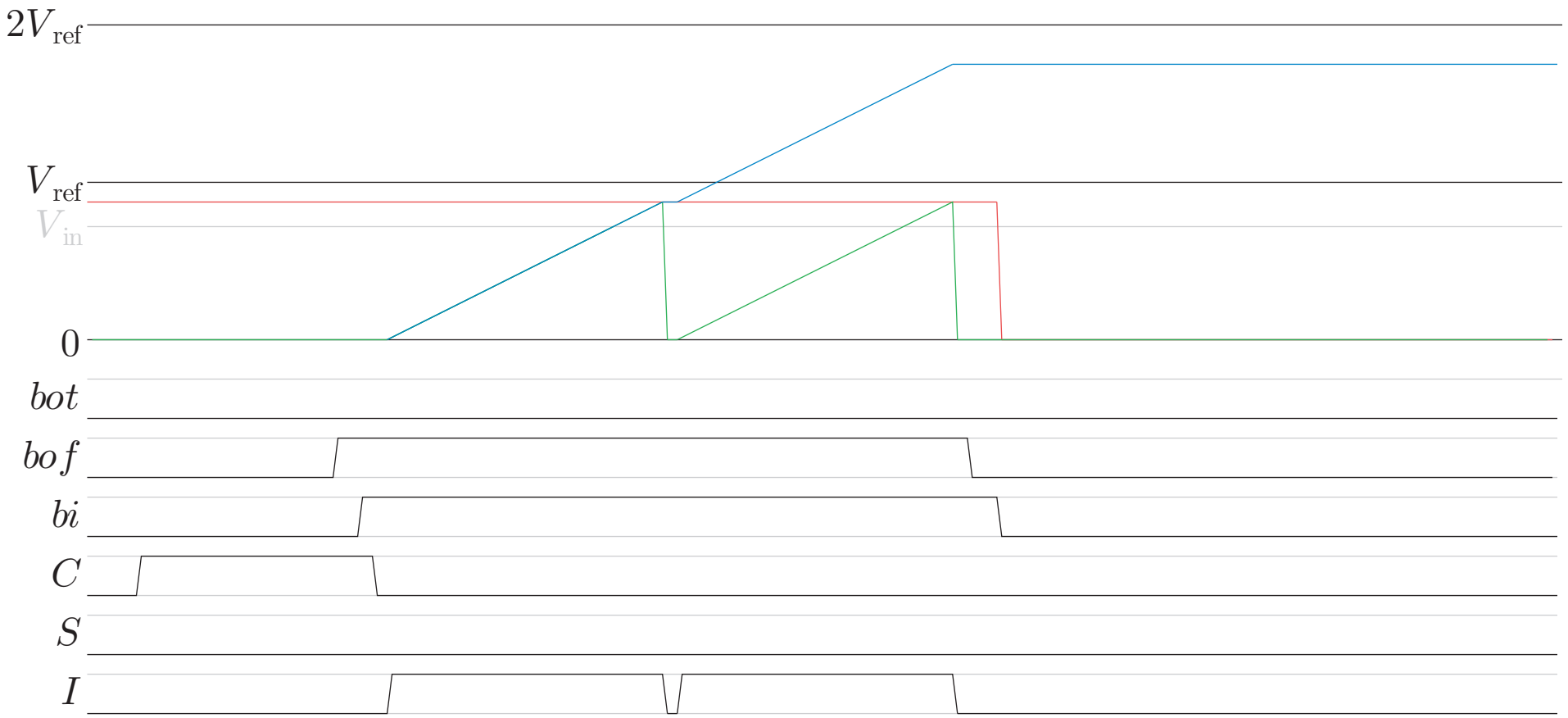
A Notional Algorithmic ADC: Timing



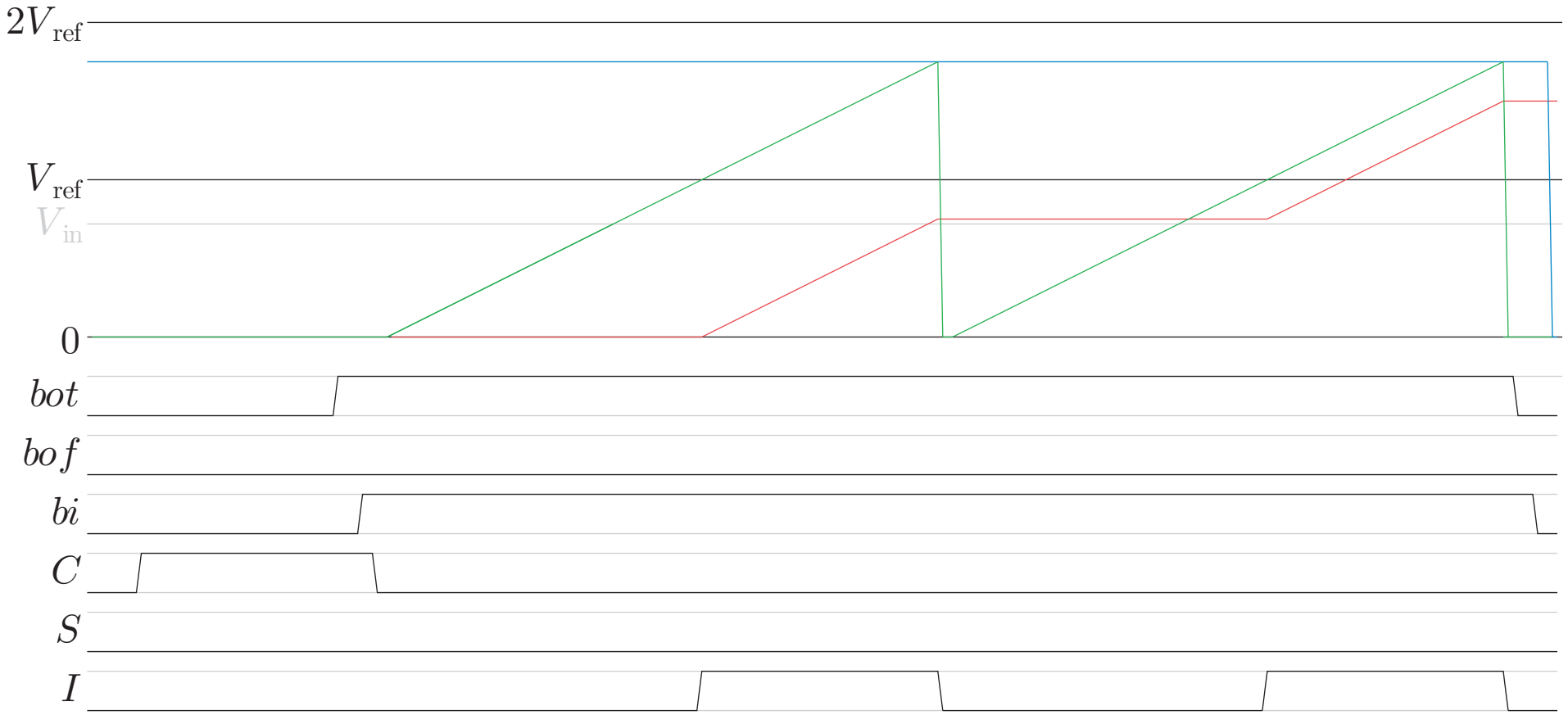
A Notional Algorithmic ADC: Timing



A Notional Algorithmic ADC: Timing



A Notional Algorithmic ADC: Timing



A Notional Algorithmic ADC: Timing