Low-Voltage Wilson Current Mirrors in CMOS

Bradley A. Minch

Mixed Analog-Digital VLSI Circuits and Systems Lab
Franklin W. Olin College of Engineering
Needham, MA 02492–1200

bradley.minch@olin.edu

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Simple EKV MOS Transistor Model

We model the channel current of an *n*MOS transistor as the difference between a forward current and a reverse current,

$$I = I_{\mathrm{F}} - I_{\mathrm{R}},$$

whose values are given by

$$I_{\mathrm{F(R)}} = I_{\mathrm{s}} \log^2 \left(1 + e^{\left(\kappa(V_{\mathrm{G}} - V_{\mathrm{T0}}) - V_{\mathrm{S(D)}}\right)/2U_{\mathrm{T}}}\right),$$

where

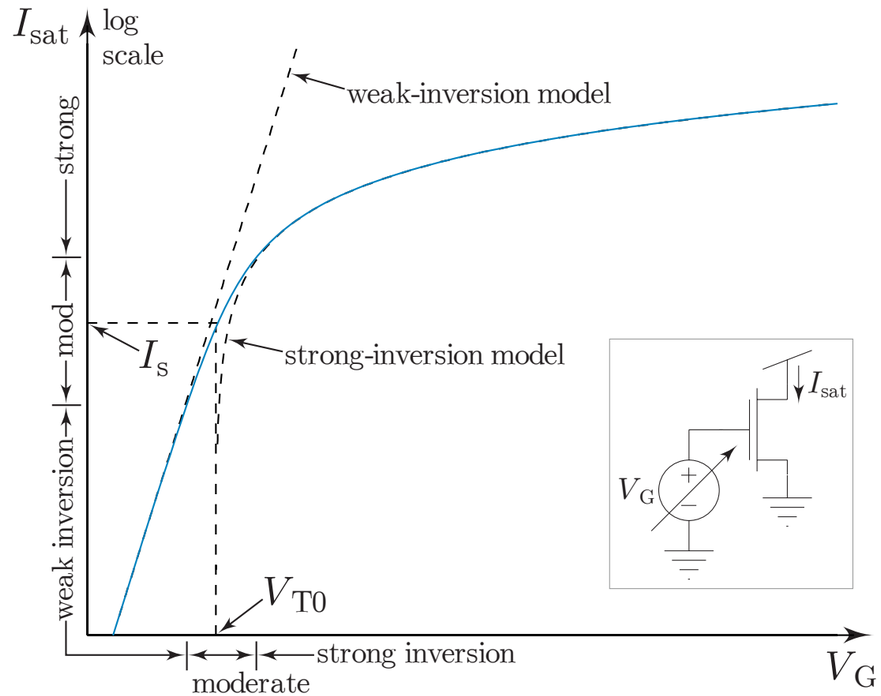
$$U_{\mathrm{T}} = \frac{kT}{q}, \quad I_{\mathrm{s}} = \frac{W}{L} \cdot \frac{2\mu C_{\mathrm{ox}} U_{\mathrm{T}}^2}{\kappa}, \quad \text{and} \quad \kappa = \frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}} + C_{\mathrm{dep}}}.$$

Note that $\kappa = 1/n$ and that I_{s} is approximately twice the saturation current at threshold. This simple model covers all regions of normal MOS transistor operation and is both continuous and smooth.

Simple EKV MOS Transistor Model

The expressions for I_{F} and I_{R} reduce asymptotically to an exponential form in weak inversion and a quadratic form in strong inversion, given by

$$I_{\mathrm{F(R)}} \approx \begin{cases} I_{\mathrm{s}} e^{\left(\kappa(V_{\mathrm{G}}-V_{\mathrm{T0}})-V_{\mathrm{S(D)}}\right)/U_{\mathrm{T}}}, \\ \qquad V_{\mathrm{G}} < V_{\mathrm{T0}} + \dfrac{V_{\mathrm{S(D)}}}{\kappa} \\ \dfrac{W}{L} \cdot \dfrac{\mu C_{\mathrm{ox}}}{2\kappa} \left(\kappa\left(V_{\mathrm{G}} - V_{\mathrm{T0}}\right) - V_{\mathrm{S(D)}}\right)^2, \\ \qquad V_{\mathrm{G}} > V_{\mathrm{T0}} + \dfrac{V_{\mathrm{S(D)}}}{\kappa}. \end{cases}$$



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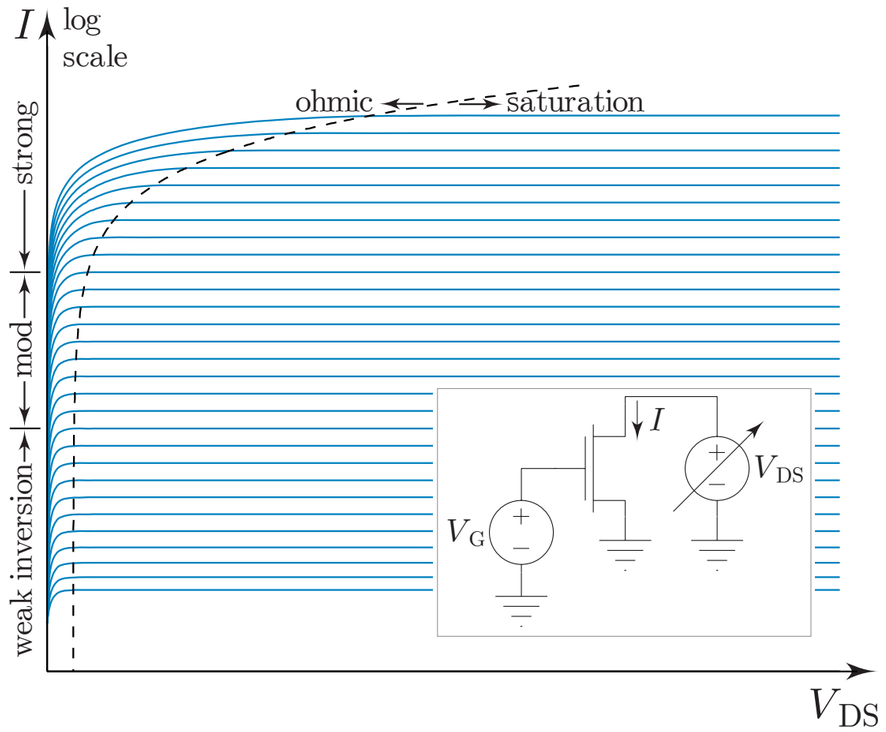
The Onset of Saturation

Note that I_F depends only on V_G and V_S and that I_R depends only on V_G and V_D. If $I_\mathrm{F} \gg I_\mathrm{R}$, then $I \approx I_\mathrm{F}$ and is nearly independent of V_D, which corresponds qualitatively to the saturation region of operation, so $I_\mathrm{sat} \approx I_\mathrm{F}$. We can define the onset of saturation operationally in terms of an arbitrary parameter, $A \gg 1$: We say that an MOS transistor is saturated if $I_\mathrm{F}/I_\mathrm{R} \geq A$. Using this notion, we can find an expression for V_DSsat, given by

$$
\begin{aligned}
V_\mathrm{DSsat} &= 2U_\mathrm{T} \log \frac{e^{\sqrt{I_\mathrm{sat}/I_\mathrm{s}}} - 1}{e^{\sqrt{I_\mathrm{sat}/AI_\mathrm{s}}} - 1} \\
&\approx \begin{cases} U_\mathrm{T} \log A, & I_\mathrm{sat} \ll I_\mathrm{s} \\ 2U_\mathrm{T} \left(1 - \dfrac{1}{\sqrt{A}}\right) \sqrt{\dfrac{I_\mathrm{sat}}{I_\mathrm{s}}}, & I_\mathrm{sat} \gg I_\mathrm{s}. \end{cases}
\end{aligned}
$$



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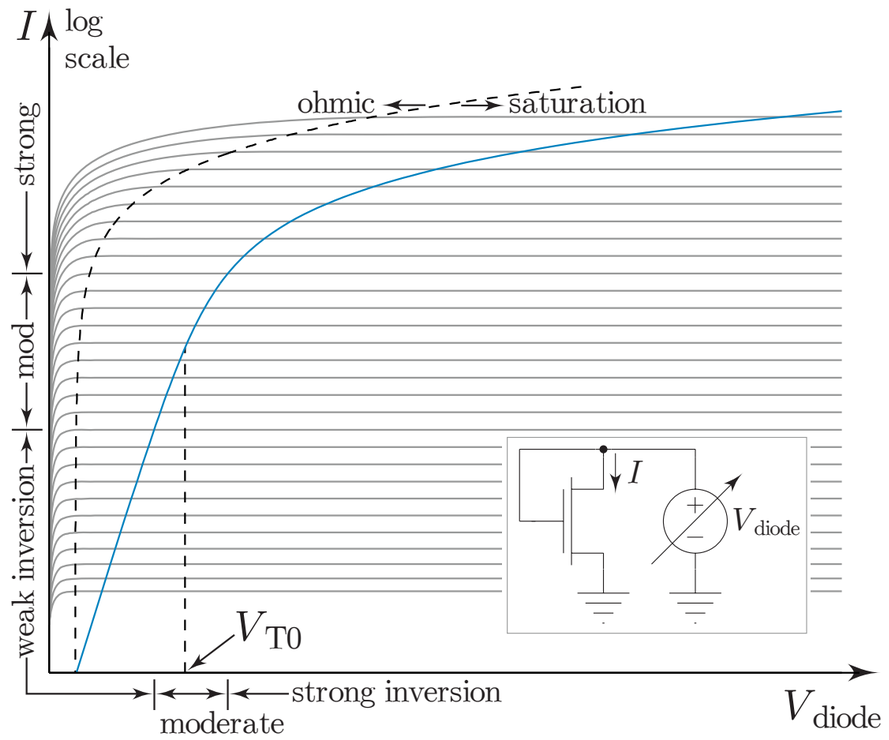
The Diode-Connected MOS Transistor

If we short the drain and gate of an MOS transistor, it acts qualitatively as a diode, allowing current to flow only in one direction. For all current levels of practical interest, the diode-connected MOS transistor operates in saturation. We can find an expression for the voltage across a diode-connected *n*MOS transistor as

$$
\begin{aligned}
V_{\text{diode}} &= V_{\text{T0}} + \frac{1-\kappa}{\kappa} \cdot V_{\text{S}} + \frac{2U_{\text{T}}}{\kappa} \cdot \log\left(e^{\sqrt{I_{\text{sat}}/I_{\text{s}}}} - 1\right) \\
&\approx \begin{cases} V_{\text{T0}} + \dfrac{1-\kappa}{\kappa} \cdot V_{\text{S}} + \dfrac{U_{\text{T}}}{\kappa} \log \dfrac{I_{\text{sat}}}{I_{\text{s}}}, \\ \qquad I_{\text{sat}} \ll I_{\text{s}} \\ V_{\text{T0}} + \dfrac{1-\kappa}{\kappa} \cdot V_{\text{S}} + \dfrac{2U_{\text{T}}}{\kappa} \sqrt{\dfrac{I_{\text{sat}}}{I_{\text{s}}}}, \\ \qquad I_{\text{sat}} \gg I_{\text{s}}. \end{cases}
\end{aligned}
$$



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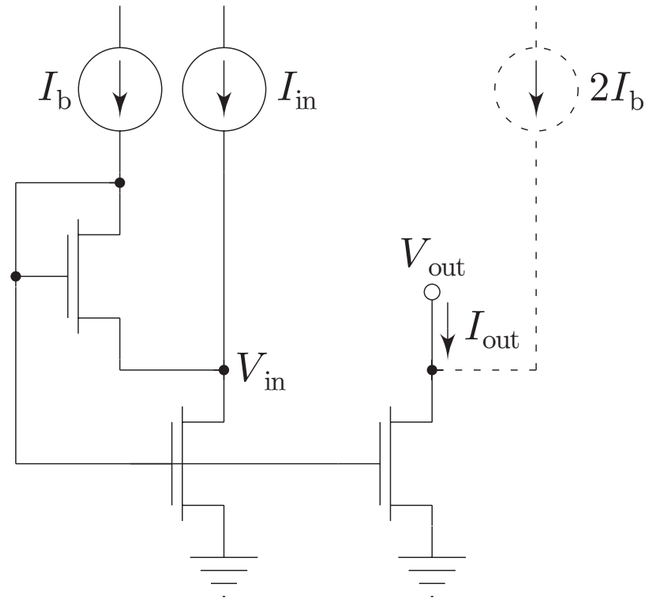
A Low-Input-Voltage Simple Current Mirror

Shown to the right is an analog of the simple current mirror that operates with a low input voltage. For the bottom transistor in the input branch, we can show that

$$\frac{I_\mathrm{F}}{I_\mathrm{R}} = 2 + \frac{I_\mathrm{in}}{I_\mathrm{b}}$$

regardless of the current levels represented by I_in and I_b. If $I_\mathrm{in} \gg I_\mathrm{b}$, then $I_\mathrm{F}/I_\mathrm{R} \gg 1$ and the input voltage is nearly V_DSsat at the I_in current level.

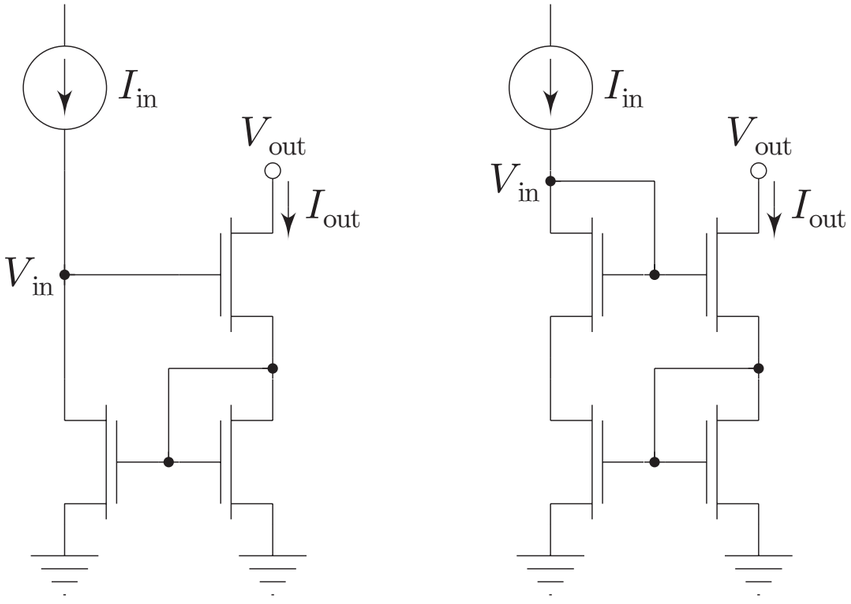
If $V_\mathrm{out} > V_\mathrm{DSsat}$, we can show that I_out is equal to $I_\mathrm{in} + 2I_\mathrm{b}$. If $I_\mathrm{in} \gg I_\mathrm{b}$, then $I_\mathrm{out} \approx I_\mathrm{in}$, and the circuit functions as a simple mirror. If $I_\mathrm{in} \approx I_\mathrm{b}$, there is a systematic error of $2I_\mathrm{b}$, which we can easily compensate as shown.



Wilson Current Mirrors in CMOS

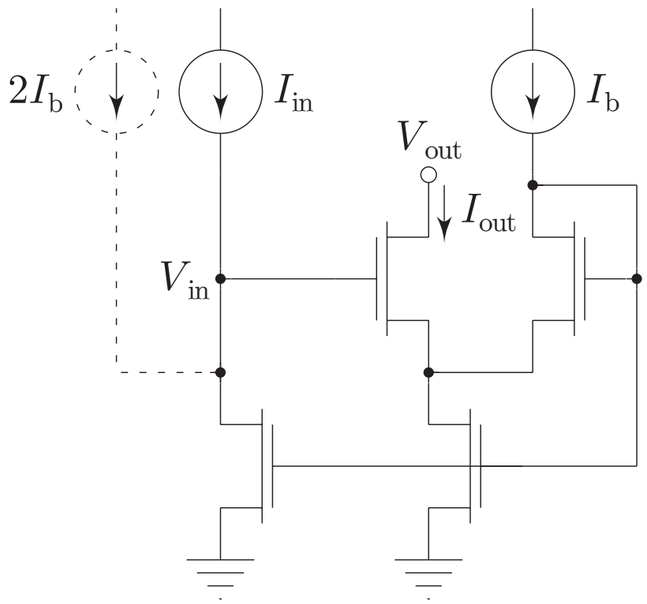
In 1967, George Wilson and Barrie Gilbert entered into a friendly competition to see who could devise the best current mirror with only three transistors. Wilson won and his mirror, in its bipolar form, has been a first choice among designers whose applications necessitate good immunity to finite β_F and a high R_{out}. At the time, Gilbert suggested adding a diode-connected transistor in the input branch to reduce a systematic gain error due to the Early effect, whence the super-Wilson mirror.

However, neither is suitable for use in CMOS on a low supply voltage, because each requires an input voltage of more than $2V_{diode} + V_{DSsat}$ and an output compliance voltage of $V_{diode} + V_{DSsat}$.

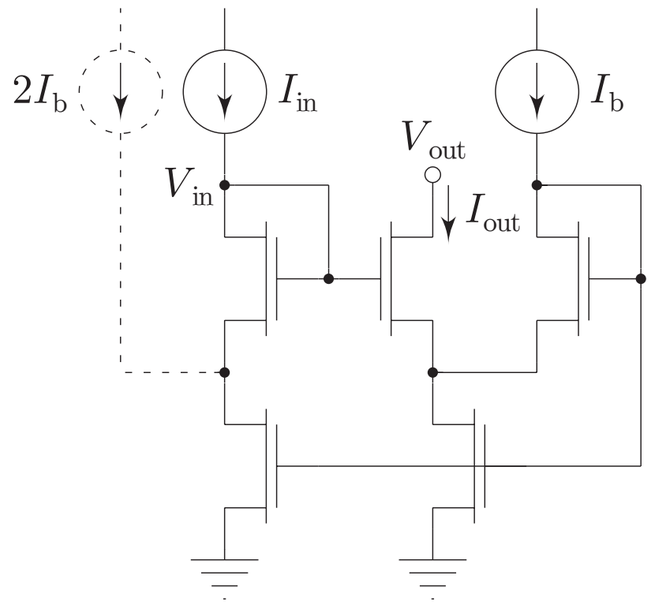


Wilson Super-Wilson

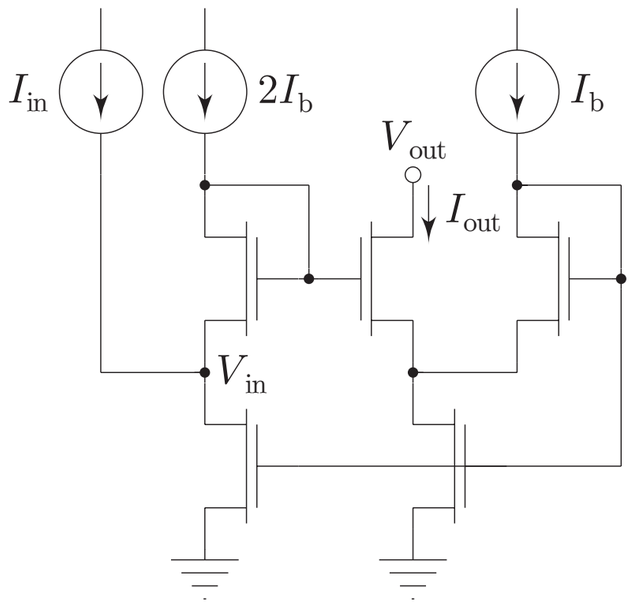
Low-Voltage Wilson Current Mirrors in CMOS



High-Swing Wilson



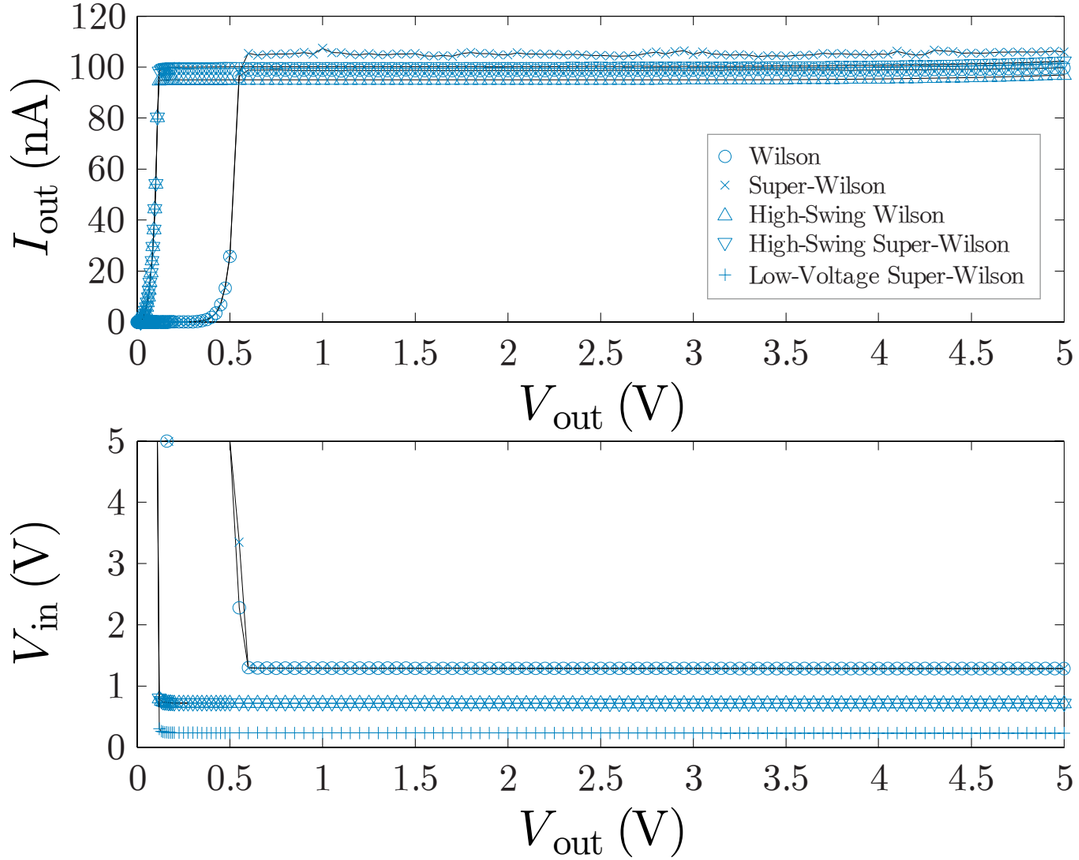
High-Swing Super-Wilson

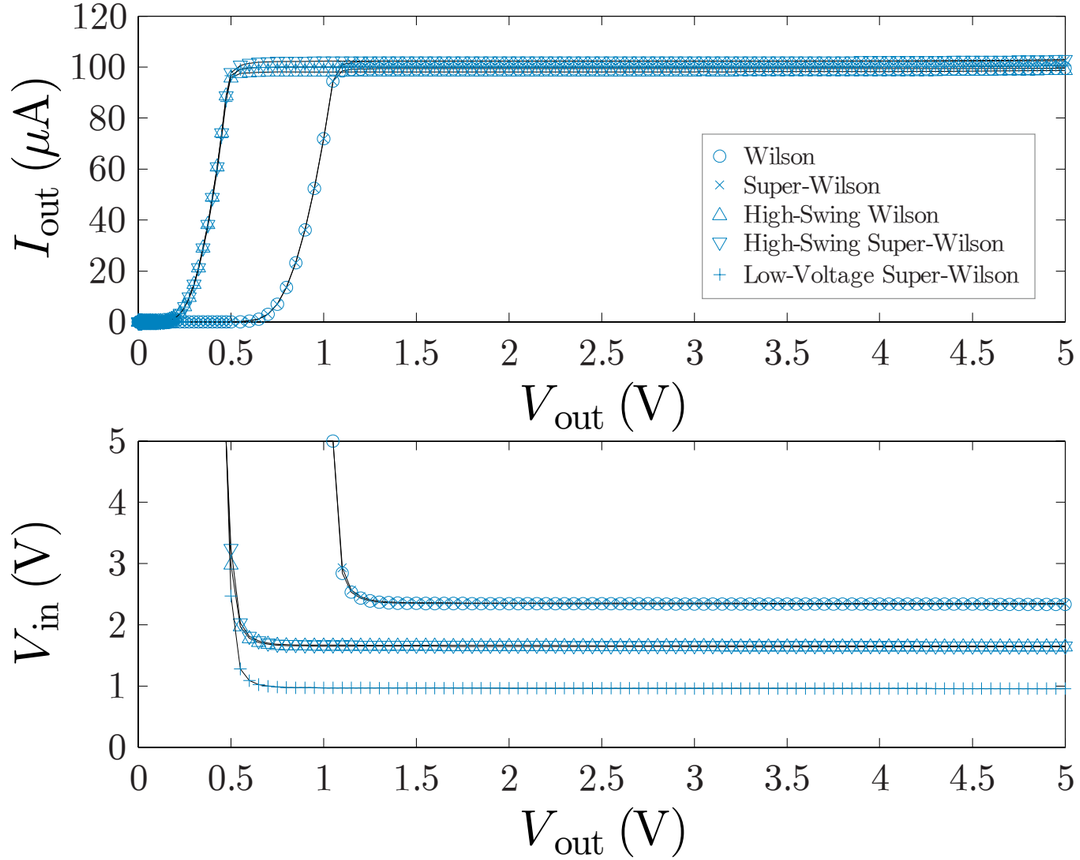


Low-Voltage Super-Wilson

Shown above are low-voltage, high-swing analogs of the Wilson and super-Wilson mirrors. Each operates at all current levels with an output compliance voltage of $2V_{\text{DSsat}}$ and a minimum supply voltage of $V_{\text{diode}} + 2V_{\text{DSsat}}$. The two on the left operate with an input voltage of $V_{\text{diode}} + V_{\text{DSsat}}$ while the third operates with an input voltage of V_{DSsat}.

Measured Output Characteristics in Moderate and in Strong Inversion





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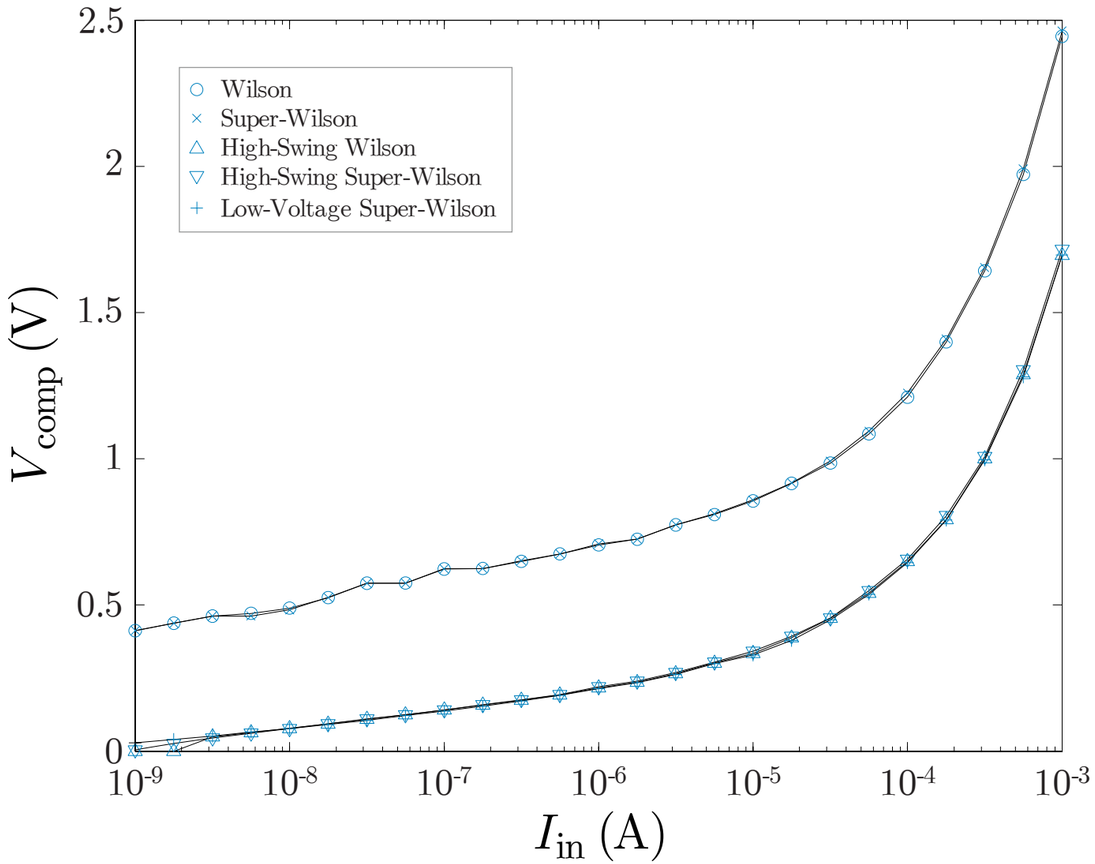
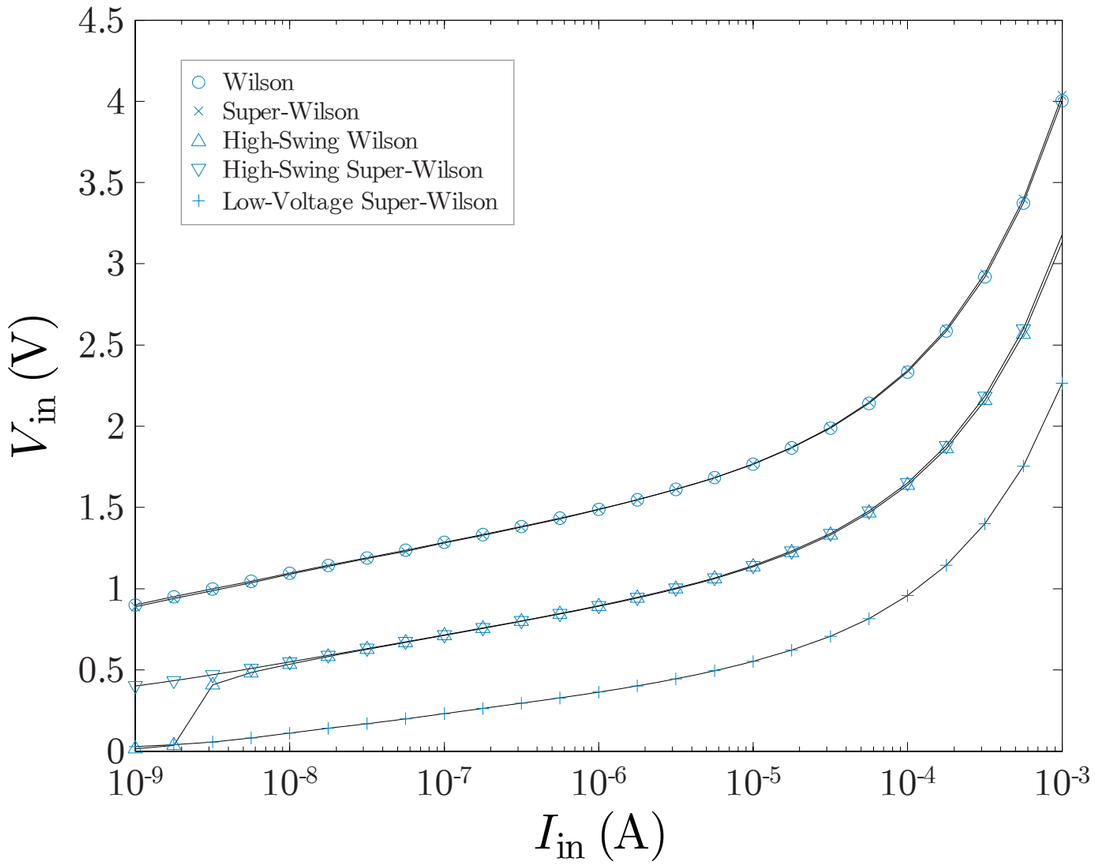
Measured Output Compliance and Input Voltage versus Input Current





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Summary

We have presented three low-voltage CMOS analogs of the Wilson current mirror that each

- can operate well at any level of inversion,
- can operate on a low supply voltage of only $V_{\text{diode}} + 2V_{\text{DSsat}}$,
- has a similar incremental R_{out} to a cascode mirror,
- and has an output compliance voltage of $2V_{\text{DSsat}}$, permitting a wide output swing.

Two of these new mirrors operate with a nominal input voltage of $V_{\text{diode}}+V_{\text{DSsat}}$ while the third operates with a low input voltage of V_{DSsat}. We provided DC measurements from versions of these mirrors that were fabricated in a 0.5-μm CMOS process through MOSIS along with a comparison with CMOS implementations of the conventional Wilson and super-Wilson mirrors.